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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	1395
Number of Logic Elements/Cells	22320
Total RAM Bits	608256
Number of I/O	153
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce22f17c7

Visual Cue	Meaning
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, <code>data1</code> , <code>tdi</code> , and <code>input</code> . The suffix <code>n</code> denotes an active-low signal. For example, <code>resetn</code> . Indicates command line commands and anything that must be typed exactly as it appears. For example, <code>c:\qdesigns\tutorial\chiptrip.gdf</code> . Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <code>SUBDESIGN</code>), and logic function names (for example, <code>TRI</code>).
	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.

Read or Write Clock Mode

Cyclone IV devices M9K memory blocks can implement read or write clock mode for FIFO and simple dual-port memories. In this mode, a write clock controls the data inputs, write address, and wren registers. Similarly, a read clock controls the data outputs, read address, and rden registers. M9K memory blocks support independent clock enables for both the read and write clocks.

When using read or write mode, if you perform a simultaneous read or write to the same address location, the output read data is unknown. If you require the output data to be a known value, use either single-clock mode, input clock mode, or output clock mode and choose the appropriate read-during-write behavior in the MegaWizard Plug-In Manager.

Single-Clock Mode

Cyclone IV devices M9K memory blocks can implement single-clock mode for FIFO, ROM, true dual-port, simple dual-port, and single-port memories. In this mode, you can control all registers of the M9K memory block with a single clock together with clock enable.

Design Considerations

This section describes designing with M9K memory blocks.

Read-During-Write Operations

“Same-Port Read-During-Write Mode” on page 3-16 and “Mixed-Port Read-During-Write Mode” on page 3-16 describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address.

There are two read-during-write data flows: same-port and mixed-port. Figure 3-13 shows the difference between these flows.

Figure 3-13. Cyclone IV Devices Read-During-Write Data Flow

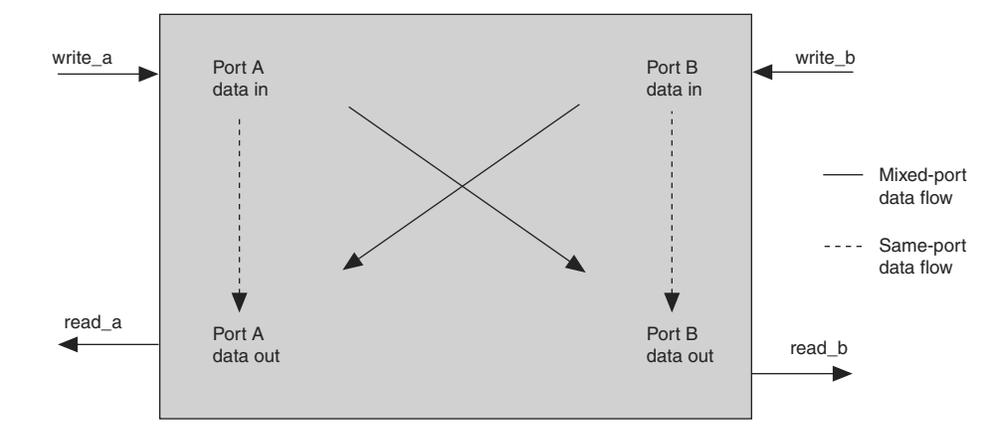


Table 4–1 lists the number of embedded multipliers and the multiplier modes that can be implemented in each Cyclone IV device.

Table 4–1. Number of Embedded Multipliers in Cyclone IV Devices

Device Family	Device	Embedded Multipliers	9 × 9 Multipliers ⁽¹⁾	18 × 18 Multipliers ⁽¹⁾
Cyclone IV GX	EP4CGX15	0	0	0
	EP4CGX22	40	80	40
	EP4CGX30	80	160	80
	EP4CGX50	140	280	140
	EP4CGX75	198	396	198
	EP4CGX110	280	560	280
	EP4CGX150	360	720	360
Cyclone IV E	EP4CE6	15	30	15
	EP4CE10	23	46	23
	EP4CE15	56	112	56
	EP4CE22	66	132	66
	EP4CE30	66	132	66
	EP4CE40	116	232	116
	EP4CE55	154	308	154
	EP4CE75	200	400	200
	EP4CE115	266	532	266

Note to Table 4–1:

(1) These columns show the number of 9 × 9 or 18 × 18 multipliers for each device.

In addition to the embedded multipliers in Cyclone IV devices, you can implement soft multipliers by using the M9K memory blocks as look-up tables (LUTs). The LUTs contain partial results from the multiplication of input data with coefficients that implement variable depth and width high-performance soft multipliers for low-cost, high-volume DSP applications. The availability of soft multipliers increases the number of available multipliers in the device.



For more information about M9K memory blocks, refer to the *Memory Blocks in Cyclone IV Devices* chapter.



For more information about soft multipliers, refer to *AN 306: Implementing Multipliers in FPGA Devices*.

Architecture

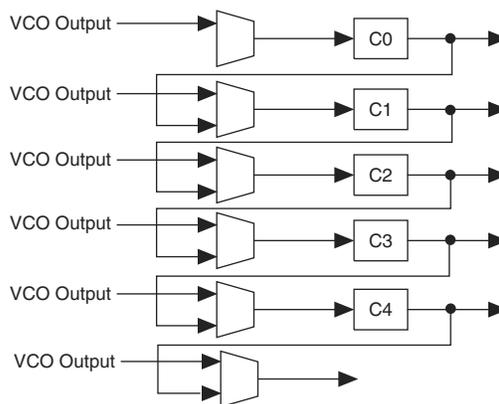
Each embedded multiplier consists of the following elements:

- Multiplier stage
- Input and output registers
- Input and output interfaces

Post-Scale Counter Cascading

PLLs of Cyclone IV devices support post-scale counter cascading to create counters larger than 512. This is implemented by feeding the output of one C counter into the input of the next C counter, as shown in Figure 5-16.

Figure 5-16. Counter Cascading



When cascading counters to implement a larger division of the high-frequency VCO clock, the cascaded counters behave as one counter with the product of the individual counter settings.

For example, if $C0 = 4$ and $C1 = 2$, the cascaded value is $C0 \times C1 = 8$.

 Post-scale counter cascading is automatically set by the Quartus II software in the configuration file. Post-scale counter cascading cannot be performed using the PLL reconfiguration.

Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on the PLL post-scale counters. You can achieve the duty cycle setting by a low and high time count setting for the post-scale counters. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices. The post-scale counter value determines the precision of the duty cycle. The precision is defined by 50% divided by the post-scale counter value. For example, if the C0 counter is 10, steps of 5% are possible for duty cycle choices between 5 to 90%.

Combining the programmable duty cycle with programmable phase shift allows the generation of precise non-overlapping clocks.

PLL Control Signals

You can use the `pfdena`, `areset`, and `locked` signals to observe and control the PLL operation and resynchronization.

 For more information about the PLL control signals, refer to the *ALTPLL Megafunction User Guide*.

Table 6-2 on page 6-7 shows the possible settings for I/O standards with current strength control. These programmable current strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for I_{OH} and I_{OL} of the corresponding I/O standard.

 When you use programmable current strength, on-chip series termination (R_S OCT) is not available.

Slew Rate Control

The output buffer for each Cyclone IV I/O pin provides optional programmable output slew-rate control. Table 6-2 on page 6-7 shows the possible slew rate option and the Quartus II default slew rate setting. However, these fast transitions may introduce noise transients in the system. A slower slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Because each I/O pin has an individual slew-rate control, you can specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges. Slew rate control is available for single-ended I/O standards with current strength of 8 mA or higher.

 You cannot use the programmable slew rate feature when using OCT with calibration.

 You cannot use the programmable slew rate feature when using the 3.0-V PCI, 3.0-V PCI-X, 3.3-V LVTTTL, or 3.3-V LVCMOS I/O standards. Only the fast slew rate (default) setting is available.

Open-Drain Output

Cyclone IV devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that are asserted by multiple devices in your system.

Bus Hold

Each Cyclone IV device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry holds the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage in which noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals.

 If you enable the bus-hold feature, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus-hold circuitry is not available on dedicated clock pins.

Bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

The CLKIN/REFCLK pins are powered by dedicated $V_{CC_CLKIN3A}$, $V_{CC_CLKIN3B}$, $V_{CC_CLKIN8A}$, and $V_{CC_CLKIN8B}$ power supplies separately in their respective I/O banks to avoid the different power level requirements in the same bank for GPIO.

Table 6-10. Cyclone IV GX HSSI REFCLK I/O Standard Support Using GPIO CLKIN Pins ⁽¹⁾, ⁽²⁾

I/O Standard	HSSI Protocol	Coupling	Termination	VCC_CLKIN Level		I/O Pin Type		
				Input	Output	Column I/O	Row I/O	Supported I/O Banks
LVDS	All	Differential AC (Need off chip resistor to restore V_{CM})	Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B
LVPECL	All		Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B
1.2V, 1.5V, 3.3V PCML	All		Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B
	All		Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B
	All	Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B	
HCSL	PCIe	Differential DC	Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B

Notes to Table 6-10:

- (1) The EP4CGX15, EP4CGX22, and EP4CGX30 devices have two pairs of dedicated clock input pins in banks 3A and 8A for HSSI input reference clock. I/O banks 3B and 8B are not available in EP4CGX15, EP4CGX22, and EP4CGX30 devices.
- (2) The EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have four pairs of dedicated clock input pins in banks 3A, 3B, 8A, and 8B for HSSI input or single-ended clock input.

 For more information about the AC-coupled termination scheme for the HSSI reference clock, refer to the *Cyclone IV Transceivers Architecture* chapter.

LVDS I/O Standard Support in Cyclone IV Devices

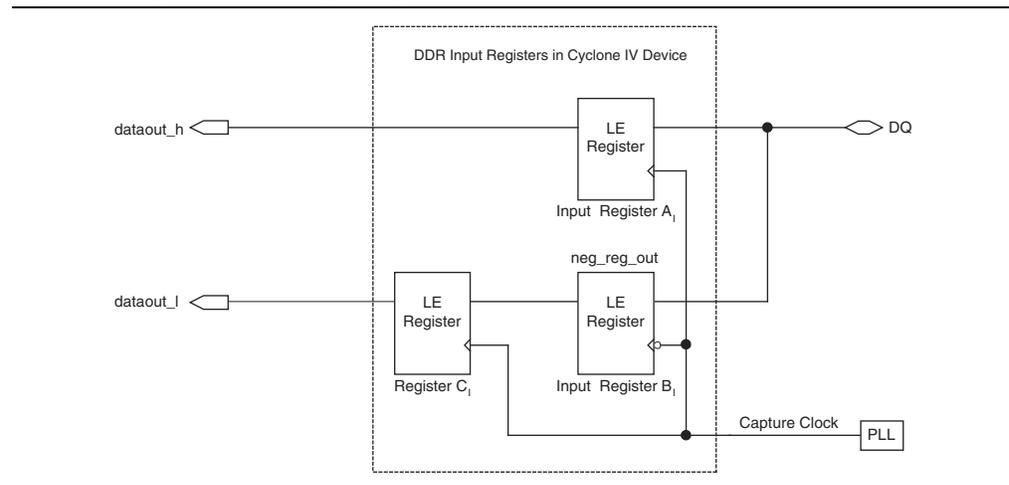
The LVDS I/O standard is a high-speed, low-voltage swing, low power, and GPIO interface standard. Cyclone IV devices meet the ANSI/TIA/EIA-644 standard with the following exceptions:

- The maximum differential output voltage (V_{OD}) is increased to 600 mV. The maximum V_{OD} for ANSI specification is 450 mV.
- The input voltage range is reduced to the range of 1.0 V to 1.6 V, 0.5 V to 1.85 V, or 0 V to 1.8 V based on different frequency ranges. The ANSI/TIA/EIA-644 specification supports an input voltage range of 0 V to 2.4 V.

 For LVDS I/O standard electrical specifications in Cyclone IV devices, refer to the *Cyclone IV Device Datasheet* chapter.

Figure 7-7 illustrates Cyclone IV DDR input registers.

Figure 7-7. Cyclone IV DDR Input Registers



These DDR input registers are implemented in the core of devices. The DDR data is first fed to two registers, input register A₁ and input register B₁.

- Input register A₁ captures the DDR data present during the rising edge of the clock
- Input register B₁ captures the DDR data present during the falling edge of the clock
- Register C₁ aligns the data before it is synchronized with the system clock

The data from the DDR input register is fed to two registers, `sync_reg_h` and `sync_reg_l`, then the data is typically transferred to a FIFO block to synchronize the two data streams to the rising edge of the system clock. Because the read-capture clock is generated by the PLL, the read-data strobe signal (DQS or CQ) is not used during read operation in Cyclone IV devices; hence, postamble is not a concern in this case.

- “FPP Configuration” on page 8–40
- “JTAG Configuration” on page 8–45
- “Device Configuration Pins” on page 8–62

Configuration Features

Table 8–1 lists the configuration methods you can use in each configuration scheme.

Table 8–1. Configuration Features in Cyclone IV Devices

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade ⁽¹⁾
AS	Serial Configuration Device	✓	✓
AP	Supported Flash Memory ⁽²⁾	—	✓
PS	External Host with Flash Memory	✓	✓ ⁽³⁾
	Download Cable	✓	—
FPP	External Host with Flash Memory	—	✓ ⁽³⁾
JTAG based configuration	External Host with Flash Memory	—	—
	Download Cable	—	—

Notes to Table 8–1:

- (1) Remote update mode is supported when you use the Remote System Upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus® II software.
- (2) For more information about the supported device families for the Micron commodity parallel flash, refer to Table 8–10 on page 8–22.
- (3) Remote update mode is supported externally using the Parallel Flash Loader (PFL) with the Quartus II software.

Configuration Data Decompression

Cyclone IV devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and send the compressed bitstream to Cyclone IV devices. During configuration, Cyclone IV devices decompress the bitstream in real time and program the SRAM cells.

 Compression may reduce the configuration bitstream size by 35 to 55%.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time required to send the bitstream to the Cyclone IV device. The time required by a Cyclone IV device to decompress a configuration file is less than the time required to send the configuration data to the device. There are two methods for enabling compression for the Cyclone IV device bitstreams in the Quartus II software:

- Before design compilation (through the Compiler Settings menu)
- After design compilation (through the **Convert Programming Files** dialog box)

To enable compression in the compiler settings of the project in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.
2. Click **Device and Pin Options**. The **Device and Pin Options** dialog box appears.

devices. The internal oscillator is designed to ensure that its maximum frequency is guaranteed to meet EPCS device specifications. Cyclone IV devices offer the option to select `CLKUSR` as the external clock source for `DCLK`. You can change the clock source option in the Quartus II software in the **Configuration** tab of the **Device and Pin Options** dialog box.

 EPCS1 does not support Cyclone IV devices because of its insufficient memory capacity.

Table 8-6. AS DCLK Output Frequency

Oscillator	Minimum	Typical	Maximum	Unit
40 MHz	20	30	40	MHz

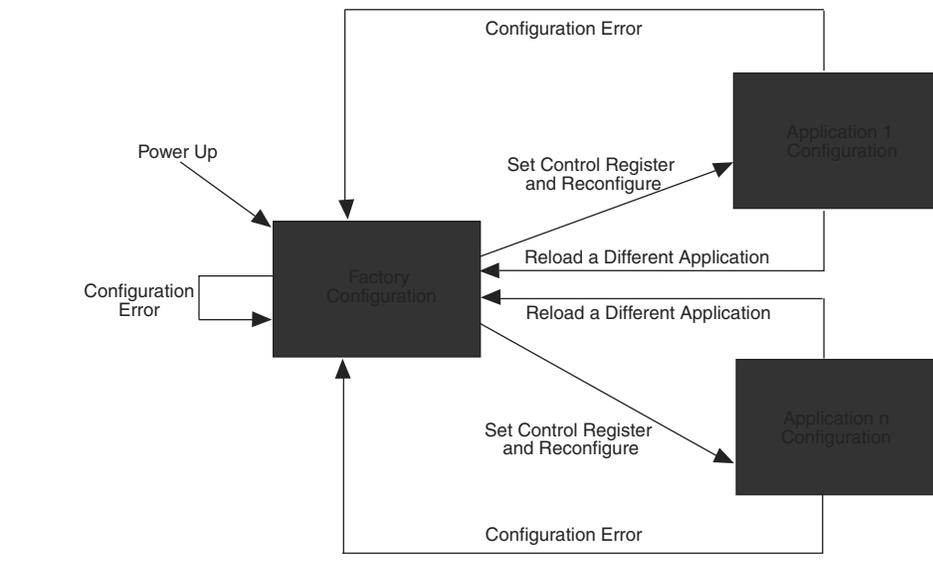
In configuration mode, the Cyclone IV device enables the serial configuration device by driving the `nCS0` output pin low, which connects to the `nCS` pin of the configuration device. The Cyclone IV device uses the `DCLK` and `DATA [1]` pins to send operation commands and read address signals to the serial configuration device. The configuration device provides data on its `DATA` pin, which connects to the `DATA [0]` input of the Cyclone IV device.

All AS configuration pins (`DATA [0]`, `DCLK`, `nCS0`, and `DATA [1]`) have weak internal pull-up resistors that are always active. After configuration, these pins are set as input tri-stated and are driven high by the weak internal pull-up resistors.

The timing parameters for AS mode are not listed here because the t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , t_{CF2ST1} , and t_{CD2UM} timing parameters are identical to the timing parameters for PS mode shown in Table 8-12 on page 8-36.

Figure 8–32 shows the transitions between the factory configuration and application configuration in remote update mode.

Figure 8–32. Transitions Between Configurations in Remote Update Mode



After power up or a configuration error, the factory configuration logic writes the remote system upgrade control register to specify the address of the application configuration to be loaded. The factory configuration also specifies whether or not to enable the user watchdog timer for the application configuration and, if enabled, specifies the timer setting.

 Only valid application configurations designed for remote update mode include the logic to reset the timer in user mode. For more information about the user watchdog timer, refer to the “User Watchdog Timer” on page 8–79.

If there is an error while loading the application configuration, the remote system upgrade status register is written by the dedicated remote system upgrade circuitry of the Cyclone IV device to specify the cause of the reconfiguration.

The following actions cause the remote system upgrade status register to be written:

- nSTATUS driven low externally
- Internal cyclical redundancy check (CRC) error
- User watchdog timer time-out
- A configuration reset (logic array nCONFIG signal or external nCONFIG pin assertion)

The Cyclone IV device automatically loads the factory configuration when an error occurs. This user-designed factory configuration reads the remote system upgrade status register to determine the reason for reconfiguration. Then the factory configuration takes the appropriate error recovery steps and writes to the remote system upgrade control register to determine the next application configuration to be loaded.

10. JTAG Boundary-Scan Testing for Cyclone IV Devices

CYIV-51010-1.3

This chapter describes the boundary-scan test (BST) features that are supported in Cyclone® IV devices. The features are similar to Cyclone III devices, unless stated in this chapter.

Cyclone IV devices (Cyclone IV E devices and Cyclone IV GX devices) support IEEE Std. 1149.1. Cyclone IV GX devices also support IEEE Std. 1149.6. The IEEE Std. 1149.6 (AC JTAG) is only supported on the high-speed serial interface (HSSI) transceivers in Cyclone IV GX devices. The purpose of IEEE Std. 1149.6 is to enable board-level connectivity checking between transmitters and receivers that are AC coupled.

This chapter includes the following sections:

- “IEEE Std. 1149.6 Boundary-Scan Register” on page 10–2
- “BST Operation Control” on page 10–3
- “I/O Voltage Support in a JTAG Chain” on page 10–5
- “Boundary-Scan Description Language Support” on page 10–6

• For more information about the JTAG instructions code with descriptions and IEEE Std. 1149.1 BST guidelines, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone III Devices* chapter.

• For more information about the following topics, refer to *AN 39: IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*:

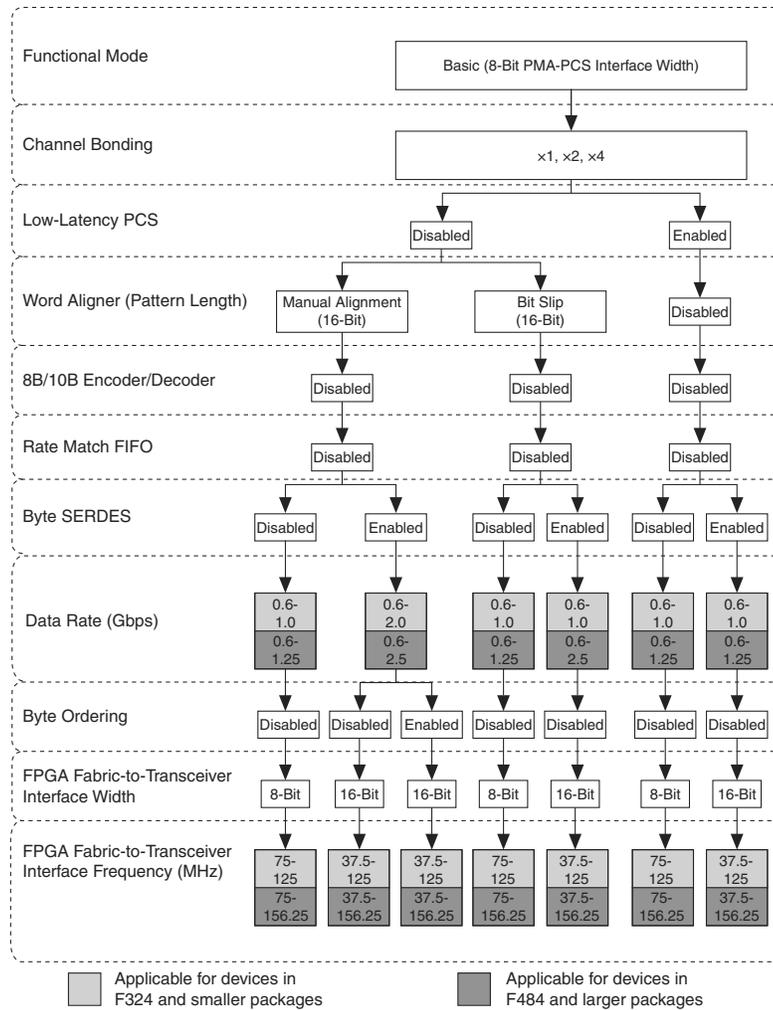
- IEEE Std. 1149.1 BST architecture and circuitry
- TAP controller state-machine
- Instruction mode

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Figure 1-45 and Figure 1-46 show the supported transceiver configurations in Basic mode with the 8-bit and 10-bit PMA-PCS interface width respectively.

Figure 1-45. Supported Transceiver Configurations in Basic Mode with the 8-bit PMA-PCS Interface Width



Transceiver Top-Level Port Lists

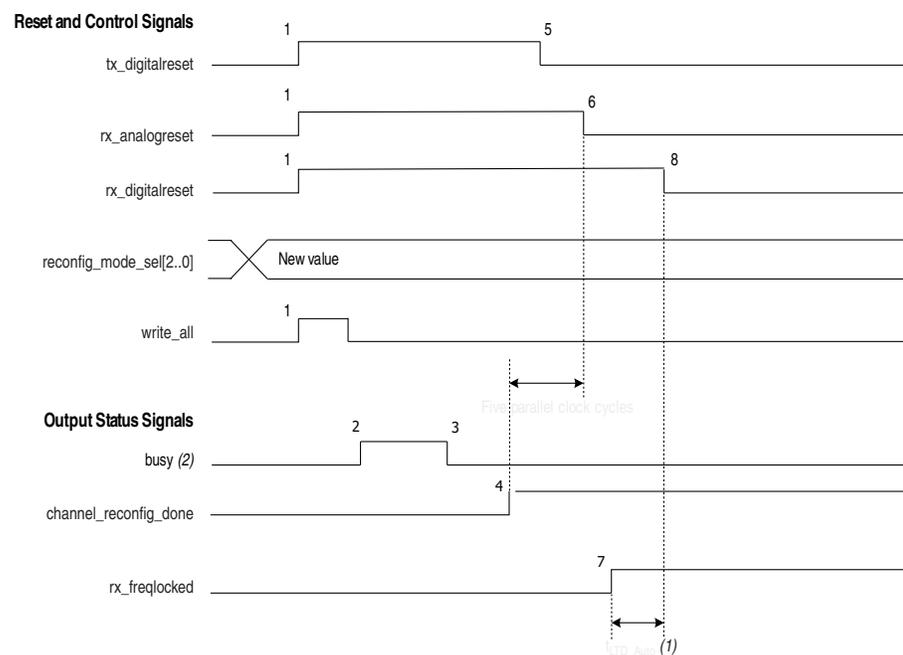
Table 1–26 through Table 1–29 provide descriptions of the ports available when instantiating a transceiver using the ALTGX megafunction. The ALTGX megafunction requires a relatively small number of signals. There are also a large number of optional signals that facilitate debugging by providing information about the state of the transceiver.

2. After the PLL is reset, wait for the `p11_locked` signal to go high (marker 4) indicating that the PLL is locked to the input reference clock. After the assertion of the `p11_locked` signal, deassert the `tx_digitalreset` signal (marker 5).
3. Wait at least five parallel clock cycles after the `p11_locked` signal is asserted to deassert the `rx_analogreset` signal (marker 6).
4. When the `rx_freqlocked` signal goes high (marker 7), from that point onwards, wait for at least t_{LTD_Auto} time, then deassert the `rx_digitalreset` signal (marker 8). At this point, the receiver is ready for data traffic.

Reset Sequence in Channel Reconfiguration Mode

Use the example reset sequence shown in Figure 2-12 when you are using the dynamic reconfiguration controller to change the PCS settings of the transceiver channel. In this example, the dynamic reconfiguration controller is used to dynamically reconfigure the transceiver channel configured in Basic $\times 1$ mode with receiver CDR in automatic lock mode.

Figure 2-12. Reset Sequence When Using the Dynamic Reconfiguration Controller to Change the PCS Settings of the Transceiver Channel



Notes to Figure 2-12:

- (1) For t_{LTD_Auto} duration, refer to the *Cyclone IV Device Datasheet* chapter.
- (2) The `busy` signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the `busy` signal is asserted and deasserted only if there is a read or write operation to the `ALTGX_RECONFIG` megafunction.

PMA Control Ports Used in a Read Transaction

- tx_vodctrl_out is 3 bits per channel
- tx_preemp_out is 5 bits per channel
- rx_eqdcgain_out is 2 bits per channel
- rx_eqctrl_out is 4 bits per channel

For example, assume the number of channels controlled by the dynamic reconfiguration controller is two, tx_vodctrl_out is 6 bits wide.

Write Transaction

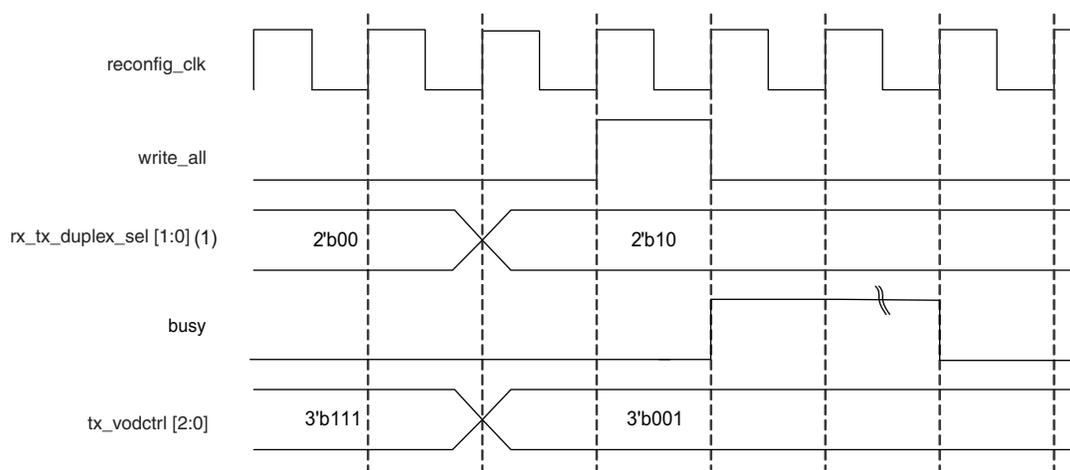
The value you set at the selected PMA control ports is written to all the transceiver channels connected to the ALTGX_RECONFIG instance.

For example, assume you have enabled tx_vodctrl in the ALTGX_RECONFIG MegaWizard Plug-In Manager to reconfigure the V_{OD} of the transceiver channels. To complete a write transaction to reconfigure the V_{OD}, perform the following steps:

1. Before you initiate a write transaction, set the selected PMA control ports to the desired settings (for example, tx_vodctrl = 3'b001).
2. Set the rx_tx_duplex_sel port to 2'b10 so that only the transmit PMA controls are written to the transceiver channel.
3. Ensure that the busy signal is low before you start a write transaction.
4. Assert the write_all signal for one reconfig_clk clock cycle. This initiates the write transaction.
5. The busy output status signal is asserted high to indicate that the dynamic reconfiguration controller is busy writing the PMA control values. When the write transaction has completed, the busy signal goes low.

Figure 3-6 shows the write transaction for Method 2.

Figure 3-6. Write Transaction Waveform—Use the same control signal for all the channels Option



Note to Figure 3-6:

(1) In this waveform example, you want to write to only the transmitter portion of the channel.

Table 3-7 lists the ALTGX megafunction ports for PLL Reconfiguration mode.

Table 3-7. ALTGX Megafunction Port List for PLL Reconfiguration Mode

Port Name ⁽¹⁾	Input/Output	Description	Comments
pll_areset [n..0]	Input	Resets the transceiver PLL. The pll_areset are asserted in two conditions: <ul style="list-style-type: none"> Used to reset the transceiver PLL during the reset sequence. During reset sequence, this signal is user controlled. After the transceiver PLL is reconfigured, this signal is asserted high by the ALTPLL_RECONFIG controller. At this time, this signal is not user controlled. 	You must connect the pll_areset port of ALTGX to the pll_areset port of the ALTPLL_RECONFIG megafunction. The ALTPLL_RECONFIG controller asserts the pll_areset port at the next rising clock edge after the pll_reconfig_done signal from the ALTGX megafunction goes high. After the pll_reconfig_done signal goes high, the transceiver PLL is reset. When the PLL reconfiguration is completed, this reset is performed automatically by the ALTPLL_RECONFIG megafunction and is not user controlled.
pll_scandata [n..0]	Input	Receives the scan data input from the ALTPLL_RECONFIG megafunction.	The reconfigurable transceiver PLL received the scan data input through this port for the dynamically reconfigurable bits from the ALTPLL_RECONFIG controller.
pll_scanclk [n..0]	Input	Drives the scanclk port on the reconfigurable transceiver PLL.	Connect the pll_scanclk port of the ALTGX megafunction to the ALTPLL_RECONFIG scanclk port.
pll_scanckena [n..0]	Input	Acts as a clock enable for the scanclk port on the reconfigurable transceiver PLL.	Connect the pll_scanckena port of the ALTGX megafunction to the ALTPLL_RECONFIG scanclk port.
pll_configupdate [n..0]	Input	Drives the configupdate port on the reconfigurable transceiver PLL.	This port is connected to the pll_configupdate port from the ALTPLL_RECONFIG controller. After the final data bit is sent out, the ALTPLL_RECONFIG controller asserts this signal.
pll_reconfig_done[n..0]	Output	This signal is asserted to indicate the reconfiguration process is done.	Connect the pll_reconfig_done port to the pll_scandone port on the ALTPLL_RECONFIG controller. The transceiver PLL scandone output signal drives this port and determines when the PLL is reconfigured.
pll_scandataout [n..0]	Output	This port scan out the current configuration of the transceiver PLL.	Connect the pll_scandataout port to the pll_scandataout port of the ALTPLL_RECONFIG controller. This port reads the current configuration of the transceiver PLL and send it to the ALTPLL_RECONFIG megafunction.

Note to Table 3-7:

(1) <n> = (number of transceiver PLLs configured in the ALTGX MegaWizard) - 1.

 For more information about the ALTPLL_RECONFIG megafunction port list, description and usage, refer to the *Phase-Locked Loop Reconfiguration (ALTPLL_RECONFIG) Megafunction User Guide*.

Section I. Device Datasheet

This section provides the Cyclone[®] IV device datasheet. It includes the following chapter:

- Chapter 1, Cyclone IV Device Datasheet

Revision History

Refer to each chapter for its own specific revision history. For information about when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Example 1-1 shows how to calculate the change of 50-Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Example 1-1. Impedance Change

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$

$$\Delta R_T = (85 - 25) \times 0.262 = 15.72$$

Because ΔR_V is negative,

$$MF_V = 1 / (3.83/100 + 1) = 0.963$$

Because ΔR_T is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{\text{final}} = 50 \times 1.114 = 55.71 \Omega$$

Pin Capacitance

Table 1-11 lists the pin capacitance for Cyclone IV devices.

Table 1-11. Pin Capacitance for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Quad Flat No Leads (QFN)	Typical – Ball-Grid Array (BGA)	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	7	7	6	pF
C_{IOLR}	Input capacitance on right I/O pins	7	7	5	pF
$C_{LVDSLRL}$	Input capacitance on right I/O pins with dedicated LVDS output	8	8	7	pF
C_{VREFLR} (2)	Input capacitance on right dual-purpose V_{REF} pin when used as V_{REF} or user I/O pin	21	21	21	pF
C_{VREFTB} (2)	Input capacitance on top and bottom dual-purpose V_{REF} pin when used as V_{REF} or user I/O pin	23 (3)	23	23	pF
C_{CLKTB}	Input capacitance on top and bottom dedicated clock input pins	7	7	6	pF
C_{CLKLR}	Input capacitance on right dedicated clock input pins	6	6	5	pF

Notes to Table 1-11:

- (1) The pin capacitance applies to FBGA, UBGA, and MBGA packages.
- (2) When you use the V_{REF} pin as a regular input or output, you can expect a reduced performance of toggle rate and t_{CO} because of higher pin capacitance.
- (3) C_{VREFTB} for the EP4CE22 device is 30 pF.