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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1395
Number of Logic Elements/Cells	22320
Total RAM Bits	608256
Number of I/O	153
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce22f17c9l

Visual Cue	Meaning
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, <code>data1</code> , <code>tdi</code> , and <code>input</code> . The suffix <code>n</code> denotes an active-low signal. For example, <code>resetn</code> . Indicates command line commands and anything that must be typed exactly as it appears. For example, <code>c:\qdesigns\tutorial\chiptrip.gdf</code> . Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <code>SUBDESIGN</code>), and logic function names (for example, <code>TRI</code>).
	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.

3. Memory Blocks in Cyclone IV Devices

CYIV-51003-1.1

Cyclone® IV devices feature embedded memory structures to address the on-chip memory needs of Altera® Cyclone IV device designs. The embedded memory structure consists of columns of M9K memory blocks that you can configure to provide various memory functions, such as RAM, shift registers, ROM, and FIFO buffers.

This chapter contains the following sections:

- “Memory Modes” on page 3–7
- “Clocking Modes” on page 3–14
- “Design Considerations” on page 3–15

Overview

M9K blocks support the following features:

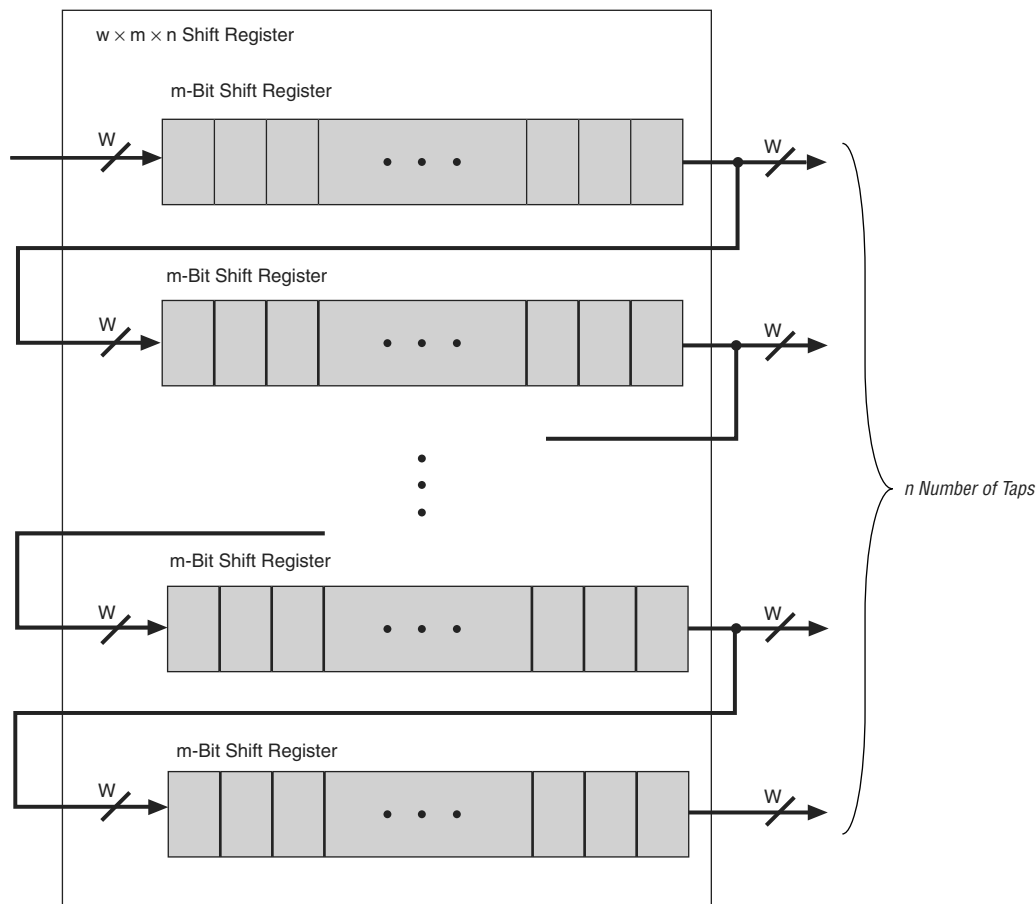
- 8,192 memory bits per block (9,216 bits per block including parity)
- Independent read-enable (*rden*) and write-enable (*wren*) signals for each port
- Packed mode in which the M9K memory block is split into two 4.5 K single-port RAMs
- Variable port configurations
- Single-port and simple dual-port modes support for all port widths
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Two clock-enable control signals for each port (port A and port B)
- Initialization file to pre-load memory content in RAM and ROM modes

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Figure 3-12 shows the Cyclone IV devices M9K memory block in shift register mode.

Figure 3-12. Cyclone IV Devices Shift Register Mode Configuration



ROM Mode

Cyclone IV devices M9K memory blocks support ROM mode. A `.mif` initializes the ROM contents of these blocks. The address lines of the ROM are registered. The outputs can be registered or unregistered. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Buffer Mode

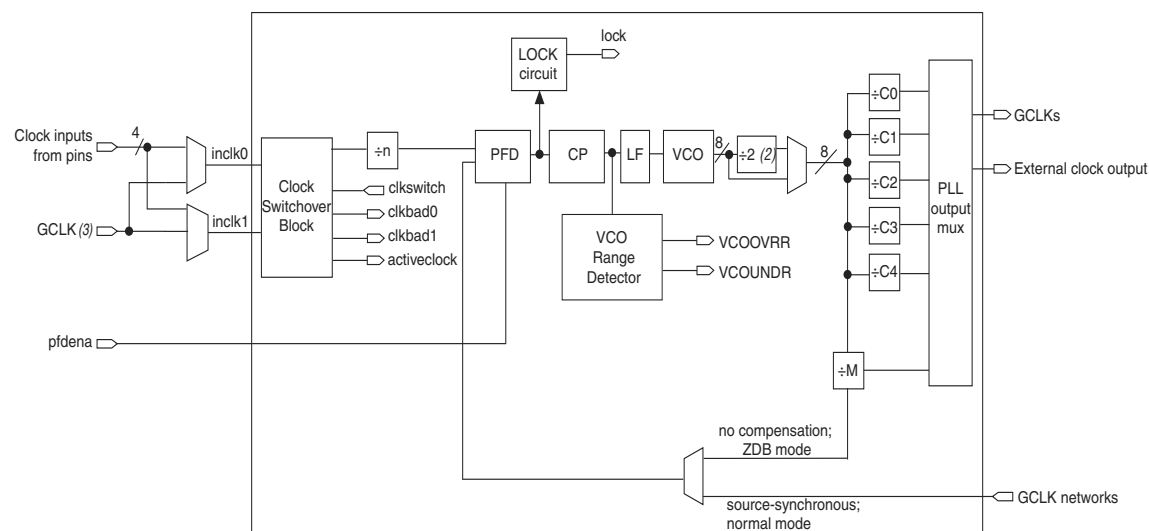
Cyclone IV devices M9K memory blocks support single-clock or dual-clock FIFO buffers. Dual clock FIFO buffers are useful when transferring data from one clock domain to another clock domain. Cyclone IV devices M9K memory blocks do not support simultaneous read and write from an empty FIFO buffer.



For more information about FIFO buffers, refer to the *Single- and Dual-Clock FIFO Megafunction User Guide*.


Figure 5–10 shows a simplified block diagram of the major components of the PLL of Cyclone IV E devices.

Figure 5–10. Cyclone IV E PLL Block Diagram ⁽¹⁾



Notes to Figure 5–10:

- (1) Each clock source can come from any of the four clock pins located on the same side of the device as the PLL.
- (2) This is the VCO post-scale counter K.
- (3) This input port is fed by a pin-driven dedicated GCLK, or through a clock control block if the clock control block is fed by an output from another PLL or a pin-driven dedicated GCLK. An internally generated global signal cannot drive the PLL.

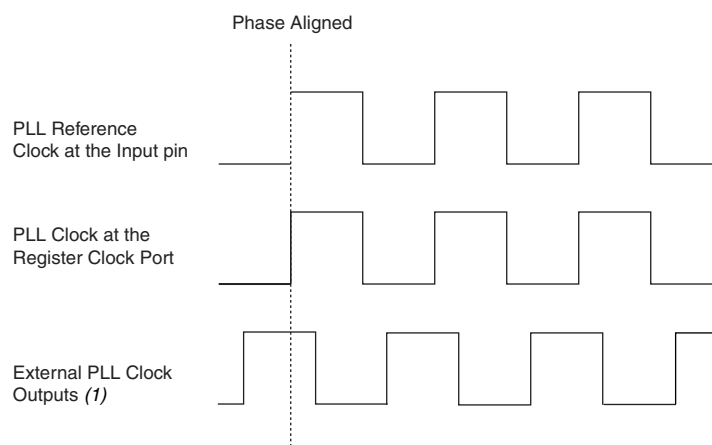
 The VCO post-scale counter K is used to divide the supported VCO range by two. The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter value. Therefore, if the VCO post-scale counter has a value of 2, the frequency reported is lower than the f_{VCO} specification specified in the *Cyclone IV Device Datasheet* chapter.

External Clock Outputs

Each PLL of Cyclone IV devices supports one single-ended clock output or one differential clock output. Only the C0 output counter can feed the dedicated external clock outputs, as shown in Figure 5–11, without going through the GCLK. Other output counters can feed other I/O pins through the GCLK.

Figure 5-14 shows a waveform example of the phase relationship of the PLL clocks in this mode.

Figure 5-14. Phase Relationship Between PLL Clocks in Normal Mode



Note to Figure 5-14:

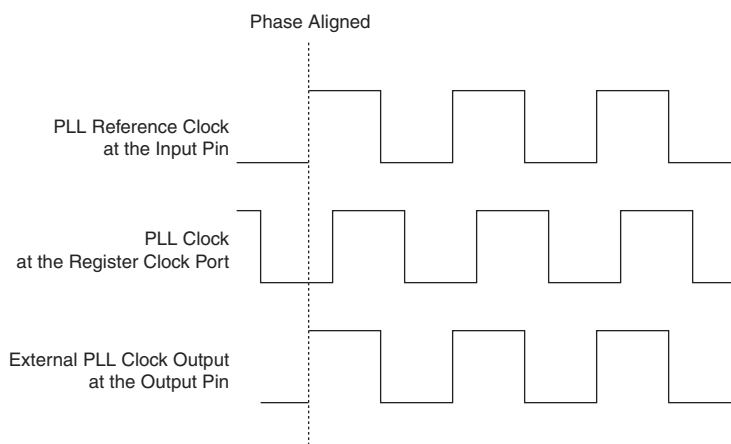
(1) The external clock output can lead or lag the PLL internal clock signals.

Zero Delay Buffer Mode

In zero delay buffer (ZDB) mode, the external clock output pin is phase-aligned with the clock input pin for zero delay through the device. When using this mode, use the same I/O standard on the input clock and output clocks to guarantee clock alignment at the input and output pins.

Figure 5-15 shows an example waveform of the phase relationship of the PLL clocks in ZDB mode.

Figure 5-15. Phase Relationship Between PLL Clocks in ZDB Mode



PLL Reconfiguration

PLLs use several divide counters and different VCO phase taps to perform frequency synthesis and phase shifts. In PLLs of Cyclone IV devices, you can reconfigure both counter settings and phase shift the PLL output clock in real time. You can also change the charge pump and loop filter components, which dynamically affects PLL bandwidth. You can use these PLL components to update the output clock frequency, PLL bandwidth, and phase shift in real time, without reconfiguring the entire FPGA.

The ability to reconfigure the PLL in real time is useful in applications that might operate at multiple frequencies. It is also useful in prototyping environments, allowing you to sweep PLL output frequencies and adjust the output clock phase dynamically. For instance, a system generating test patterns is required to generate and send patterns at 75 or 150 MHz, depending on the requirements of the device under test. Reconfiguring PLL components in real time allows you to switch between two such output frequencies in a few microseconds.

You can also use this feature to adjust clock-to-out (t_{CO}) delays in real time by changing the PLL output clock phase shift. This approach eliminates the need to regenerate a configuration file with the new PLL settings.

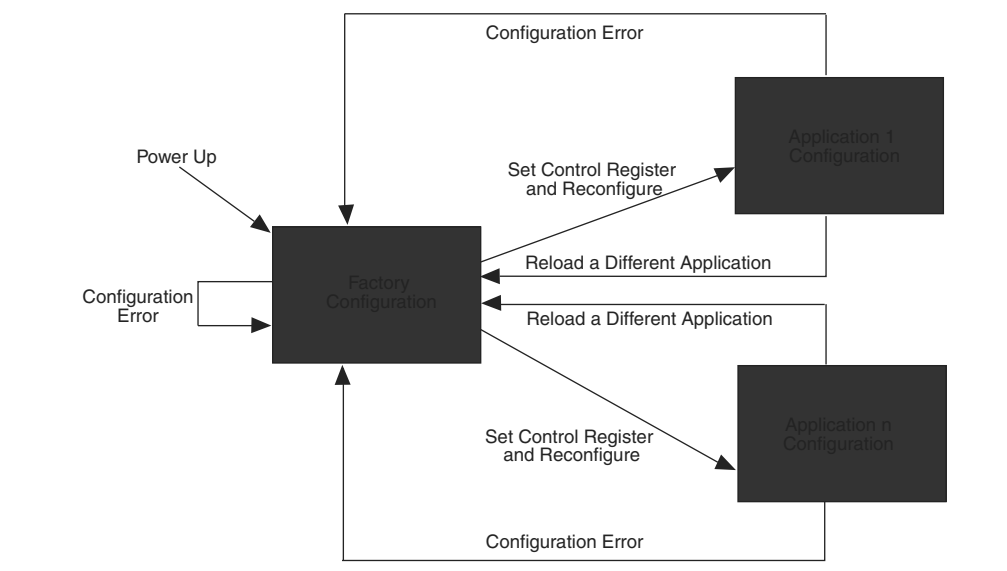
PLL Reconfiguration Hardware Implementation

The following PLL components are configurable in real time:

- Pre-scale counter (N)
- Feedback counter (M)
- Post-scale output counters (C0–C4)
- Dynamically adjust the charge pump current (I_{CP}) and loop filter components (R, C) to facilitate on-the-fly reconfiguration of the PLL bandwidth

Figure 8-32 shows the transitions between the factory configuration and application configuration in remote update mode.

Figure 8-32. Transitions Between Configurations in Remote Update Mode



After power up or a configuration error, the factory configuration logic writes the remote system upgrade control register to specify the address of the application configuration to be loaded. The factory configuration also specifies whether or not to enable the user watchdog timer for the application configuration and, if enabled, specifies the timer setting.



Only valid application configurations designed for remote update mode include the logic to reset the timer in user mode. For more information about the user watchdog timer, refer to the “User Watchdog Timer” on page 8-79.

If there is an error while loading the application configuration, the remote system upgrade status register is written by the dedicated remote system upgrade circuitry of the Cyclone IV device to specify the cause of the reconfiguration.

The following actions cause the remote system upgrade status register to be written:

- `nSTATUS` driven low externally
- Internal cyclical redundancy check (CRC) error
- User watchdog timer time-out
- A configuration reset (logic array `nCONFIG` signal or external `nCONFIG` pin assertion)

The Cyclone IV device automatically loads the factory configuration when an error occurs. This user-designed factory configuration reads the remote system upgrade status register to determine the reason for reconfiguration. Then the factory configuration takes the appropriate error recovery steps and writes to the remote system upgrade control register to determine the next application configuration to be loaded.

The byte ordering block operates in either word-alignment-based byte ordering or user-controlled byte ordering modes.

In word-alignment-based byte ordering mode, the byte ordering block starts looking for the byte ordering pattern in the byte-deserialized data and restores the order if necessary when it detects a rising edge on the rx_syncstatus signal. Whenever the byte ordering pattern is found, the rx_byteorderalignstatus signal is asserted regardless if the pad byte insertion is necessary. If the byte ordering block detects another rising edge on the rx_syncstatus signal from the word aligner, it deasserts the rx_byteorderalignstatus signal and repeats the byte ordering operation.

In user-controlled byte ordering mode, the byte ordering operation is user-triggered using rx_enabyteord port. A rising edge on rx_enabyteord port triggers the byte ordering block to start looking for the byte ordering pattern in the byte-deserialized data and restores the order if necessary. When the byte ordering pattern is found, the rx_byteorderalignstatus signal is asserted regardless if a pad byte insertion is necessary.

RX Phase Compensation FIFO

The RX phase compensation FIFO compensates for the phase difference between the parallel receiver clock and the FPGA fabric interface clock, when interfacing the receiver channel to the FPGA fabric (directly or through the PIPE and PCIe hard IP blocks). The FIFO is four words deep, with latency between two to three parallel clock cycles.

Figure 1-24 shows the RX phase compensation FIFO block diagram.

Figure 1-24. RX Phase Compensation FIFO Block Diagram



Note to Figure 1-24:

(1) Parameter x refers to the transceiver channel width, where 8, 10, 16, or 20 bits are supported.




The FIFO can operate in registered mode, contributing to only one parallel clock cycle of latency in the Deterministic Latency functional mode. For more information, refer to “Deterministic Latency Mode” on page 1-73. For more information about FIFO clocking, refer to “FPGA Fabric-Transceiver Interface Clocking” on page 1-43.

Miscellaneous Receiver PCS Feature

The receiver PCS supports the following additional feature:

- **Output bit-flip**—reverses the bit order at a byte level at the output of the receiver phase compensation FIFO. For example, if the 16-bit parallel receiver data at the output of the receiver phase compensation FIFO is '10111100 10101101' (16'hBCAD), enabling this option reverses the data on rx_dataout port to '00111101 10110101' (16'h3DB5).

 In any configuration, a receiver channel cannot source CDR clocks from other PLLs beyond the two multipurpose PLLs directly adjacent to transceiver block where the channel resides.


The Cyclone IV GX transceivers support non-bonded ($\times 1$) and bonded ($\times 2$ and $\times 4$) channel configurations. The two configurations differ in regards to clocking and phase compensation FIFO control. Bonded configuration provides a relatively lower channel-to-channel skew between the bonded channels than in non-bonded configuration. Table 1-8 lists the supported conditions in non-bonded and bonded channel configurations.

Table 1-8. Supported Conditions in Non-Bonded and Bonded Channel Configurations

Channel Configuration	Description	Supported Channel Operation Mode
Non-bonded ($\times 1$)	<ul style="list-style-type: none"> Low-speed clock in each channel is sourced independently Phase compensation FIFO in each channel has its own pointers and control logic 	<ul style="list-style-type: none"> Transmitter Only Receiver Only Transmitter and Receiver
Bonded ($\times 2$ and $\times 4$)	<ul style="list-style-type: none"> Low-speed clock in each bonded channel is sourced from a common bonded clock path for lower channel-to-channel skew Phase compensation FIFOs in bonded channels share common pointers and control logic for equal latency through the FIFOs in all bonded channels $\times 2$ bonded configuration is supported with channel 0 and channel 1 in a transceiver block $\times 4$ bonded configuration is supported with all four channels in a transceiver block 	<ul style="list-style-type: none"> Transmitter Only Transmitter and Receiver

Non-Bonded Channel Configuration

In non-bonded channel configuration, the high- and low-speed clocks for each channel are sourced independently. The phase compensation FIFOs in each channel has its own pointers and control logic. When implementing multi-channel serial interface in non-bonded channel configuration, the clock skew and unequal latency results in larger channel-to-channel skew.


 Altera recommends using bonded channel configuration ($\times 2$ or $\times 4$) when implementing multi-channel serial interface for a lower channel-to-channel skew.


In a transceiver block, the high- and low-speed clocks for each channel are distributed primarily from one of the two multipurpose PLLs directly adjacent to the block. Transceiver channels for devices in F484 and larger packages support additional clocking flexibility. In these packages, some channels support high-speed and low-speed clock distribution from PLLs beyond the two multipurpose PLLs directly adjacent to the block.

Table 2–2 lists the power-down signals available for each transceiver block.

Table 2–2. Transceiver Block Power-Down Signals

Signal	Description
pll_areset	Resets the transceiver PLL. The pll_areset signal is asserted in two conditions: <ul style="list-style-type: none"> ■ During reset sequence, the signal is asserted to reset the transceiver PLL. This signal is controlled by the user. ■ After the transceiver PLL is reconfigured, the signal is asserted high by the ALTPLL_RECONFIG controller. This signal is not controlled by the user.
gxb_powerdown	Powers down the entire transceiver block. When this signal is asserted, this signal powers down the PCS and PMA in all the transceiver channels. This signal operates independently from the other reset signals. This signal is common to the transceiver block.
pll_locked	A status signal. Indicates the status of the transmitter multipurpose PLLs or general purpose PLLs. <ul style="list-style-type: none"> ■ A high level—indicates the multipurpose PLL or general purpose PLL is locked to the incoming reference clock frequency.
rx_freqlocked	A status signal. Indicates the status of the receiver CDR lock mode. <ul style="list-style-type: none"> ■ A high level—the receiver is in lock-to-data mode. ■ A low level—the receiver CDR is in lock-to-reference mode.
busy	A status signal. An output from the ALTGX_RECONFIG block indicates the status of the dynamic reconfiguration controller. This signal remains low for the first reconfig_clk clock cycle after power up. It then gets asserted from the second reconfig_clk clock cycle. Assertion on this signal indicates that the offset cancellation process is being executed on the receiver buffer as well as the receiver CDR. When this signal is deasserted, it indicates that offset cancellation is complete. This busy signal is also used to indicate the dynamic reconfiguration duration such as in analog reconfiguration mode and channel reconfiguration mode.

 For more information about offset cancellation, refer to the *Cyclone IV Dynamic Reconfiguration* chapter.

 If none of the channels is instantiated in a transceiver block, the Quartus® II software automatically powers down the entire transceiver block.

Blocks Affected by the Reset and Power-Down Signals

Table 2–3 lists the blocks that are affected by specific reset and power-down signals.

Table 2–3. Blocks Affected by Reset and Power-Down Signals (Part 1 of 2)

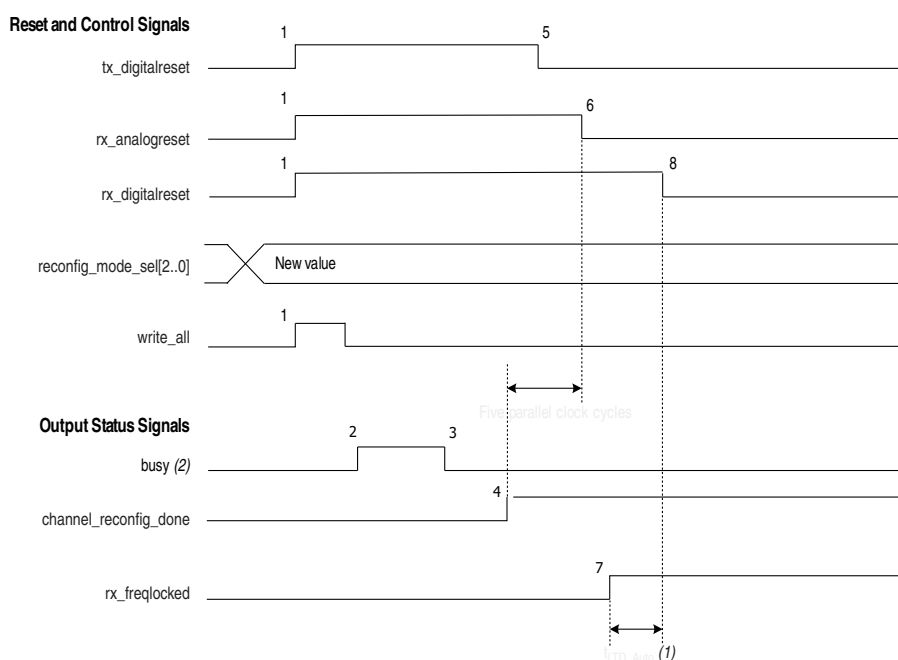
Transceiver Block	rx_digitalreset	rx_analogreset	tx_digitalreset	pll_areset	gxb_powerdown
multipurpose PLLs and general purpose PLLs	—	—	—	✓	—
Transmitter Phase Compensation FIFO	—	—	✓	—	✓
Byte Serializer	—	—	✓	—	✓
8B/10B Encoder	—	—	✓	—	✓

- After the PLL is reset, wait for the `p11_locked` signal to go high (marker 4) indicating that the PLL is locked to the input reference clock. After the assertion of the `p11_locked` signal, deassert the `tx_digitalreset` signal (marker 5).
- Wait at least five parallel clock cycles after the `p11_locked` signal is asserted to deassert the `rx_analogreset` signal (marker 6).
- When the `rx_freqlocked` signal goes high (marker 7), from that point onwards, wait for at least t_{LTD_Auto} time, then deassert the `rx_digitalreset` signal (marker 8). At this point, the receiver is ready for data traffic.

Reset Sequence in Channel Reconfiguration Mode

Use the example reset sequence shown in Figure 2-12 when you are using the dynamic reconfiguration controller to change the PCS settings of the transceiver channel. In this example, the dynamic reconfiguration is used to dynamically reconfigure the transceiver channel configured in Basic $\times 1$ mode with receiver CDR in automatic lock mode.

Figure 2-12. Reset Sequence When Using the Dynamic Reconfiguration Controller to Change the PCS Settings of the Transceiver Channel



Notes to Figure 2-12:

- (1) For t_{LTD_Auto} duration, refer to the *Cyclone IV Device Datasheet* chapter.
- (2) The `busy` signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the `busy` signal is asserted and deasserted only if there is a read or write operation to the `ALTGX_RECONFIG` megafunction.

Document Revision History

Table 2–8 lists the revision history for this chapter.

Table 2–8. Document Revision History

Date	Version	Changes
September 2014	1.4	<ul style="list-style-type: none"> Removed the <code>rx_pll_locked</code> signal from the “Sample Reset Sequence of Receiver Only Channel—Receiver CDR in Manual Lock Mode” and the “Sample Reset Sequence of Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode” figures.
May 2013	1.3	<ul style="list-style-type: none"> Added <code>rx_pll_locked</code> to Figure 2–7 and Figure 2–9. Added information on <code>rx_pll_locked</code> to “Receiver Only Channel—Receiver CDR in Manual Lock Mode” and “Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode”.
November 2011	1.2	Updated the “All Supported Functional Modes Except the PCIe Functional Mode” section.
December 2010	1.1	<ul style="list-style-type: none"> Updated for the Quartus II software version 10.1 release. Updated all <code>pll_powerdown</code> to <code>pll_areset</code>. Added information about the <code>busy</code> signal in Figure 2–4, Figure 2–5, Figure 2–6, Figure 2–7, Figure 2–8, Figure 2–9, Figure 2–10, Figure 2–12, and Figure 2–13. Added information for clarity (“Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode”, “Receiver Only Channel—Receiver CDR in Automatic Lock Mode”, “Receiver Only Channel—Receiver CDR in Manual Lock Mode”, “Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode”, and “Reset Sequence in Channel Reconfiguration Mode”). Minor text edits.
July 2010	1.0	Initial release.

The following are the channel reconfiguration mode options:

- Channel interface reconfiguration
- Data rate division at receiver channel

Channel Interface Reconfiguration Mode

Enable this option if the reconfiguration of the transceiver channel involves the following changes:

- The reconfigured channel has a changed FPGA fabric-Transceiver channel interface data width
- The reconfigured channel has changed input control signals and output status signals
- The reconfigured channel has enabled and disabled the static PCS blocks of the transceiver channel

The following are the new input signals available when you enable this option:

- `tx_dataainfull`—the width of this input signal depends on the number of channels you set up in the ALTGX MegaWizard Plug-In Manager. It is 22 bits wide per channel. This signal is available only for **Transmitter only** and **Receiver and Transmitter** configurations. This port replaces the existing `tx_dataain` port.
- `rx_dataoutfull`—the width of this output signal depends on the number of channels you set up in the ALTGX MegaWizard Plug-In Manager. It is 32 bits wide per channel. This signal is available only for **Receiver only** and **Receiver and Transmitter** configurations. This port replaces the existing `rx_dataout` port.

The Quartus II software has legality checks for the connectivity of `tx_dataainfull` and `rx_dataoutfull` and the various control and status signals you enable in the **Clocking/Interface** screen. For example, the Quartus II software allows you to select and connect the `pipestatus` and `powerdn` signals. It assumes that you are planning to switch to and from PCI Express (PIPE) functional mode.

Chapter Revision Dates

The chapters in this document, Cyclone IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Cyclone IV Device Datasheet
Revised: *December 2016*
Part Number: *CYIV-53001-2.1*

This chapter provides additional information about the document and Altera.

About this Handbook

This handbook provides comprehensive information about the Altera® Cyclone® IV family of devices.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact ⁽¹⁾	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general) (software licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, \qdesigns directory, D: drive, and chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Indicate document titles. For example, <i>Stratix IV Design Guidelines</i> .
<i>italic type</i>	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>.pof file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."


 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
V_i	AC Input Voltage	$V_i = 4.20$	100	%
		$V_i = 4.25$	98	%
		$V_i = 4.30$	65	%
		$V_i = 4.35$	43	%
		$V_i = 4.40$	29	%
		$V_i = 4.45$	20	%
		$V_i = 4.50$	13	%
		$V_i = 4.55$	9	%
		$V_i = 4.60$	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as $([\Delta T]/T) \times 100$. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1–1. Cyclone IV Devices Overshoot Duration

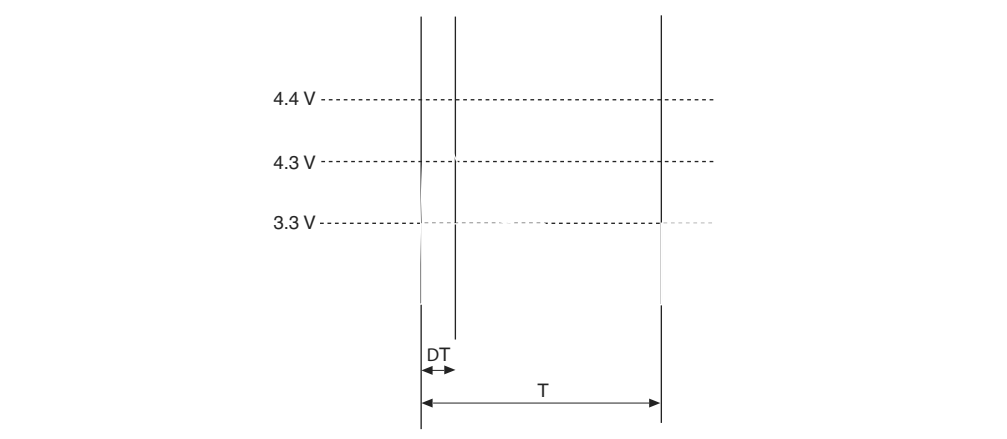


Table 1-16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices ⁽¹⁾

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V) ⁽²⁾		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 x V _{CCIO} ⁽³⁾	0.5 x V _{CCIO} ⁽³⁾	0.52 x V _{CCIO} ⁽³⁾	—	0.5 x V _{CCIO}	—
				0.47 x V _{CCIO} ⁽⁴⁾	0.5 x V _{CCIO} ⁽⁴⁾	0.53 x V _{CCIO} ⁽⁴⁾			

Notes to Table 1-16:

- (1) For an explanation of terms used in Table 1-16, refer to “Glossary” on page 1-37.
- (2) V_{TT} of the transmitting device must track V_{REF} of the receiving device.
- (3) Value shown refers to DC input reference voltage, V_{REF(DC)}.
- (4) Value shown refers to AC input reference voltage, V_{REF(AC)}.

Table 1-17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices

I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)		V _{IH(AC)} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V _{REF} - 0.18	V _{REF} + 0.18	—	—	V _{REF} - 0.35	V _{REF} + 0.35	—	V _{TT} - 0.57	V _{TT} + 0.57	8.1	-8.1
SSTL-2 Class II	—	V _{REF} - 0.18	V _{REF} + 0.18	—	—	V _{REF} - 0.35	V _{REF} + 0.35	—	V _{TT} - 0.76	V _{TT} + 0.76	16.4	-16.4
SSTL-18 Class I	—	V _{REF} - 0.125	V _{REF} + 0.125	—	—	V _{REF} - 0.25	V _{REF} + 0.25	—	V _{TT} - 0.475	V _{TT} + 0.475	6.7	-6.7
SSTL-18 Class II	—	V _{REF} - 0.125	V _{REF} + 0.125	—	—	V _{REF} - 0.25	V _{REF} + 0.25	—	0.28	V _{CCIO} - 0.28	13.4	-13.4
HSTL-18 Class I	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	8	-8
HSTL-18 Class II	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	16	-16
HSTL-15 Class I	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	8	-8
HSTL-15 Class II	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 x V _{CCIO}	0.75 x V _{CCIO}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 x V _{CCIO}	0.75 x V _{CCIO}	14	-14

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PLD-Transceiver Interface											
Interface speed (F324 and smaller package)	—	25	—	125	25	—	125	25	—	125	MHz
Interface speed (F484 and larger package)	—	25	—	156.25	25	—	156.25	25	—	156.25	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles									

Notes to Table 1–21:

- (1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.
- (2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The rate matcher supports only up to ± 300 parts per million (ppm).
- (5) Supported for the F169 and F324 device packages only.
- (6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.
- (7) To support CDR ppm tolerance greater than ± 300 ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.
- (8) Asynchronous spread-spectrum clocking is not supported.
- (9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is ± 200 ppm.
- (10) Time taken until `p1l_locked` goes high after `p1l_powerdown` deasserts.
- (11) Time that the CDR must be kept in lock-to-reference mode after `rx_analogreset` deasserts and before `rx_locktodata` is asserted in manual mode.
- (12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode (Figure 1–2), or after `rx_freqlocked` signal goes high in automatic mode (Figure 1–3).
- (13) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode.
- (14) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode.
- (15) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–25. PLL Specifications for Cyclone IV Devices ^{(1), (2)} (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or \overline{areset} is deasserted)	—	—	1	ms
$t_{OUTJITTER_PERIOD_DEDCLK}$ ⁽⁶⁾	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_CCJ_DEDCLK}$ ⁽⁶⁾	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_PERIOD_IO}$ ⁽⁶⁾	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER_CCJ_IO}$ ⁽⁶⁾	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	± 50	ps
t_{ARESET}	Minimum pulse width on \overline{areset} signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 ⁽⁷⁾	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
$t_{CASC_OUTJITTER_PERIOD_DEDCLK}$ ^{(8), (9)}	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	425	ps
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	42.5	mUI

Notes to Table 1–25:

- (1) This table is applicable for general purpose PLLs and multipurpose PLLs.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through the decoupling capacitor and ferrite bead.
- (3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (4) The V_{CO} frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the V_{CO} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.
- (7) With 100-MHz scanclk frequency.
- (8) The cascaded PLLs specification is applicable only with the following conditions:
 - Upstream PLL— $0.59 \text{ MHz} \leq \text{Upstream PLL bandwidth} < 1 \text{ MHz}$
 - Downstream PLL—Downstream PLL bandwidth $> 2 \text{ MHz}$
- (9) PLL cascading is not supported for transceiver applications.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	1.209	2.184	2.336	2.451	2.387	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.208	2.200	2.399	2.554	2.446	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.438	0.404	0.751	0.825	0.886	0.839	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.713	0.682	1.228	1.41	1.566	1.424	ns

Notes to Table 1–44:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.210	2.209	2.398	2.526	2.443	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.313	1.208	2.205	2.406	2.563	2.450	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.461	0.421	0.789	0.869	0.933	0.884	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.712	0.682	1.225	1.407	1.562	1.421	ns

Notes to Table 1–45:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software