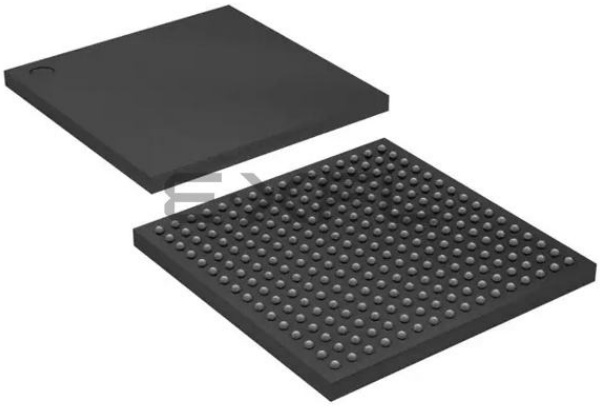

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1395
Number of Logic Elements/Cells	22320
Total RAM Bits	608256
Number of I/O	153
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce22f17c9ln

Figure 3–3 and Figure 3–4 show the address clock enable waveform during read and write cycles, respectively.

Figure 3–3. Cyclone IV Devices Address Clock Enable During Read Cycle Waveform

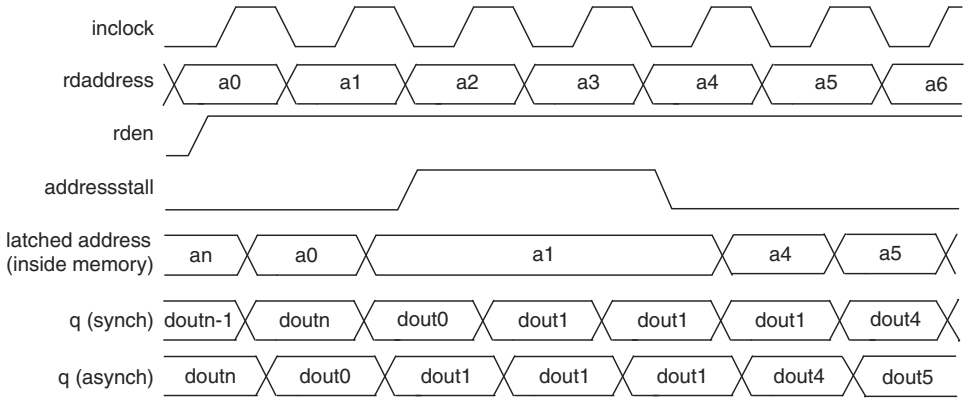
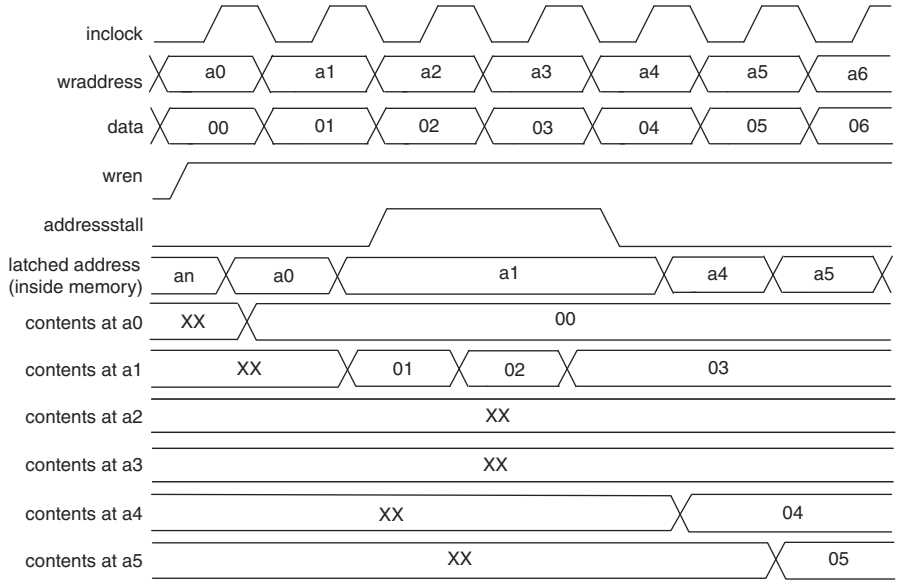


Figure 3–4. Cyclone IV Devices Address Clock Enable During Write Cycle Waveform



Mixed-Width Support

M9K memory blocks support mixed data widths. When using simple dual-port, true dual-port, or FIFO modes, mixed width support allows you to read and write different data widths to an M9K memory block. For more information about the different widths supported per memory mode, refer to "Memory Modes" on page 3–7.

Table 3–3. Cyclone IV Devices M9K Block Mixed-Width Configurations (Simple Dual-Port Mode) *(Part 2 of 2)*

Read Port	Write Port								
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	256 × 32	1024 × 9	512 × 18	256 × 36
512 × 16	✓	✓	✓	✓	✓	✓	—	—	—
256 × 32	✓	✓	✓	✓	✓	✓	—	—	—
1024 × 9	—	—	—	—	—	—	✓	✓	✓
512 × 18	—	—	—	—	—	—	✓	✓	✓
256 × 36	—	—	—	—	—	—	✓	✓	✓

In simple dual-port mode, M9K memory blocks support separate `wren` and `rden` signals. You can save power by keeping the `rden` signal low (inactive) when not reading. Read-during-write operations to the same address can either output "Don't Care" data at that location or output "Old Data". To choose the desired behavior, set the **Read-During-Write** option to either **Don't Care** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about this behavior, refer to "Read-During-Write Operations" on page 3–15.

Figure 3–9 shows the timing waveform for read and write operations in simple dual-port mode with unregistered outputs. Registering the outputs of the RAM simply delays the `q` output by one clock cycle.

Figure 3–9. Cyclone IV Devices Simple Dual-Port Timing Waveform

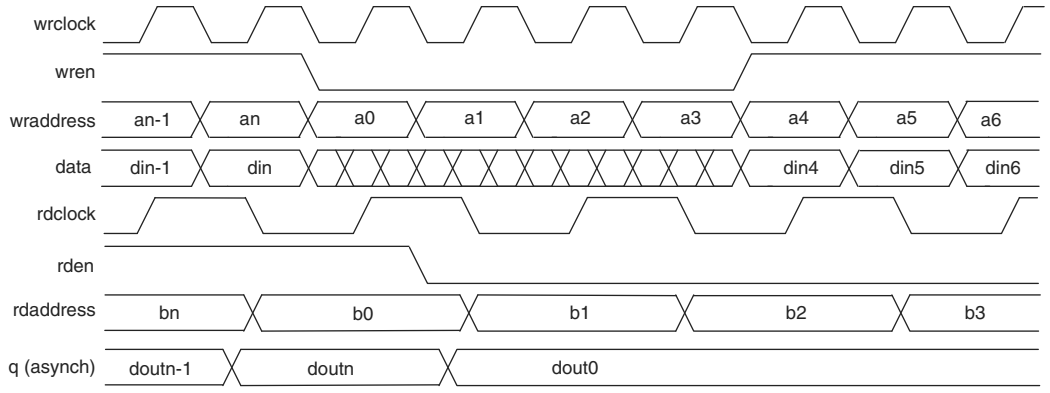


Table 4–1 lists the number of embedded multipliers and the multiplier modes that can be implemented in each Cyclone IV device.

Table 4–1. Number of Embedded Multipliers in Cyclone IV Devices

Device Family	Device	Embedded Multipliers	9 × 9 Multipliers (1)	18 × 18 Multipliers (1)
Cyclone IV GX	EP4CGX15	0	0	0
	EP4CGX22	40	80	40
	EP4CGX30	80	160	80
	EP4CGX50	140	280	140
	EP4CGX75	198	396	198
	EP4CGX110	280	560	280
	EP4CGX150	360	720	360
Cyclone IV E	EP4CE6	15	30	15
	EP4CE10	23	46	23
	EP4CE15	56	112	56
	EP4CE22	66	132	66
	EP4CE30	66	132	66
	EP4CE40	116	232	116
	EP4CE55	154	308	154
	EP4CE75	200	400	200
	EP4CE115	266	532	266

Note to Table 4–1:

(1) These columns show the number of 9 × 9 or 18 × 18 multipliers for each device.

In addition to the embedded multipliers in Cyclone IV devices, you can implement soft multipliers by using the M9K memory blocks as look-up tables (LUTs). The LUTs contain partial results from the multiplication of input data with coefficients that implement variable depth and width high-performance soft multipliers for low-cost, high-volume DSP applications. The availability of soft multipliers increases the number of available multipliers in the device.

For more information about M9K memory blocks, refer to the *Memory Blocks in Cyclone IV Devices* chapter.

For more information about soft multipliers, refer to *AN 306: Implementing Multipliers in FPGA Devices*.

Architecture

Each embedded multiplier consists of the following elements:

- Multiplier stage
- Input and output registers
- Input and output interfaces

Table 5–12. Dynamic Phase Shifting Control Signals (Part 2 of 2)

Signal Name	Description	Source	Destination
scanclk	Free running clock from core used in combination with phasestep to enable or disable dynamic phase shifting. Shared with scanclk for dynamic reconfiguration.	GCLK or I/O pins	PLL reconfiguration circuit
phasedone	When asserted, it indicates to core logic that the phase adjustment is complete and PLL is ready to act on a possible second adjustment pulse. Asserts based on internal PLL timing. De-asserts on the rising edge of scanclk.	PLL reconfiguration circuit	Logic array or I/O pins

Table 5–13 lists the PLL counter selection based on the corresponding PHASECOUNTERSELECT setting.

Table 5–13. Phase Counter Select Mapping

phasecounterselect			Selects
[2]	[1]	[0]	
0	0	0	All Output Counters
0	0	1	M Counter
0	1	0	C0 Counter
0	1	1	C1 Counter
1	0	0	C2 Counter
1	0	1	C3 Counter
1	1	0	C4 Counter

To perform one dynamic phase-shift, follow these steps:

1. Set PHASEUPDOWN and PHASECOUNTERSELECT as required.
2. Assert PHASESTEP for at least two SCANCLK cycles. Each PHASESTEP pulse allows one phase shift.
3. Deassert PHASESTEP after PHASEDONE goes low.
4. Wait for PHASEDONE to go high.
5. Repeat steps 1 through 4 as many times as required to perform multiple phase-shifts.

PHASEUPDOWN and PHASECOUNTERSELECT signals are synchronous to SCANCLK and must meet the t_{su} and t_h requirements with respect to the SCANCLK edges.

You can repeat dynamic phase-shifting indefinitely. For example, in a design where the VCO frequency is set to 1,000 MHz and the output clock frequency is set to 100 MHz, performing 40 dynamic phase shifts (each one yields 125 ps phase shift) results in shifting the output clock by 180°, in other words, a phase shift of 5 ns.

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figure 6–5 and Figure 6–6.

Figure 6–5. Cyclone IV Devices HSTL I/O Standard Termination

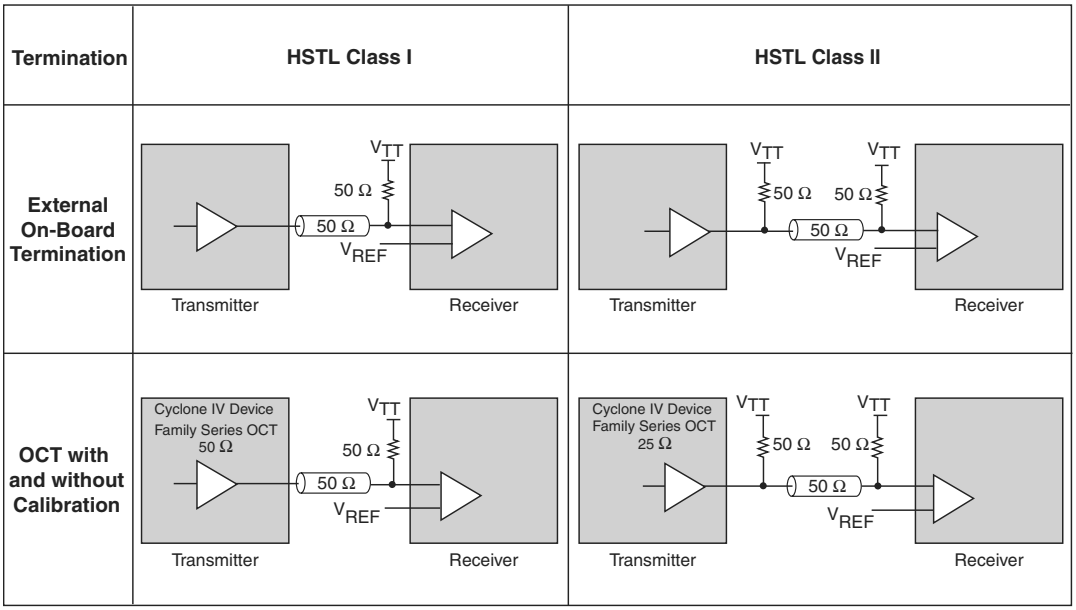


Figure 6–6. Cyclone IV Devices SSTL I/O Standard Termination

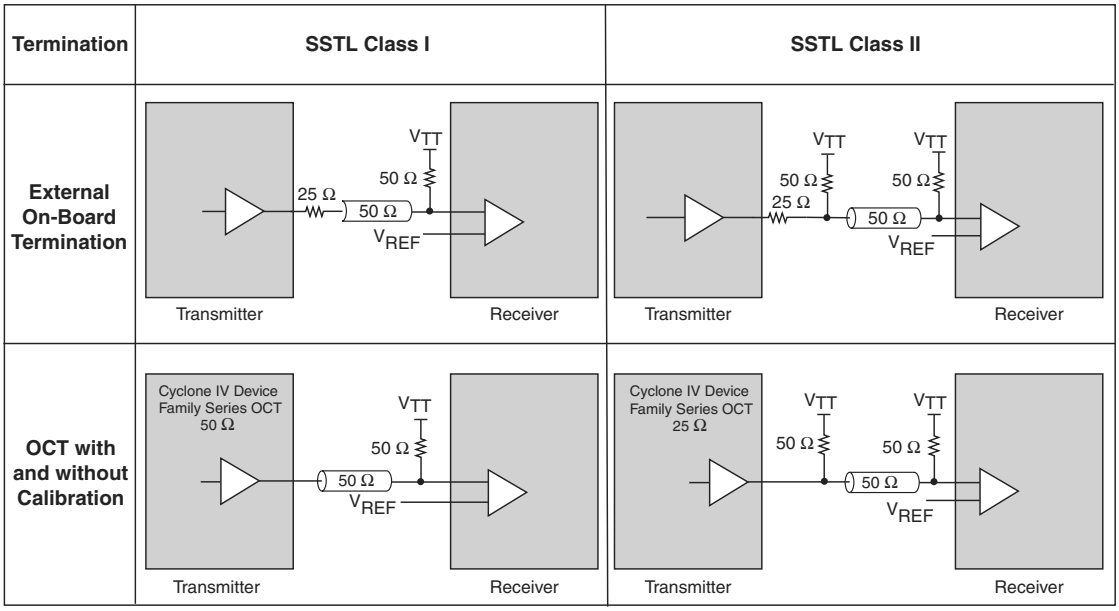


Table 6–4. Number of VREF Pins Per I/O Bank for Cyclone IV E Devices (Part 2 of 2)

Device	EP4CE6			EP4CE10			EP4CE15						EP4CE22			EP4CE30			EP4CE40				EP4CE55			EP4CE75			EP4CE115	
I/O Bank *(1)*	144-EQPF	256-UBGA	256-FBGA	144-EQPF	256-UBGA	256-FBGA	144-EQPF	164-MBGA	256-MBGA	256-UBGA	256-FBGA	484-FBGA	144-EQPF	256-UBGA	256-FBGA	324-FBGA	484-FBGA	780-FBGA	324-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-FBGA	780-FBGA
8	1	1	1	1	1	1	2	2	2	2	2	2	1	1	1	4	4	4	4	4	4	4	2	2	2	3	3	3	3	3

Note to Table 6–4:

(1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as output only.

Table 6–5. Number of VREF Pins Per I/O Bank for Cyclone IV GX Devices

Device	4CGX15	4CGX22		4CGX30			4CGX50		4CGX75		4CGX110			4CGX150		
I/O Bank *(1)*	169-FBGA	169-FBGA	324-FBGA	169-FBGA	324-FBGA	484-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	896-FBGA	484-FBGA	672-FBGA	896-FBGA
3	1	1		1		3	3		3		3			3		
4	1	1		1		3	3		3		3			3		
5	1	1		1		3	3		3		3			3		
6	1	1		1		3	3		3		3			3		
7	1	1		1		3	3		3		3			3		
8 *(2)*	1	1		1		3	3		3		3			3		

Notes to Table 6–5:

(1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as output only.

(2) Bank 9 does not have VREF pin. If input pins with VREF I/O standards are used in bank 9 during user mode, it shares the VREF pin in bank 8.

Each Cyclone IV I/O bank has its own VCCIO pins. Each I/O bank can support only one V_{CCIO} setting from among 1.2, 1.5, 1.8, 2.5, 3.0, or 3.3 V. Any number of supported single-ended or differential standards can be simultaneously supported in a single I/O bank, as long as they use the same V_{CCIO} levels for input and output pins.

Table 8–2. Uncompressed Raw Binary File (.rbf) Sizes for Cyclone IV Devices (Part 2 of 2)

Device		Data Size (bits)
Cyclone IV GX	EP4CGX15	3,805,568
	EP4CGX22	7,600,040
	EP4CGX30	7,600,040
		22,010,888 (1)
	EP4CGX50	22,010,888
	EP4CGX75	22,010,888
	EP4CGX110	39,425,016
	EP4CGX150	39,425,016

Note to Table 8–2:

(1) Only for the F484 package.

Use the data in Table 8–2 to estimate the file size before design compilation. Different configuration file formats, such as Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) formats, have different file sizes. However, for any specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you use compression, the file size varies after each compilation, because the compression ratio depends on the design.

For more information about setting device configuration options or creating configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook*.

Configuration and JTAG Pin I/O Requirements

Cyclone IV devices are manufactured using the TSMC 60-nm low-k dielectric process. Although Cyclone IV devices use TSMC 2.5-V transistor technology in the I/O buffers, the devices are compatible and able to interface with 2.5, 3.0, and 3.3-V configuration voltage standards by following specific requirements.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. When using a serial configuration device in an AS configuration scheme, you must connect a 25-Ω series resistor for the DATA[0] pin. When cascading the Cyclone IV device family in a multi-device configuration for AS, AP, FPP, and PS configuration schemes, you must connect the repeater buffers between the master and slave devices for the DATA and DCLK pins. When using the JTAG configuration scheme in a multi-device configuration, connect 25-Ω resistors on both ends of the TDO-TDI path if the TDO output driver is a non-Cyclone IV device.

The output resistance of the repeater buffers and the TDO path for all cases must fit the maximum overshoot equation shown in Equation 8–1.

Equation 8–1. (1)

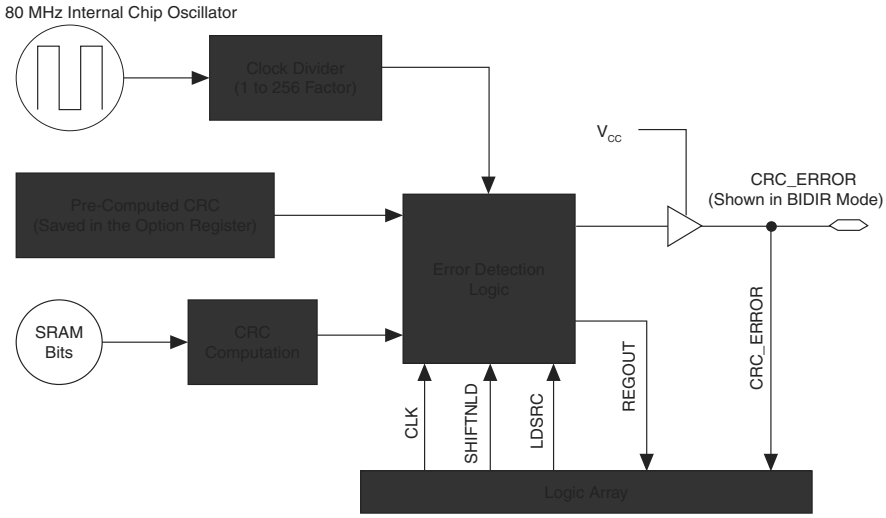
$$0.8Z_O \leq R_E \leq 1.8Z_O$$

Note to Equation 8–1:

(1) Z_O is the transmission line impedance and R_E is the equivalent resistance of the output buffer.

Figure 9–3 shows the error detection block diagram in FPGA devices and shows the interface that the WYSIWYG atom enables in your design.

Figure 9–3. Error Detection Block Diagram



The user logic is affected by the soft error failure, so reading out the 32-bit CRC signature through the `regout` should not be relied upon to detect a soft error. You should rely on the `CRC_ERROR` output signal itself, because this `CRC_ERROR` output signal cannot be affected by a soft error.

To enable the `cycloneiv_crcblock` WYSIWYG atom, you must name the atom for each Cyclone IV device accordingly.

Example 9–1 shows an example of how to define the input and output ports of a WYSIWYG atom in a Cyclone IV device.

Example 9–1. Error Detection Block Diagram

```
cycloneiv_crcblock<crcblock_name>

(

.clk(<clock source>),

.shiftnld(<shiftnld source>),

.ldsrc(<ldsrc source>),

.crcerror(<crcerror out destination>),

.regout(<output destination>),

);
```

Document Revision History

Table 10–3 lists the revision history for this chapter.

Table 10–3. Document Revision History

Date	Version	Changes
December 2013	1.3	■ Updated the “EXTEST_PULSE” section.
November 2011	1.2	■ Updated the “BST Operation Control” section. ■ Updated Table 10–2.
February 2010	1.1	■ Added Cyclone IV E devices in Table 10–1 and Table 10–2 for the Quartus II software version 9.1 SP1 release. ■ Updated Figure 10–1 and Figure 10–2. ■ Minor text edits.
November 2009	1.0	Initial release.

Section I. Transceivers

This section provides a complete overview of all features relating to the Cyclone® IV device transceivers. This section includes the following chapters:

- Chapter 1, Cyclone IV Transceivers Architecture
- Chapter 2, Cyclone IV Reset Control and Power Down
- Chapter 3, Cyclone IV Dynamic Reconfiguration

Revision History

Refer to the chapter for its own specific revision history. For information about when the chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

Transceiver Top-Level Port Lists

Table 1–26 through Table 1–29 provide descriptions of the ports available when instantiating a transceiver using the ALTGX megafunction. The ALTGX megafunction requires a relatively small number of signals. There are also a large number of optional signals that facilitate debugging by providing information about the state of the transceiver.

Document Revision History

Table 2–8 lists the revision history for this chapter.

Table 2–8. Document Revision History

Date	Version	Changes
September 2014	1.4	■ Removed the `rx_pll_locked` signal from the "Sample Reset Sequence of Receiver Only Channel—Receiver CDR in Manual Lock Mode" and the "Sample Reset Sequence of Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode" figures.
May 2013	1.3	■ Added rx_pll_locked to Figure 2–7 and Figure 2–9. ■ Added information on rx_pll_locked to "Receiver Only Channel—Receiver CDR in Manual Lock Mode" and "Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode".
November 2011	1.2	Updated the "All Supported Functional Modes Except the PCIe Functional Mode" section.
December 2010	1.1	■ Updated for the Quartus II software version 10.1 release. ■ Updated all `pll_powerdown` to `pll_areset`. ■ Added information about the `busy` signal in Figure 2–4, Figure 2–5, Figure 2–6, Figure 2–7, Figure 2–8, Figure 2–9, Figure 2–10, Figure 2–12, and Figure 2–13. ■ Added information for clarity ("Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode", "Receiver Only Channel—Receiver CDR in Automatic Lock Mode", "Receiver Only Channel—Receiver CDR in Manual Lock Mode", "Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode", and "Reset Sequence in Channel Reconfiguration Mode"). ■ Minor text edits.
July 2010	1.0	Initial release.

Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices (1) (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (2)			V_{OD} (mV) (3)			V_{OS} (V) (3)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (Column I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS (Row I/Os) (4)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
BLVDS (Column I/Os) (4)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS (Row I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
RSDS® (Row I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4

Notes to Table 1–20:

(1) For an explanation of terms used in Table 1–20, refer to "Glossary" on page 1–37.

(2) V_{IN} range: 0 V $\leq V_{IN} \leq$ 1.85 V.

(3) R_L range: 90 $\leq R_L \leq$ 110 Ω .

(4) There are no fixed V_{IN}, V_{OD}, and V_{OS} specifications for BLVDS. They depend on the system topology.

(5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.

(6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

Figure 1–2 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.

Figure 1–2. Lock Time Parameters for Manual Mode

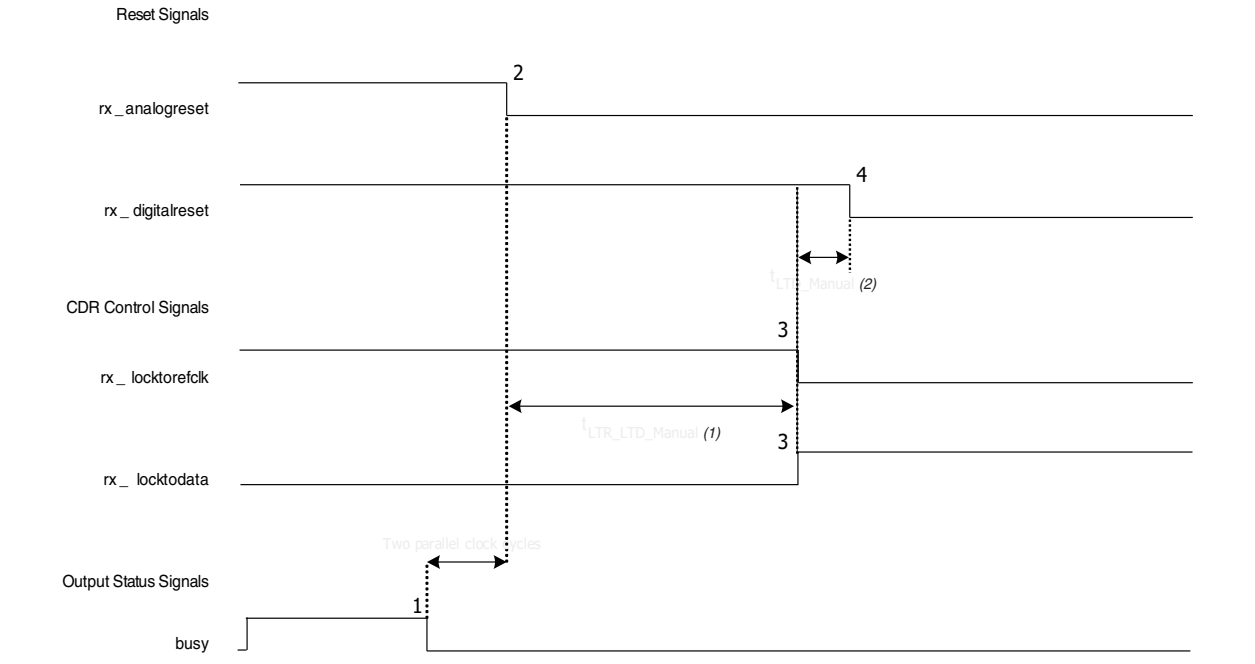


Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode

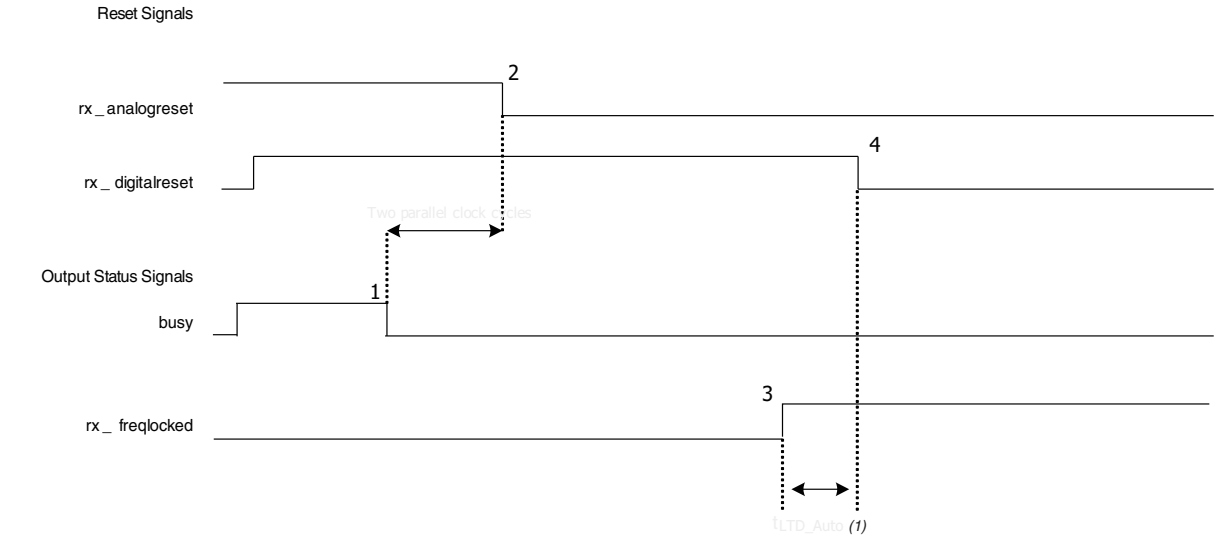


Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Parallel (AP) (1)	20 to 40	33	MHz
Active Serial (AS)	20 to 40	33	MHz

Note to Table 1–29:

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

Table 1–30. JTAG Timing Parameters for Cyclone IV Devices (1)

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	19	—	ns
t_{JCL}	TCK clock low time	19	—	ns
t_{JPSU_TDI}	JTAG port setup time for TDI	1	—	ns
t_{JPSU_TMS}	JTAG port setup time for TMS	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output (2), (3)	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output (2), (3)	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance (2), (3)	—	15	ns
t_{JSSU}	Capture register setup time	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 1–30:

(1) For more information about JTAG waveforms, refer to "JTAG Waveform" in "Glossary" on page 1–37.

(2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.

(3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to "Glossary" on page 1–37.

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 1 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	360	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	360	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	360	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	360	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	360	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	360	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	360	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
Transmitter channel-to-channel skew (TCCS)	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

Notes to Table 1–42:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns

Notes to Table 1–43:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices *(1), (2)*

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	1.209	2.184	2.336	2.451	2.387	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.208	2.200	2.399	2.554	2.446	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.438	0.404	0.751	0.825	0.886	0.839	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.713	0.682	1.228	1.41	1.566	1.424	ns

Notes to Table 1–44:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices *(1), (2)*

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.210	2.209	2.398	2.526	2.443	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.313	1.208	2.205	2.406	2.563	2.450	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.461	0.421	0.789	0.869	0.933	0.884	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.712	0.682	1.225	1.407	1.562	1.421	ns

Notes to Table 1–45:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

Table 1–46. Glossary (Part 5 of 5)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	$V_{IL\ (AC)}$	Low-level AC input voltage.
	$V_{IL\ (DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} – V_{OL}$.
	V_{OH}	Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level.
	V_{OL}	Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX\ (AC)}$	AC differential output cross point voltage: the voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for the SSTL and HSTL I/O standards.
	$V_{REF\ (AC)}$	AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on V_{REF} must not exceed 2% of $V_{REF(DC)}$.
	$V_{REF\ (DC)}$	DC input reference voltage for the SSTL and HSTL I/O standards.
	$V_{SWING\ (AC)}$	AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	$V_{SWING\ (DC)}$	DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	V_{TT}	Termination voltage for the SSTL and HSTL I/O standards.
	$V_{X\ (AC)}$	AC differential input cross point voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—