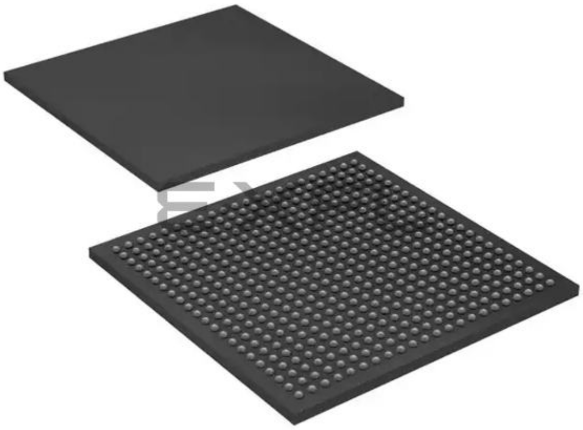

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1803
Number of Logic Elements/Cells	28848
Total RAM Bits	608256
Number of I/O	328
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce30f23c6n

In addition to the three general routing outputs, LEs in an LAB have register chain outputs, which allows registers in the same LAB to cascade together. The register chain output allows the LUTs to be used for combinational functions and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources.

LE Operating Modes

Cyclone IV LEs operate in the following modes:

- Normal mode
- Arithmetic mode

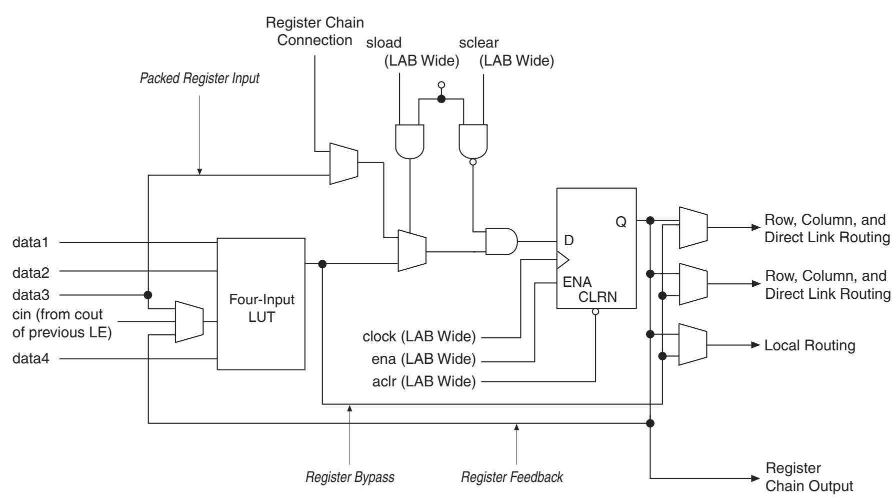
The Quartus® II software automatically chooses the appropriate mode for common functions, such as counters, adders, subtractors, and arithmetic functions, in conjunction with parameterized functions such as the library of parameterized modules (LPM) functions. You can also create special-purpose functions that specify which LE operating mode to use for optimal performance, if required.

Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (Figure 2–2). The Quartus II Compiler automatically selects the carry-in (`cin`) or the `data3` signal as one of the inputs to the LUT. LEs in normal mode support packed registers and register feedback.

Figure 2–2 shows LEs in normal mode.

Figure 2–2. Cyclone IV Device LEs in Normal Mode

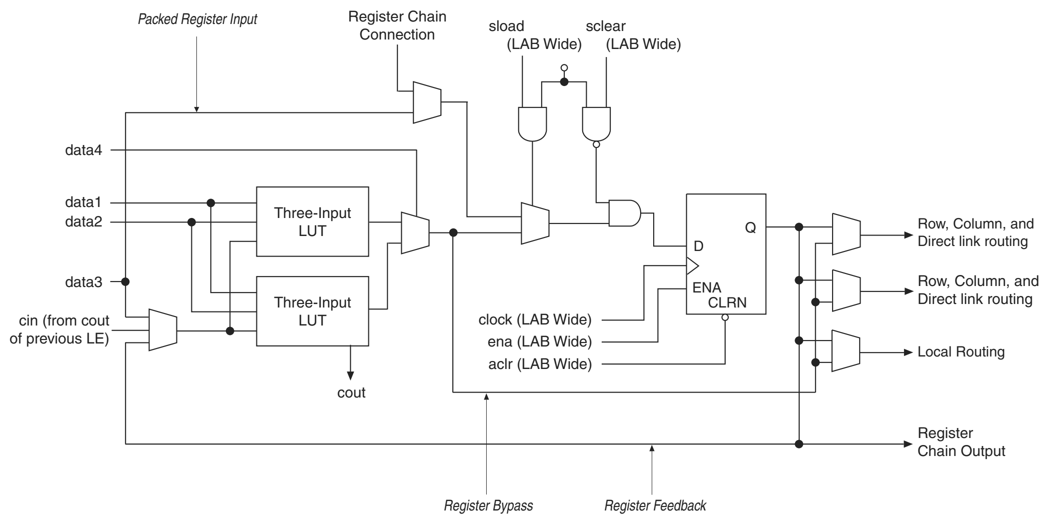


Arithmetic Mode

Arithmetic mode is ideal for implementing adders, counters, accumulators, and comparators. An LE in arithmetic mode implements a 2-bit full adder and basic carry chain (Figure 2–3). LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output. Register feedback and register packing are supported when LEs are used in arithmetic mode.

Figure 2–3 shows LEs in arithmetic mode.

Figure 2–3. Cyclone IV Device LEs in Arithmetic Mode



The Quartus II Compiler automatically creates carry chain logic during design processing. You can also manually create the carry chain logic during design entry. Parameterized functions, such as LPM functions, automatically take advantage of carry chains for the appropriate functions.

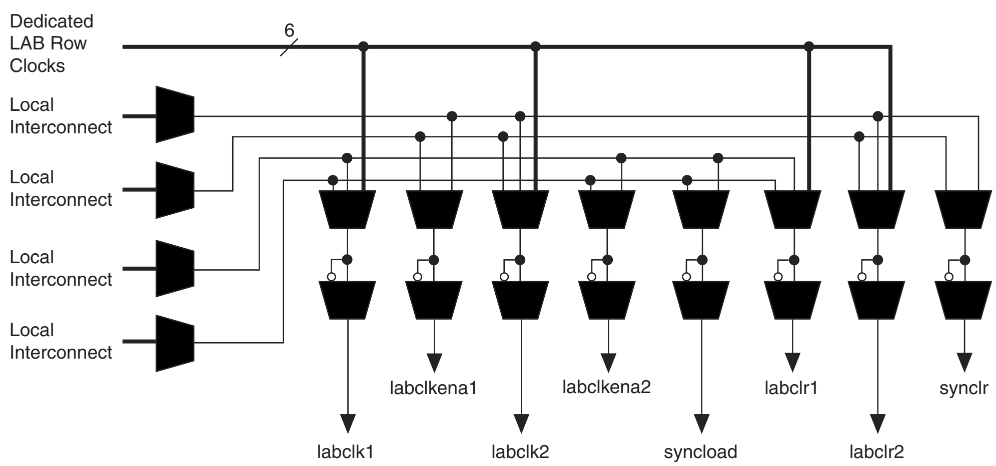
The Quartus II Compiler creates carry chains longer than 16 LEs by automatically linking LABs in the same column. For enhanced fitting, a long carry chain runs vertically, which allows fast horizontal connections to M9K memory blocks or embedded multipliers through direct link interconnects. For example, if a design has a long carry chain in an LAB column next to a column of M9K memory blocks, any LE output can feed an adjacent M9K memory block through the direct link interconnect. If the carry chains run horizontally, any LAB which is not next to the column of M9K memory blocks uses other row or column interconnects to drive a M9K memory block. A carry chain continues as far as a full column.

Each LAB can use two clocks and two clock enable signals. The clock and clock enable signals of each LAB are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses the `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect inherent low skew allows clock and control signal distribution in addition to data distribution.

Figure 2–6 shows the LAB control signal generation circuit.

Figure 2–6. Cyclone IV Device LAB-Wide Control Signals



LAB-wide signals control the logic for the clear signal of the register. The LE directly supports an asynchronous clear function. Each LAB supports up to two asynchronous clear signals (`labclr1` and `labclr2`).

A LAB-wide asynchronous load signal to control the logic for the preset signal of the register is not available. The register preset is achieved with a NOT gate push-back technique. Cyclone IV devices only support either a preset or asynchronous clear signal**.**

In addition to the clear port, Cyclone IV devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

Document Revision History

Table 2–1 shows the revision history for this chapter.

Table 2–1. Document Revision History

Date	Version	Changes
November 2009	1.0	Initial release.

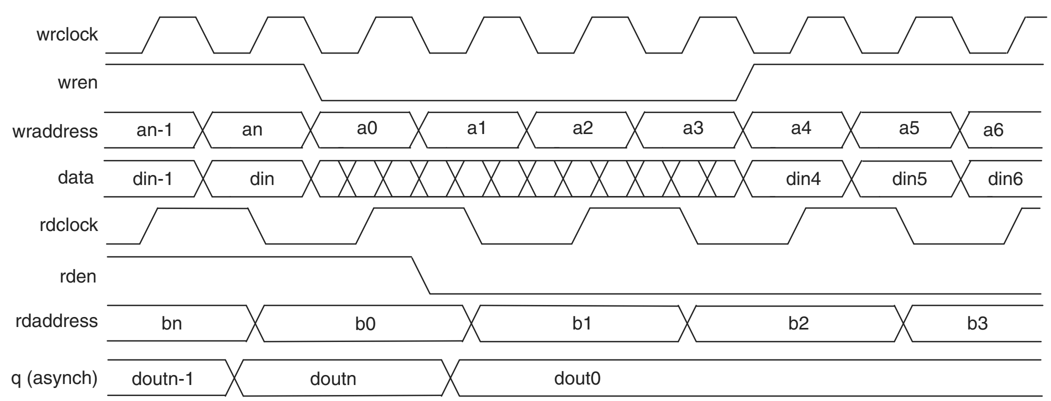
Table 3–3. Cyclone IV Devices M9K Block Mixed-Width Configurations (Simple Dual-Port Mode) ***(Part 2 of 2)***

Read Port	Write Port								
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	256 × 32	1024 × 9	512 × 18	256 × 36
512 × 16	✓	✓	✓	✓	✓	✓	—	—	—
256 × 32	✓	✓	✓	✓	✓	✓	—	—	—
1024 × 9	—	—	—	—	—	—	✓	✓	✓
512 × 18	—	—	—	—	—	—	✓	✓	✓
256 × 36	—	—	—	—	—	—	✓	✓	✓

In simple dual-port mode, M9K memory blocks support separate `wren` and `rden` signals. You can save power by keeping the `rden` signal low (inactive) when not reading. Read-during-write operations to the same address can either output "Don't Care" data at that location or output "Old Data". To choose the desired behavior, set the **Read-During-Write** option to either **Don't Care** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about this behavior, refer to "Read-During-Write Operations" on page 3–15.

Figure 3–9 shows the timing waveform for read and write operations in simple dual-port mode with unregistered outputs. Registering the outputs of the RAM simply delays the `q` output by one clock cycle.

Figure 3–9. Cyclone IV Devices Simple Dual-Port Timing Waveform



Clocking Modes

Cyclone IV devices M9K memory blocks support the following clocking modes:

- Independent
- Input or output
- Read or write
- Single-clock

When using read or write clock mode, if you perform a simultaneous read or write to the same address location, the output read data is unknown. If you require the output data to be a known value, use either single-clock mode or I/O clock mode and choose the appropriate read-during-write behavior in the MegaWizard Plug-In Manager.

☞ Violating the setup or hold time on the memory block input registers might corrupt the memory contents. This applies to both read and write operations.

☞ Asynchronous clears are available on read address registers, output registers, and output latches only.

Table 3–5 lists the clocking mode versus memory mode support matrix.

Table 3–5. Cyclone IV Devices Memory Clock Modes

Clocking Mode	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode	ROM Mode	FIFO Mode
Independent	✓	—	—	✓	—
Input or output	✓	✓	✓	✓	—
Read or write	—	✓	—	—	✓
Single-clock	✓	✓	✓	✓	✓

Independent Clock Mode

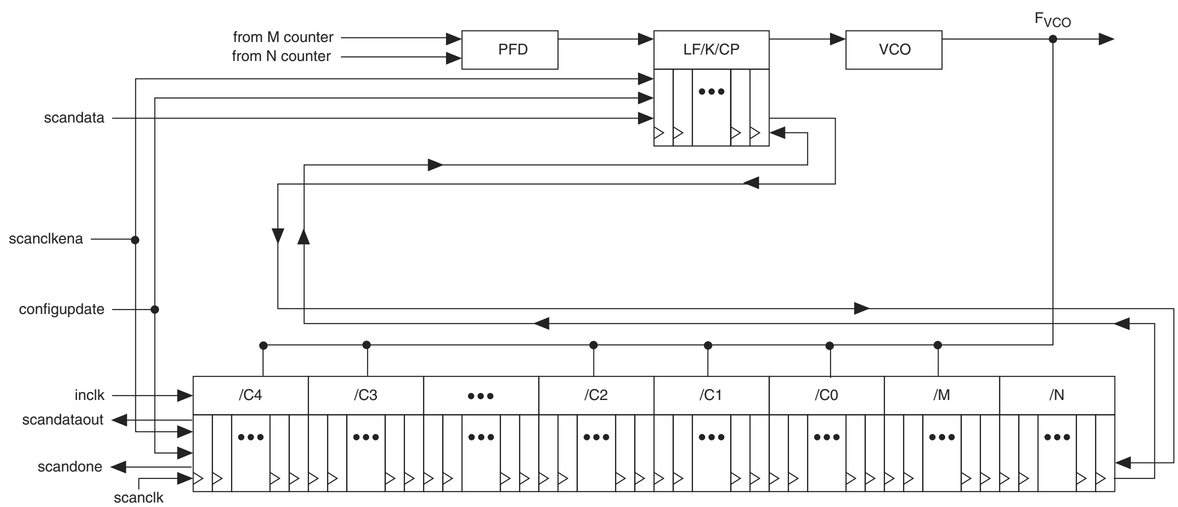
Cyclone IV devices M9K memory blocks can implement independent clock mode for true dual-port memories. In this mode, a separate clock is available for each port (port A and port B). `clock A` controls all registers on the port A side, while `clock B` controls all registers on the port B side. Each port also supports independent clock enables for port A and B registers.

Input or Output Clock Mode

Cyclone IV devices M9K memory blocks can implement input or output clock mode for FIFO, single-port, true, and simple dual-port memories. In this mode, an input clock controls all input registers to the memory block including data, address, `byteena`, `wren`, and `rden` registers. An output clock controls the data-output registers. Each memory block port also supports independent clock enables for input and output registers.

Figure 5–22 shows how to adjust PLL counter settings dynamically by shifting their new settings into a serial shift register chain or scan chain. Serial data shifts to the scan chain via the `scandataport`, and shift registers are clocked by `scanclk`. The maximum `scanclk` frequency is 100 MHz. After shifting the last bit of data, asserting the `configupdate` signal for at least one `scanclk` clock cycle synchronously updates the PLL configuration bits with the data in the scan registers.

Figure 5–22. PLL Reconfiguration Scan Chain



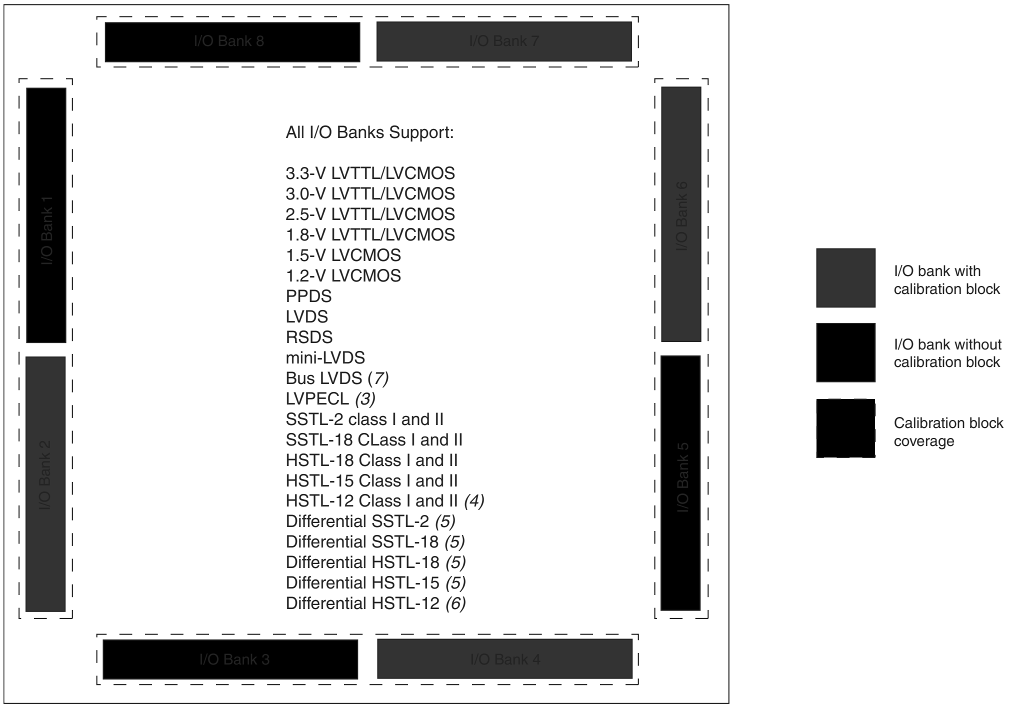
The counter settings are updated synchronously to the clock frequency of the individual counters. Therefore, not all counters update simultaneously.

To reconfigure the PLL counters, perform the following steps:

1. The `scanclkena` signal is asserted at least one `scanclk` cycle prior to shifting in the first bit of `scandata` (`D0`).
2. Serial data (`scandata`) is shifted into the scan chain on the second rising edge of `scanclk`.
3. After all 144 bits have been scanned into the scan chain, the `scanclkena` signal is de-asserted to prevent inadvertent shifting of bits in the scan chain.
4. The `configupdate` signal is asserted for one `scanclk` cycle to update the PLL counters with the contents of the scan chain.
5. The `scandone` signal goes high indicating that the PLL is being reconfigured. A falling edge indicates that the PLL counters have been updated with new settings.
6. Reset the PLL using the `areset` signal if you make any changes to the M, N, post-scale output C counters, or the I_{CP}, R, C settings.
7. You can repeat steps 1 through 5 to reconfigure the PLL any number of times.

Figure 6–9 shows the overview of Cyclone IV E I/O banks.

Figure 6–9. Cyclone IV E I/O Banks *(1)*, *(2)*



Notes to Figure 6–9:

(1) This is a top view of the silicon die. This is only a graphical representation. For exact pin locations, refer to the pin list and the Quartus II software.

(2) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only. External resistors are needed for the differential outputs in column I/O banks.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(4) The HSTL-12 Class II is supported in column I/O banks 3, 4, 7, and 8 only.

(5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. Differential SSTL-18, differential HSTL-18, and HSTL-15 I/O standards do not support Class II output.

(6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 3, 4, 7, and 8.

(7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses true LVDS input buffer.

When Cyclone IV devices successfully load the application configuration, they enter user mode. In user mode, the soft logic (the Nios II processor or state machine and the remote communication interface) assists the Cyclone IV device in determining when a remote system update is arriving. When a remote system update arrives, the soft logic receives the incoming data, writes it to the configuration memory device and triggers the device to load the factory configuration. The factory configuration reads the remote system upgrade status register, determines the valid application configuration to load, writes the remote system upgrade control register accordingly, and starts system reconfiguration.

WYSIWYG is an optimization technique that performs optimization on a VQM (Verilog Quartus Mapping) netlist in the Quartus II software.

Error Detection Block

Table 9–3 lists the types of CRC detection to check the configuration bits.

Table 9–3. Types of CRC Detection to Check the Configuration Bits

First Type of CRC Detection	Second Type of CRC Detection
■ CRAM error checking ability (32-bit CRC) during user mode, for use by the `CRC_ERROR` pin. ■ There is only one 32-bit CRC value. This value covers all the CRAM data.	■ 16-bit CRC embedded in every configuration data frame. ■ During configuration, after a frame of data is loaded into the device, the pre-computed CRC is shifted into the CRC circuitry. ■ Simultaneously, the CRC value for the data frame shifted-in is calculated. If the pre-computed CRC and calculated CRC values do not match, `nSTATUS` is set low. ■ Every data frame has a 16-bit CRC. Therefore, there are many 16-bit CRC values for the whole configuration bit stream. ■ Every device has a different length of configuration data frame.

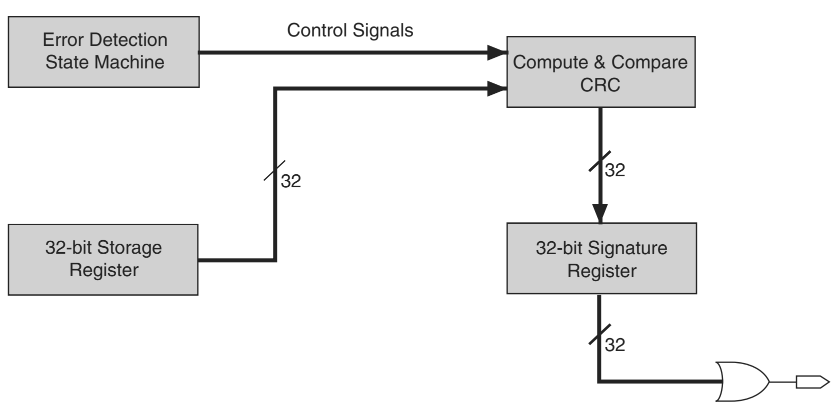
This section focuses on the first type—the 32-bit CRC when the device is in user mode.

Error Detection Registers

There are two sets of 32-bit registers in the error detection circuitry that store the computed CRC signature and pre-calculated CRC value. A non-zero value on the signature register causes the `CRC_ERROR` pin to set high.

Figure 9–1 shows the block diagram of the error detection block and the two related 32-bit registers: the signature register and the storage register.

Figure 9–1. Error Detection Block Diagram



1. Cyclone IV Transceivers Architecture

CYIV-52001-3.7

Cyclone® IV GX devices include up to eight full-duplex transceivers at serial data rates between 600 Mbps and 3.125 Gbps in a low-cost FPGA. Table 1–1 lists the supported Cyclone IV GX transceiver channel serial protocols.

Table 1–1. Serial Protocols Supported by the Cyclone IV GX Transceiver Channels

Protocol	Data Rate (Gbps)	F324 and smaller packages	F484 and larger packages
PCI Express® (PCIe®) (1)	2.5	✓	✓
Gbps Ethernet (GbE)	1.25	✓	✓
Common Public Radio Interface (CPRI)	0.6144, 1.2288, 2.4576, and 3.072	✓ (2)	✓
OBSAI	0.768, 1.536, and 3.072	✓ (2)	✓
XAUI	3.125	—	✓
Serial digital interface (SDI)	HD-SDI at 1.485 and 1.4835	✓	✓
	3G-SDI at 2.97 and 2.967	—	
Serial RapidIO® (SRIO)	1.25, 2.5, and 3.125	—	✓
Serial Advanced Technology Attachment (SATA)	1.5 and 3.0	—	✓
V-by-one	3.125	—	✓
Display Port	1.62 and 2.7	—	✓

Notes to Table 1–1:

(1) Provides the physical interface for PCI Express (PIPE)-compliant interface that supports Gen1 ×1, ×2, and ×4 initial lane width configurations. When implementing ×1 or ×2 interface, remaining channels in the transceiver block are available to implement other protocols.

(2) Supports data rates up to 2.5 Gbps only.

You can implement these protocols through the ALTGX MegaWizard™ Plug-In Manager, which also offers the highly flexible Basic functional mode to implement proprietary serial protocols at the following serial data rates:

- 600 Mbps to 2.5 Gbps for devices in F324 and smaller packages
- 600 Mbps to 3.125 Gbps for devices in F484 and larger packages

For descriptions of the ports available when instantiating a transceiver using the ALTGX megafunction, refer to “Transceiver Top-Level Port Lists” on page 1–85.

For more information about Cyclone IV transceivers that run at ≥2.97 Gbps data rate, refer to the *Cyclone IV Device Family Pin Connection Guidelines*.

The hard IP block supports 1, 2, or 4 initial lane configurations with a maximum payload of 256 bytes at Gen1 frequency. The application interface is 64 bits with a data width of 16 bits per channel running at up to 125 MHz. As a hard macro and a verified block, it uses very few FPGA resources, while significantly reducing design risk and the time required to achieve timing closure. It is compliant with the PCI Express Base Specification 1.1. You do not have to pay a licensing fee to use this module. Configuring the hard IP block requires using the PCI Express Compiler.

For more information about the hard IP block, refer to the *PCI Express Compiler User Guide*.

Figure 1–43 shows the lane placement requirements when implementing PCIe with hard IP block.

Figure 1–43. PCIe with Hard IP Block Lane Placement Requirements (1)

Note to Figure 1–43:

(1) Applicable for PCIe ×1, ×2, and ×4 implementations with hard IP blocks only.

Transceiver Functional Modes

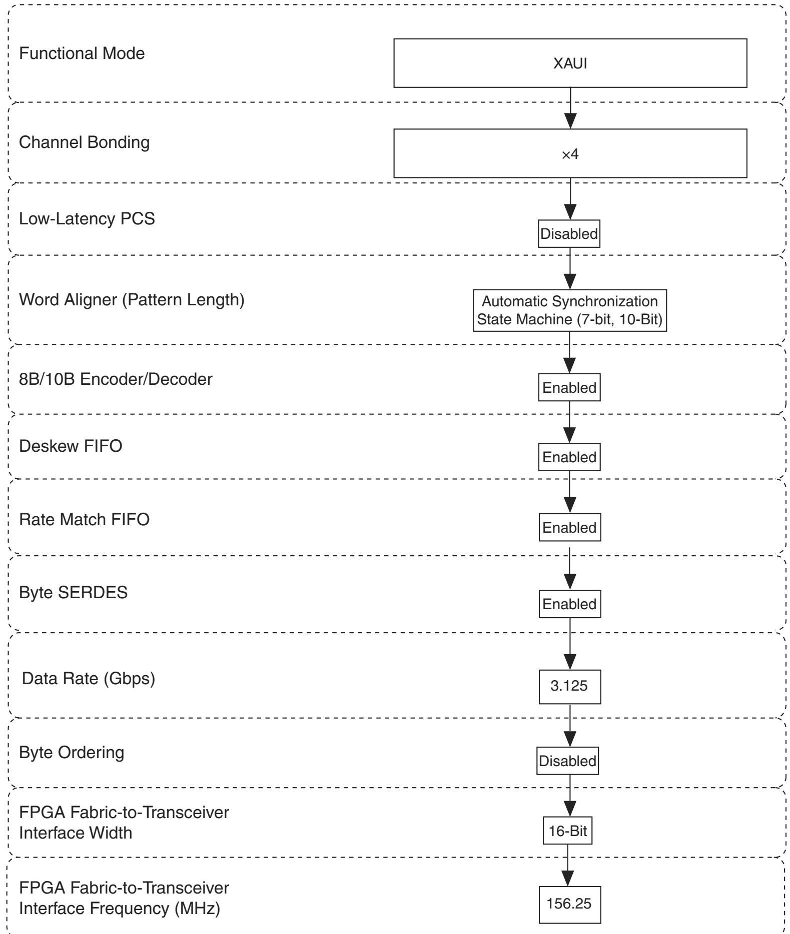
The Cyclone IV GX transceiver supports the functional modes as listed in Table 1–14 for protocol implementation.

Table 1–14. Transceiver Functional Modes for Protocol Implementation (Part 1 of 2)

Functional Mode	Protocol	Key Feature	Reference
Basic	Proprietary, SATA, V-by-One, Display Port	Low latency PCS, transmitter in electrical idle, signal detect at receiver, wider spread asynchronous SSC	"Basic Mode" on page 1–48
PCI Express (PIPE)	PCIe Gen1 with PIPE Interface	PIPE ports, receiver detect, transmitter in electrical idle, electrical idle inference, signal detect at receiver, fast recovery, protocol-compliant word aligner and rate match FIFO, synchronous SSC	"PCI Express (PIPE) Mode" on page 1–52
GIGE	GbE	Running disparity preservation, protocol-compliant word aligner, recovered clock port for applications such as Synchronous Ethernet	"GIGE Mode" on page 1–59
Serial RapidIO	SRIO	Protocol-compliant word aligner	"Serial RapidIO Mode" on page 1–64
XAUI	XAUI	Deskew FIFO, protocol-compliant word aligner and rate match FIFO	"XAUI Mode" on page 1–67

Figure 1–64 shows the transceiver configuration in XAUI mode.

Figure 1–64. Transceiver Configuration in XAUI Mode



XGMII and PCS Code Conversions

In XAUI mode, the 8B/10B encoder in the transmitter datapath maps various 8-bit XGMII codes to 10-bit PCS code groups as listed in Table 1–21.

Table 1–21. XGMII Character to PCS Code Groups Mapping (Part 1 of 2)

XGMII TXC (1)	XGMII TXD (2), (3)	PCS Code Group	Description
0	00 through FF	Dxx,y	Normal data transmission
1	07	K28.0, K28.3, or K28.5	Idle in ||I||
1	07	K28.5	Idle in ||T||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error

4. Wait for at least $t_{LTR\_LTD\_Manual}$ (the time between markers 6 and 7), then deassert the `rx_locktorefclk` signal. At the same time, assert the `rx_locktodata` signal (marker 7). At this point, the receiver CDR enters lock-to-data mode and the receiver CDR starts locking to the received data.
5. Deassert `rx_digitalreset` at least t_{LTD_Manual} (the time between markers 7 and 8) after asserting the `rx_locktodata` signal. At this point, the transmitter and receiver are ready for data traffic.

Reset Sequence in Loss of Link Conditions

Loss of link can occur due to loss of local reference clock source or loss of the link due to an unplugged cable. Other adverse conditions like loss of power could also cause the loss of signal from the other device or link partner.

Loss of Local REFCLK or Other Reference Clock Condition

Should local reference clock input become disabled or unstable, take the following steps:

1. Monitor `pll_locked` signal. `Pll_locked` is de-asserted if local reference clock source becomes unavailable.
2. `Pll_locked` assertion indicates a stable reference clock because TX PLL locks to the incoming clock. You can follow appropriate reset sequence provided in the device handbook, starting from `pll_locked` assertion.

Loss of Link Due To Unplugged Cable or Far End Shut-off Condition

Use one or more of the following methods to identify whether link partner is alive:

- Signal detect is available in PCIe and Basic modes. You can monitor `rx_signaldetect` signal as loss of link indicator. `rx_signaldetect` is asserted when the link partner comes back up.
- You can implement a ppm detector in device core for modes that do not have signal detect to monitor the link. Ppm detector helps in identifying whether the link is alive.
- Data corruption or RX phase comp FIFO overflow or underflow condition in user logic may indicate a loss of link condition.

Apply the following reset sequences when loss of link is detected:

- For Automatic CDR lock mode:
  a. Monitor `rx_freqlocked` signal. Loss of link causes `rx_freqlocked` to be de-asserted when CDR moves back to lock-to-data (LTD) mode.
  b. Assert `rx_digitalreset`.
  c. `rx_freqlocked` toggles over time when CDR switches between lock-to-reference (LTR) and LTD modes.
  d. If `rx_freqlocked` goes low at any point, re-assert `rx_digitalreset`.
  e. If data corruption or RX phase comp FIFO overflow or underflow condition is observed in user logic, assert `rx_digitalreset` for 2 parallel clock cycles, then de-assert the signal.

- In PCIe mode simulation, you must assert the tx_forceelecidle signal for at least one parallel clock cycle before transmitting normal data for correct simulation behavior.

Reference Information

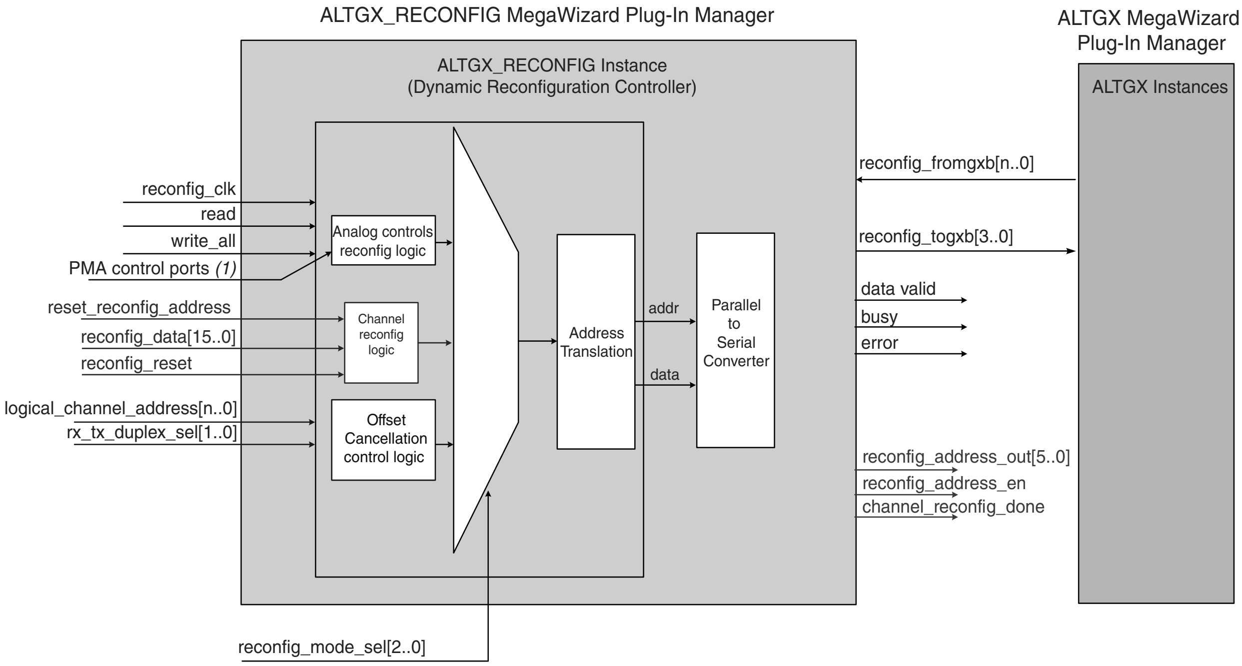
For more information about some useful reference terms used in this chapter, refer to the links listed in Table 2–7.

Table 2–7. Reference Information

Terms Used in this Chapter	Useful Reference Points
Automatic Lock Mode	page 2–8
Bonded channel configuration	page 2–6
busy	page 2–3
Dynamic Reconfiguration Reset Sequences	page 2–19
gxb_powerdown	page 2–3
LTD	page 2–6
LTR	page 2–6
Manual Lock Mode	page 2–9
Non-Bonded channel configuration	page 2–10
PCIe	page 2–17
pll_locked	page 2–3
pll_areset	page 2–3
rx_analogreset	page 2–2
rx_digitalreset	page 2–2
rx_freqlocked	page 2–3
tx_digitalreset	page 2–2

Figure 3–1 shows a conceptual view of the dynamic reconfiguration controller architecture. For a detailed description of the inputs and outputs of the ALTGX_RECONFIG instance, refer to "Error Indication During Dynamic Reconfiguration" on page 3–36.

Figure 3–1. Dynamic Reconfiguration Controller



Note to Figure 3–1:

(1) The PMA control ports consist of the V_{OD}, pre-emphasis, DC gain, and manual equalization controls.

Only PMA reconfiguration mode supports manual equalization controls.

You can use one ALTGX_RECONFIG instance to control multiple transceiver blocks. However, you cannot use multiple ALTGX_RECONFIG instances to control one transceiver block.

Contents

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (F324 and smaller package) *(15)*	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package) *(15)*	—	600	—	3125	600	—	3125	600	—	2500	Mbps
Absolute V_{MAX} for a receiver pin *(3)*	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{ICM} = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps	0.1	—	2.7	0.1	—	2.7	0.1	—	2.7	V
V_{ICM}	V_{ICM} = 0.82 V setting	—	820 ± 10%	—	—	820 ± 10%	—	—	820 ± 10%	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150–Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI	Compliant									—
Programmable ppm detector *(4)*	—	± 62.5, 100, 125, 200, 250, 300									ppm
Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)	—	—	—	±300 *(5)*, ±350 *(6)*, *(7)*	—	—	±300 *(5)*, ±350 *(6)*, *(7)*	—	—	±300 *(5)*, ±350 *(6)*, *(7)*	ppm
CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) *(8)*	—	—	—	350 to –5350 *(7)*, *(9)*	—	—	350 to –5350 *(7)*, *(9)*	—	—	350 to –5350 *(7)*, *(9)*	ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	No Equalization	—	—	1.5	—	—	1.5	—	—	1.5	dB
	Medium Low	—	—	4.5	—	—	4.5	—	—	4.5	dB
	Medium High	—	—	5.5	—	—	5.5	—	—	5.5	dB
	High	—	—	7	—	—	7	—	—	7	dB

Figure 1–2 shows the lock time parameters in manual mode.

☞ LTD = lock-to-data. LTR = lock-to-reference.

Figure 1–2. Lock Time Parameters for Manual Mode

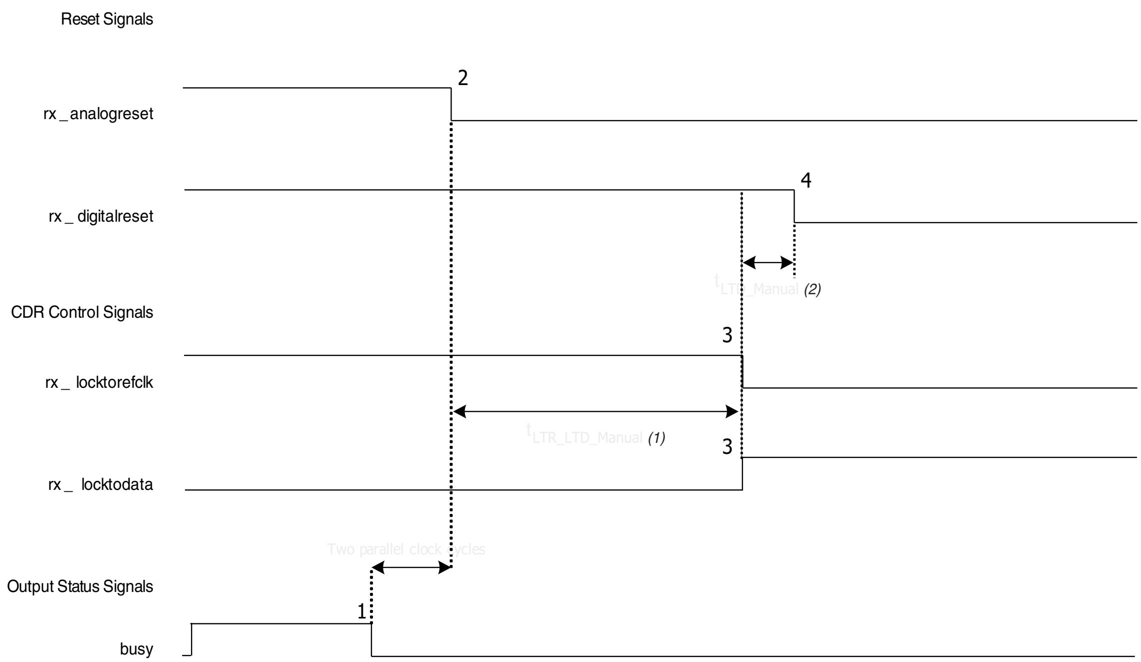


Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode