Intel - EP4CE30F23C9L Datasheet





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Details	
Product Status	Active
Number of LABs/CLBs	1803
Number of Logic Elements/Cells	28848
Total RAM Bits	608256
Number of I/O	328
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce30f23c9l

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Package Matrix

Table 1–3 lists Cyclone IV E device package offerings.

Table 1-3.	Package Offer	ngs for the Cyclo	ne IV E Device F	amily ^{(1),} ⁽²⁾
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Package	E1	44	M1	64	M2	56	U2	56	F2	56	F3	24	U4	84	F4	84	F7	80
Size (mm)	22 >	< 22	8 >	< 8	9)	9	14 >	< 14	17 >	< 17	19 3	c 19	19,	< 19	23 >	× 23	29 >	« 29
Pitch (mm)	0.	.5	0.	.5	0.	5	0.	.8	1.	.0	1.	.0	0.	.8	1.	.0	1.	.0
Device	User I/O	(s) San	User I/O	(8) SOA	User I/O	LVDS ⁽³⁾	User I/O	(8) San	User I/O	(8) San	User I/O	(3)	User I/O	LVDS ⁽³⁾	User I/O	LVDS ⁽³⁾	User I/O	LVDS ⁽³⁾
EP4CE6	▲91	21	—	_	—	_	▲ 179	66	▲ 179	66	_	—	—	—	—	—	—	—
EP4CE10	91	21	—	_	—	_	179	66	179	66	_	_	_	—	_	—	_	—
EP4CE15	81	18	89	21	165	53	165	53	165	53	_	_	_	— .	▲ 343	137	_	—
EP4CE22	₹79	17	—	_	—	_	▼ 153	52	▼ 153	52	_	_	_	—	—	—	_	—
EP4CE30	_	—	—	_	—	_	—	_	_	_	▲ 193	68	_	—	328	124	▲532	224
EP4CE40		—	—	_	—	_	—	_		_	193	68	▲ 328	124	328	124	532	224
EP4CE55	—	—	—	_	—		—	—		—	_	—	324	132	324	132	374	160
EP4CE75	_	—	—	_	—	_	—	_		—	—		292	110	292	110	426	178
EP4CE115	—	—	—	_	—		—	—		—	_	—	—		280	103	▼528	230

Notes to Table 1-3:

(1) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane of your PCB. Use this exposed pad for electrical connectivity and not for thermal purposes.

(2) Use the Pin Migration View window in Pin Planner of the Quartus II software to verify the pin migration compatibility when you perform device migration. For more information, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

(3) This includes both dedicated and emulated LVDS pairs. For more information, refer to the I/O Features in Cyclone IV Devices chapter.

In addition to the three general routing outputs, LEs in an LAB have register chain outputs, which allows registers in the same LAB to cascade together. The register chain output allows the LUTs to be used for combinational functions and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources.

LE Operating Modes

Cyclone IV LEs operate in the following modes:

- Normal mode
- Arithmetic mode

The Quartus[®] II software automatically chooses the appropriate mode for common functions, such as counters, adders, subtractors, and arithmetic functions, in conjunction with parameterized functions such as the library of parameterized modules (LPM) functions. You can also create special-purpose functions that specify which LE operating mode to use for optimal performance, if required.

Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (Figure 2–2). The Quartus II Compiler automatically selects the carry-in (cin) or the data3 signal as one of the inputs to the LUT. LEs in normal mode support packed registers and register feedback.

Figure 2–2 shows LEs in normal mode.





2–3

Bood Bort		Write Port												
ncau r ui i	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	256 × 32	1024 × 9	512 × 18	256 × 36					
512 × 16	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	—	—	—					
256 × 32	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	~	—	—	—					
1024 × 9	—	—	—	—	—	—	\checkmark	\checkmark	\checkmark					
512 × 18		—	—	—	—	—	\checkmark	\checkmark	\checkmark					
256 × 36	—	—	—	—	—	—	\checkmark	\checkmark	\checkmark					

Table 3-3.	Cyclone IV Devices M9K Block Mixed-Width Configurations (Simple Dual-Port Mode)	(Part 2 of 2)
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In simple dual-port mode, M9K memory blocks support separate wren and rden signals. You can save power by keeping the rden signal low (inactive) when not reading. Read-during-write operations to the same address can either output "Don't Care" data at that location or output "Old Data". To choose the desired behavior, set the **Read-During-Write** option to either **Don't Care** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about this behavior, refer to "Read-During-Write Operations" on page 3–15.

Figure 3–9 shows the timing waveform for read and write operations in simple dual-port mode with unregistered outputs. Registering the outputs of the RAM simply delays the q output by one clock cycle.





If you do not use dedicated clock pins to feed the GCLKs, you can use them as general-purpose input pins to feed the logic array. However, when using them as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

Constitution For more information about how to connect the clock and PLL pins, refer to the *Cyclone IV Device Family Pin Connection Guidelines*.

Clock Control Block

The clock control block drives the GCLKs. Clock control blocks are located on each side of the device, close to the dedicated clock input pins. GCLKs are optimized for minimum clock skew and delay.

Table 5–4 lists the sources that can feed the clock control block, which in turn feeds the GCLKs.

Input	Description
Dedicated clock inputs	Dedicated clock input pins can drive clocks or global signals, such as synchronous and asynchronous clears, presets, or clock enables onto given GCLKs.
Dual-purpose clock (DPCLK and CDPCLK) I/O input	DPCLK and CDPCLK I/O pins are bidirectional dual function pins that are used for high fan-out control signals, such as protocol signals, TRDY and IRDY signals for PCI, via the GCLK. Clock control blocks that have inputs driven by dual-purpose clock I/O pins are not able to drive PLL inputs.
PLL outputs	PLL counter outputs can drive the GCLK.
Internal logic	You can drive the GCLK through logic array routing to enable internal logic elements (LEs) to drive a high fan-out, low-skew signal path. Clock control blocks that have inputs driven by internal logic are not able to drive PLL inputs.

Table 5-4. Clock Control Block Inputs

In Cyclone IV devices, dedicated clock input pins, PLL counter outputs, dual-purpose clock I/O inputs, and internal logic can all feed the clock control block for each GCLK. The output from the clock control block in turn feeds the corresponding GCLK. The GCLK can drive the PLL input if the clock control block inputs are outputs of another PLL or dedicated clock input pins. There are five or six clock control blocks on each side of the device periphery—depending on device density; providing up to 30 clock control blocks in each Cyclone IV GX device. The maximum number of clock control blocks per Cyclone IV E device is 20. For the clock control block locations, refer to Figure 5–2 on page 5–12, Figure 5–3 on page 5–13, and Figure 5–4 on page 5–14.

The clock control blocks on the left side of the Cyclone IV GX device do not support any clock inputs.

The control block has two functions:

- Dynamic GCLK clock source selection (not applicable for DPCLK, CDPCLK, and internal logic input)
- GCLK network power down (dynamic enable and disable)

Table 6–8 and Table 6–9 summarize the total number of supported row and column differential channels in the Cyclone IV device family.

Table 6–8. Cyclone IV E I/O and Differential Channel Count

Device		EP4CE6			EP4CE10				EDAFE16					EP4CE22			EP4CE30			EDACEAD	Er46640			EP4CE55			EP4CE75		EDAPE116	
Numbers of Differential Channels <i>(1), (2</i>)	144-EQPF	256-UBGA	256-FBGA	144-EQPF	256-UBGA	256-FBGA	144-EQPF	164-MBGA	256-MBGA	256-UBGA	256-FBGA	484-FBGA	144-EQPF	256-UBGA	256-FBGA	324-FBGA	484-FBGA	780-FBGA	324-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-FBGA	780-FBGA
User I/O (3)	91	179	179	91	179	179	81	89	165	165	165	343	79	153	153	193	328	532	193	328	328	532	324	324	374	292	292	426	280	528
User I/O Banks	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
LVDS (4), (6)	8	23	23	8	23	23	6	8	21	21	21	67	7	20	20	30	60	112	30	60	60	112	62	62	70	54	54	79	50	103
Emulated LVDS <i>(5), (</i> <i>6)</i>	13	43	43	13	43	43	12	13	32	32	32	70	10	32	32	38	64	112	38	64	64	112	70	70	90	56	56	99	53	127

Notes to Table 6-8:

(1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as output only.

(2) For differential pad placement guidelines, refer to "Pad Placement" on page 6-23.

(3) The I/O pin count includes all GPIOs, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(4) The true LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in row I/O banks 1, 2, 5, and 6.

(5) The emulated LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in column I/O banks 3, 4, 7, and 8.

(6) LVDS input and output buffers are sharing the same p and n pins. One LVDS I/O channel can only be either transmitter or receiver at a time.

Table 7–2 lists the number of DQS or DQ groups supported on each side of the Cyclone IV E device.

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
		Left	0	0	0	0	—	—
	144 pip EOED	Right	0	0	0	0	—	—
	144-pill EQFP	Bottom (1), (3)	1	0	0	0	—	—
		Top (1), (4)	1	0	0	0	—	—
		Left (1)	1	1	0	0	—	—
EP4CE6	256-pip LIBGA	Right ⁽²⁾	1	1	0	0	—	—
EP4CE10	250-piil 080A	Bottom	2	2	1	1	—	—
		Тор	2	2	1	1	—	—
		Left (1)	1	1	0	0	—	—
	256 pip EPCA	Right ⁽²⁾	1	1	0	0	—	—
	250-piii FBGA	Bottom	2	2	1	1	—	—
		Тор	2	2	1	1	—	—
		Left	0	0	0	0	—	—
	144 pip EOED	Right	0	0	0	0	—	—
	144-pill EQFP	Bottom (1), (3)	1	0	0	0	—	—
		Top (1), (4)	1	0	0	0	—	—
		Left	0	0	0	0	—	—
	164 pip MPCA	Right	0	0	0	0	—	—
		Bottom (1), (3)	1	0	0	0	—	—
		Top (1), (4)	1	0	0	0	—	—
		Left	1	1	0	0	—	—
	256 pip MPCA	Right	1	1	0	0	—	—
		Bottom (1), (3)	2	2	1	1	—	—
		Top (1), (4)	2	2	1	1	—	—
EF40E15		Left (1)	1	1	0	0	—	—
	256 pip LIPCA	Right (2)	1	1	0	0	—	—
	250-piil 080A	Bottom	2	2	1	1	—	—
		Тор	2	2	1	1	—	—
		Left (1)	1	1	0	0	—	—
	256 pip EPCA	Right ⁽²⁾	1	1	0	0	—	—
	250-piii FBGA	Bottom	2	2	1	1	—	—
		Тор	2	2	1	1	—	—
		Left	4	4	2	2	1	1
	484-nin EPCA	Right	4	4	2	2	1	1
	чоч-ріп град	Bottom	4	4	2	2	1	1
		Тор	4	4	2	2	1	1

You can begin reconfiguration by pulling the nCONFIG pin low. The nCONFIG pin must be low for at least 500 ns. When nCONFIG is pulled low, the Cyclone IV device is reset. The Cyclone IV device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. When nCONFIG returns to a logic-high level and nSTATUS is released by the Cyclone IV device, reconfiguration begins.

Configuration Error

If an error occurs during configuration, Cyclone IV devices assert the nSTATUS signal low, indicating a data frame error and the CONF_DONE signal stays low. If the **Auto-restart configuration after error** option (available in the Quartus II software in the **General** tab of the **Device and Pin Options** dialog box) is turned on, the Cyclone IV device releases nSTATUS after a reset time-out period (a maximum of 230 μ s), and retries configuration. If this option is turned off, the system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 500 ns to restart configuration.

Initialization

In Cyclone IV devices, the initialization clock source is either the internal oscillator or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the device provides itself with enough clock cycles for proper initialization. When using the internal oscillator, you do not have to send additional clock cycles from an external source to the CLKUSR pin during the initialization stage. Additionally, you can use the CLKUSR pin as a user I/O pin.

You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the **CLKUSR** option. The CLKUSR pin allows you to control when your device enters user mode for an indefinite amount of time. You can turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software in the **General** tab of the **Device and Pin Options** dialog box. When you turn on the **Enable user supplied start-up clock option (CLKUSR)** option, the CLKUSR pin is the initialization clock source. Supplying a clock on the CLKUSR pin does not affect the configuration process. After the configuration data is accepted and CONF_DONE goes high, Cyclone IV devices require 3,192 clock cycles to initialize properly and enter user mode.

If you use the optional CLKUSR pin and the nCONFIG pin is pulled low to restart configuration during device initialization, ensure that the CLKUSR pin continues to toggle when nSTATUS is low (a maximum of 230 µs).

User Mode

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software in the **General** tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it is high due to an external $10-k\Omega$ pull-up resistor when nCONFIG is low and during the beginning of configuration. After the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. This low-to-high transition signals that the device has entered user mode. In user mode, the user I/O pins function as assigned in your design and no longer have weak pull-up resistors.

Byte-Wide Multi-Device AP Configuration

The simpler method for multi-device AP configuration is the byte-wide multi-device AP configuration. In the byte-wide multi-device AP configuration, the LSB of the DATA [7..0] pin from the flash and master device (set to the AP configuration scheme) is connected to the slave devices set to the FPP configuration scheme, as shown in Figure 8–8.





Notes to Figure 8-8:

- (1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.
- (3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the master device in AP mode and the slave devices in FPP mode. To connect MSEL [3..0] for the master device in AP mode and the slave devices in FPP mode, refer to Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (5) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.
- (6) Connect the repeater buffers between the Cyclone IV E master device and slave devices for DATA [15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8–5.

Word-Wide Multi-Device AP Configuration

The more efficient setup is one in which some of the slave devices are connected to the LSB of the DATA[7..0] and the remaining slave devices are connected to the MSB of the DATA[15..8]. In the word-wide multi-device AP configuration, the nCEO pin of the master device enables two separate daisy chains of slave devices, allowing both chains to be programmed concurrently, as shown in Figure 8–9.

The nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors, as shown in Figure 8–8 on page 8–26 and Figure 8–9 on page 8–27. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they receive their configuration data. When all target devices in the chain receive their configuration data and release CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

Guidelines for Connecting Parallel Flash to Cyclone IV E Devices for an AP Interface

For single- and multi-device AP configuration, the board trace length and loading between the supported parallel flash and Cyclone IV E devices must follow the recommendations listed in Table 8–11. These recommendations also apply to an AP configuration with multiple bus masters.

Cyclone IV E AP Pins	Maximum Board Trace Length from Cyclone IV E Device to Flash Device (inches)	Maximum Board Load (pF)
DCLK	6	15
DATA[150]	6	30
PADD[230]	6	30
nRESET	6	30
Flash_nCE	6	30
nOE	6	30
nAVD	6	30
nWE	6	30
I/O (1)	6	30

 Table 8–11. Maximum Trace Length and Loading for AP Configuration

Note to Table 8-11:

(1) The AP configuration ignores the WAIT signal from the flash during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.

Configuring With Multiple Bus Masters

Similar to the AS configuration scheme, the AP configuration scheme supports multiple bus masters for the parallel flash. For another master to take control of the AP configuration bus, the master must assert nCONFIG low for at least 500 ns to reset the master Cyclone IV E device and override the weak 10-k Ω pull-down resistor on the nCE pin. This resets the master Cyclone IV E device then takes control of the AP configuration bus. The other master device then takes control of the AP configuration bus, then releases the nCE pin, and finally pulses nCONFIG low to restart the configuration.

In the AP configuration scheme, multiple masters share the parallel flash. Similar to the AS configuration scheme, the bus control is negotiated by the nCE pin.

EN_ACTIVE_CLK

The EN_ACTIVE_CLK instruction causes the CLKUSR pin signal to replace the internal oscillator as the clock source. When using the EN_ACTIVE_CLK instruction, you must enable the internal oscillator for the clock change to occur. After this instruction is issued, other JTAG instructions can be issued while the CLKUSR pin signal remains as the clock source. The clock source is only reverted back to the internal oscillator by issuing the DIS_ACTIVE_CLK instruction or a POR.

DIS_ACTIVE_CLK

The DIS_ACTIVE_CLK instruction breaks the CLKUSR enable latch set by the EN_ACTIVE_CLK instruction and causes the clock source to revert back to the internal oscillator. After the DIS_ACTIVE_CLK instruction is issued, you must continue to clock the CLKUSR pin for 10 clock cycles.

Changing the Start Boot Address of the AP Flash

In the AP configuration scheme (for Cyclone IV E devices only), you can change the default configuration boot address of the parallel flash memory to any desired address using the APFC_BOOT_ADDR JTAG instruction.

APFC_BOOT_ADDR

The APFC_BOOT_ADDR instruction is for Cyclone IV E devices only and allows you to define a start boot address for the parallel flash memory in the AP configuration scheme.

This instruction shifts in a start boot address for the AP flash. When this instruction becomes the active instruction, the TDI and TDO pins are connected through a 22-bit active boot address shift register. The shifted-in boot address bits get loaded into the 22-bit AP boot address update register, which feeds into the AP controller. The content of the AP boot address update register can be captured and shifted-out of the active boot address shift register from TDO.

The boot address in the boot address shift register and update register are shifted to the right (in the LSB direction) by two bits versus the intended boot address. The reason for this is that the two LSB of the address are not accessible. When this boot address is fed into the AP controller, two 0s are attached in the end as LSB, thereby pushing the shifted-in boot address to the left by two bits, which become the actual AP boot address the AP controller gets.

If you have enabled the remote update feature, the APFC_BOOT_ADDR instruction sets the boot address for the factory configuration only.

The APFC_BOOT_ADDR instruction is retained after reconfiguration while the system board is still powered on. However, you must reprogram the instruction whenever you restart the system board.

Device Configuration Pins

Table 8–18 through Table 8–21 describe the connections and functionality of all the configuration related pins on Cyclone IV devices. Table 8–18 and Table 8–19 list the device pin configuration for the Cyclone IV GX and Cyclone IV E, respectively.

Table 8–18. Configuration Pin Summary for Cyclone IV GX Devices

Bank	Description	Input/Output	Dedicated	Powered By	Configuration Mode
8	Data[4:2]	Input	—	V _{CCIO}	FPP
3	Data[7:5]	Input	—	V _{CCIO}	FPP
9	nCSO (2)	Output	—	V _{CCIO}	AS
3	CRC_ERROR	Output	—	V _{CCIO} /Pull-up (1)	Optional, all modes
9	DATA[0] (2)	Input	Yes	V _{CCIO}	PS, FPP, AS
٥	עסאג [1] (געער (2)	Input		V _{CCIO}	FPP
9	DATA[I]/ASDO (-)	Output		V _{CCIO}	AS
3	INIT_DONE	Output	—	Pull-up	Optional, all modes
3	nSTATUS	Bidirectional	Yes	Pull-up	All modes
9	nCE	Input	Yes	V _{CCIO}	All modes
٥	DCI K (2)	Input	Vac	V _{CCIO}	PS, FPP
9	DCTK (-)	Output	165	V _{CCIO}	AS
3	CONF_DONE	Bidirectional	Yes	Pull-up	All modes
9	TDI	Input	Yes	V _{CCIO}	JTAG
9	TMS	Input	Yes	V _{CCIO}	JTAG
9	ТСК	Input	Yes	V _{CCIO}	JTAG
9	nCONFIG	Input	Yes	V _{CCIO}	All modes
8	CLKUSR	Input	—	V _{CCIO}	Optional
3	nCEO	Output	—	V _{CCIO}	Optional, all modes
3	MSEL	Input	Yes	V _{CCINT}	All modes
9	TDO	Output	Yes	V _{CCIO}	JTAG
6	DEV_OE	Input	—	V _{CCIO}	Optional
6	DEV_CLRn	Input	—	V _{CCIO}	Optional

Notes to Table 8-18:

(1) The CRC_ERROR pin is a dedicated open-drain output or an optional user I/O pin. Active high signal indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled in the Quartus II software from the Error Detection CRC tab of the Device and Pin Options dialog box. When using this pin, connect it to an external 10-kΩ pull-up resistor to an acceptable voltage that satisfies the input voltage of the receiving device.

(2) To tri-state AS configuration pins in the AS configuration scheme, turn on the **Enable input tri-state on active configuration pins in user mode** option from the **Device and Pin Options** dialog box. This tri-states DCLK, nCSO, Data[0], and Data[1]/ASDO pins. Dual-purpose pins settings for these pins are ignored. To set these pins to different settings, turn off the **Enable input tri-state on active configuration pins in user mode** option and set the desired setting from the Dual-purpose Pins Setting menu.

Table 8-19.	Configuration	Pin Summary	for Cyclone	IV E Devices	(Part 1 of 3)
		· · · · ·			· · · · · · · · · · · · · · · · · · ·

Bank	Description	Input/Output	Dedicated	Powered By	Configuration Mode
1	nCSO (1) FLASH_nCE (2)	Output	—	V _{CCIO}	AS, AP
6	CRC_ERROR (3)	Output	—	V _{CCIO} /Pull-up (4)	Optional, all modes

Pin Name	User Mode Configuration Scheme Pin Type		Pin Type	Description					
CONF_DONE	N/A	All	Bidirectional open-drain	 Status output—the target Cyclone IV device drives the CONF_DONE pin low before and during configuration. After all the configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE. Status input—after all the data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an 					
				external 10-kΩ pull-up resistor in order for the device to initialize. Driving CONF_DONE low after configuration and initialization does not affect the configured device. Do not connect hus					
				holds or ADC to CONF_DONE pin.					
nCE	N/A	All	Input	Active-low chip enable. The nCE pin activates the Cyclone IV device with a low signal to allow configuration. You must hold nCE pin low during configuration, initialization, and user-mode. In a single-device configuration, you must tie the nCE pin low. In a multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. You must hold the nCE pin low for successful JTAG programming of the device.					
	N/A if		Output	Output that drives low when configuration is complete. In a single-device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In a multi-device configuration, this pin feeds the nCE pin of the next device. The $nCEO$ of the last device in the chain is left floating or used as a user I/O pin after configuration.					
nCEO	I/O if option is off.	All	open-drain	If you use the nCEO pin to feed the nCE pin of the next device, use an external 10-k Ω pull-up resistor to pull the nCEO pin high to the V _{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor.					
				If you use the nCEO pin as a user I/O pin after configuration, set the state of the pin on the Dual-Purpose Pin settings.					
nCSO,				Output control signal from the Cyclone IV device to the serial configuration device in AS mode that enables the configuration device. This pin functions as nCSO in AS mode and FLASH_nCE in AP mode.					
FLASH_nCE (1)	I/O	AS, AP <i>(2)</i>	Output	Output control signal from the Cyclone IV device to the parallel flash in AP mode that enables the flash. Connects to the $CE\#$ pin on the Micron P30 or P33 flash. ⁽²⁾					
				This pin has an internal pull-up resistor that is always active.					

Table 8-20	. Dedicated	Configuration	Pins on th	ne Cyclone	IV Device	(Part 2 of 4)
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IEEE Std. 1149.6 Boundary-Scan Register

The boundary-scan cell (BSC) for HSSI transmitters ($GXB_TX[p,n]$) and receivers ($GXB_RX[p,n]$) in Cyclone IV GX devices are different from the BSCs for I/O pins.

Figure 10–1 shows the Cyclone IV GX HSSI transmitter boundary-scan cell.





In some applications, it is necessary for a device to wake up very quickly to begin operation. Cyclone IV devices offer the Fast-On feature to support fast wake-up time applications. The MSEL pin settings determine the POR time (t_{POR}) of the device.

- **To** For more information about the MSEL pin settings, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.
- For more information about the POR specifications, refer to the *Cyclone IV Device Datasheet* chapter.

Document Revision History

Table 11–3 lists the revision history for this chapter.

Table 11-3. Document Revision History

Date	Version	Changes
May 2013	1.3	Updated Note (4) in Table 11–1.
		 Updated for the Quartus II software version 10.0 release.
July 2010	1.2	 Updated "I/O Pins Remain Tri-stated During Power-Up" section.
		■ Updated Table 11–1.
February 2010	1.1	Updated Table 11–1 and Table 11–2 for the Quartus II software version 9.1 SP1 release.
November 2009	1.0	Initial release.

Visual Cue	Meaning
	Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. The suffix n denotes an active-low signal. For example, resetn.
Courier type	Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf.
	Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI).
4	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets indicate a list of items when the sequence of the items is not important.
Ĩ	The hand points to information that requires special attention.
0	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
▋┯┫	The multimedia icon directs you to a related multimedia presentation.
CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
VIARNING	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.

The Cyclone IV GX device includes a hard intellectual property (IP) implementation of the PCIe MegaCore[®] functions, supporting Gen1 ×1, ×2, and ×4 initial lane widths configured in the root port or endpoint mode. For more information, refer to "PCI-Express Hard IP Block" on page 1–46.

Transceiver Architecture

Cyclone IV GX devices offer either one or two transceiver blocks per device, depending on the package. Each block consists of four full-duplex (transmitter and receiver) channels, located on the left side of the device (in a die-top view). Figure 1–1 and Figure 1–2 show the die-top view of the transceiver block and related resource locations in Cyclone IV GX devices.





Note to Figure 1–1:

(1) Channel 2 and Channel 3 are not available in the F169 and smaller packages.

There are three methods that you can use to dynamically reconfigure the PMA controls of a transceiver channel:

- "Method 1: Using logical_channel_address to Reconfigure Specific Transceiver Channels" on page 3–14
- "Method 2: Writing the Same Control Signals to Control All the Transceiver Channels" on page 3–16
- "Method 3: Writing Different Control Signals for all the Transceiver Channels at the Same Time" on page 3–19

Method 1: Using logical_channel_address to Reconfigure Specific Transceiver Channels

Enable the logical_channel_address port by selecting the **Use** 'logical_channel_address' port option on the **Analog controls** tab. This method is applicable only for a design where the dynamic reconfiguration controller controls more than one channel.

You can additionally reconfigure either the receiver portion, transmitter portion, or both the receiver and transmitter portions of the transceiver channel by setting the corresponding value on the rx_tx_duplex_sel input port. For more information, refer to Table 3–2 on page 3–4.

Connecting the PMA Control Ports

The selected PMA control ports remain fixed in width, regardless of the number of channels controlled by the ALTGX_RECONFIG instance:

- tx_vodctrl and tx_vodctrl_out are fixed to 3 bits
- tx preemp and tx preemp out are fixed to 5 bits
- rx_eqdcgain and rx_eqdcgain_out are fixed to 2 bits
- rx_eqctrl and rx_eqctrl_out are fixed to 4 bits

Write Transaction

To complete a write transaction, perform the following steps:

- Set the selected PMA control ports to the desired settings (for example, tx_vodctrl = 3'b001).
- 2. Set the logical_channel_address input port to the logical channel address of the transceiver channel whose PMA controls you want to reconfigure.
- 3. Set the rx_tx_duplex_sel port to **2'b10** so that only the transmit PMA controls are written to the transceiver channel.
- 4. Ensure that the busy signal is low before you start a write transaction.
- 5. Assert the write_all signal for one reconfig_clk clock cycle.

The busy output status signal is asserted high to indicate that the dynamic reconfiguration controller is busy writing the PMA control values. When the write transaction has completed, the busy signal goes low.

The .**mif** files carries the reconfiguration information that will be used to reconfigure the multipurpose PLL or general purpose PLL dynamically. The .**mif** contents is generated automatically when you select the **Enable PLL Reconfiguration** option in the **Reconfiguration Setting** in ALTGX instances. The .**mif** files will be generated based on the data rate and input reference clock setting in the ALTGX MegaWizard. You must use the external ROM and feed its content to the ALTPLL_RECONFIG megafunction to reconfigure the multipurpose PLL setting.



Figure 3–16 shows the connection for PLL reconfiguration mode.





Notes to Figure 3-16:

- (1) $\langle n \rangle =$ (number of transceiver PLLs configured in the ALTGX MegaWizard) 1.
- (2) You must connect the pll_reconfig_done signal from the ALTGX to the pll_scandone port from ALTPLL_RECONFIG.

(3) You need two ALTPLL_RECONFIG controllers if you have two separate ALTGX instances with transceiver PLL instantiated in each ALTGX instance.

C For more information about connecting the ALTPLL_RECONFIG and ALTGX instances, refer to the *AN 609: Implementing Dynamic Reconfiguration in Cyclone IV GX Devices*.

***** For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices (1)

I/O Standard	V _{CCIO} (V)			V _{Swing(DC)} (V)		V _{X(AC)} (V)			V _{Swing(AC)} (V)		V _{OX(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V _{CCIO}	$V_{CC10}/2 - 0.2$	_	V _{CCI0} /2 + 0.2	0.7	V _{CCI} 0	V _{CCIO} /2 – 0.125		V _{CCI0} /2 + 0.125
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V _{CCIO}	V _{CCIO} /2 – 0.175	_	V _{CCI0} /2 + 0.175	0.5	V _{CCI} 0	V _{CCIO} /2 – 0.125		V _{CCI0} /2 + 0.125

Note to Table 1-18:

(1) Differential SSTL requires a V_{REF} input.

Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)				V _{DIF(AC)} (V)	
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Mi n	Max	
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.85	_	0.95	0.85		0.95	0.4		
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.71	_	0.79	0.71		0.79	0.4	_	
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO}	$0.48 \times V_{CCIO}$	_	0.52 x V _{CCI0}	0.48 x V _{CCIO}		0.52 x V _{CCI0}	0.3	0.48 x V _{CCI0}	

Note to Table 1-19:

(1) Differential HSTL requires a V_{REF} input.

 Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾ (Part 1 of 2)

1/0 Standard	V _{CCIO} (V)			V _{ID} (mV)			V _{IcM} (V) ⁽²⁾			V _{OD} (mV) ⁽³⁾			V _{0S} (V) ⁽³⁾		
i/U Stanuaru	Min Typ Max		Max	Min	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max	
						0.05	$D_{MAX} \leq 500 \; Mbps$	1.80							
LVPECL (Row I/Os) (6)	2.375	2.5	2.625	100	_	0.55	$\begin{array}{l} 500 \text{ Mbps} \leq \text{ D}_{\text{MAX}} \\ \leq 700 \text{ Mbps} \end{array}$	1.80	_	_	_	_	_	_	
						1.05	D _{MAX} > 700 Mbps	1.55							
			2.625	100		0.05	$D_{MAX} \leq ~500~Mbps$	1.80				_	_	_	
(Column	2.375	2.5				0.55	$\begin{array}{l} 500 \text{ Mbps} \leq \text{D}_{\text{MAX}} \\ \leq 700 \text{ Mbps} \end{array}$	1.80	_	_	_				
1,00)						1.05	D _{MAX} > 700 Mbps	1.55							
						0.05	$D_{MAX} \leq 500 \; Mbps$	1.80				1.125	1.25	1.375	
LVDS (Row I/Os)	2.375	5 2.5	2.625	100	_	0.55	$\begin{array}{l} 500 \mbox{ Mbps} \leq D_{MAX} \\ \leq \mbox{ 700 } \mbox{ Mbps} \end{array}$	1.80	247	_	600				
						1.05	D _{MAX} > 700 Mbps	1.55							