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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	1803
Number of Logic Elements/Cells	28848
Total RAM Bits	608256
Number of I/O	328
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce30f23c9ln

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1. Cyclone IV FPGA Device Family Overview

CYIV-51001-2.0

Altera's new Cyclone® IV FPGA device family extends the Cyclone FPGA series leadership in providing the market's lowest-cost, lowest-power FPGAs, now with a transceiver variant. Cyclone IV devices are targeted to high-volume, cost-sensitive applications, enabling system designers to meet increasing bandwidth requirements while lowering costs.

Built on an optimized low-power process, the Cyclone IV device family offers the following two variants:

- Cyclone IV E—lowest power, high functionality with the lowest cost
- Cyclone IV GX—lowest power and lowest cost FPGAs with 3.125 Gbps transceivers



Cyclone IV E devices are offered in core voltage of 1.0 V and 1.2 V.



For more information, refer to the *Power Requirements for Cyclone IV Devices* chapter.

Providing power and cost savings without sacrificing performance, along with a low-cost integrated transceiver option, Cyclone IV devices are ideal for low-cost, small-form-factor applications in the wireless, wireline, broadcast, industrial, consumer, and communications industries.

Cyclone IV Device Family Features

The Cyclone IV device family offers the following features:

- Low-cost, low-power FPGA fabric:
 - 6K to 150K logic elements
 - Up to 6.3 Mb of embedded memory
 - Up to 360 18 × 18 multipliers for DSP processing intensive applications
 - Protocol bridging applications for under 1.5 W total power

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Table 1–2 lists Cyclone IV GX device resources.

Table 1–2. Resources for the Cyclone IV GX Device Family

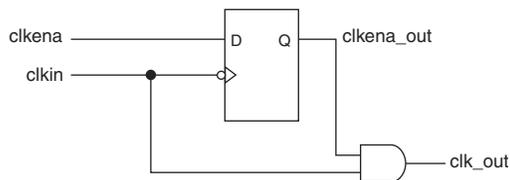
Resources	EP4CGX15	EP4CGX22	EP4CGX30 ⁽¹⁾	EP4CGX30 ⁽²⁾	EP4CGX50 ⁽³⁾	EP4CGX75 ⁽³⁾	EP4CGX110 ⁽³⁾	EP4CGX150 ⁽³⁾
Logic elements (LEs)	14,400	21,280	29,440	29,440	49,888	73,920	109,424	149,760
Embedded memory (Kbits)	540	756	1,080	1,080	2,502	4,158	5,490	6,480
Embedded 18 × 18 multipliers	0	40	80	80	140	198	280	360
General purpose PLLs	1	2	2	4 ⁽⁴⁾	4 ⁽⁴⁾	4 ⁽⁴⁾	4 ⁽⁴⁾	4 ⁽⁴⁾
Multipurpose PLLs	2 ⁽⁵⁾	2 ⁽⁵⁾	2 ⁽⁵⁾	2 ⁽⁵⁾	4 ⁽⁵⁾	4 ⁽⁵⁾	4 ⁽⁵⁾	4 ⁽⁵⁾
Global clock networks	20	20	20	30	30	30	30	30
High-speed transceivers ⁽⁶⁾	2	4	4	4	8	8	8	8
Transceiver maximum data rate (Gbps)	2.5	2.5	2.5	3.125	3.125	3.125	3.125	3.125
PCIe (PIPE) hard IP blocks	1	1	1	1	1	1	1	1
User I/O banks	9 ⁽⁷⁾	9 ⁽⁷⁾	9 ⁽⁷⁾	11 ⁽⁸⁾	11 ⁽⁸⁾	11 ⁽⁸⁾	11 ⁽⁸⁾	11 ⁽⁸⁾
Maximum user I/O ⁽⁹⁾	72	150	150	290	310	310	475	475

Notes to Table 1–2:

- (1) Applicable for the F169 and F324 packages.
- (2) Applicable for the F484 package.
- (3) Only two multipurpose PLLs for F484 package.
- (4) Two of the general purpose PLLs are able to support transceiver clocking. For more information, refer to the *Clock Networks and PLLs in Cyclone IV Devices* chapter.
- (5) You can use the multipurpose PLLs for general purpose clocking when they are not used to clock the transceivers. For more information, refer to the *Clock Networks and PLLs in Cyclone IV Devices* chapter.
- (6) If PCIe ×1, you can use the remaining transceivers in a quad for other protocols at the same or different data rates.
- (7) Including one configuration I/O bank and two dedicated clock input I/O banks for HSSI reference clock input.
- (8) Including one configuration I/O bank and four dedicated clock input I/O banks for HSSI reference clock input.
- (9) The user I/Os count from pin-out files includes all general purpose I/O, dedicated clock pins, and dual purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the pin count.

Figure 5-7 shows how to implement the `clkena` signal with a single register.

Figure 5-7. `clkena` Implementation

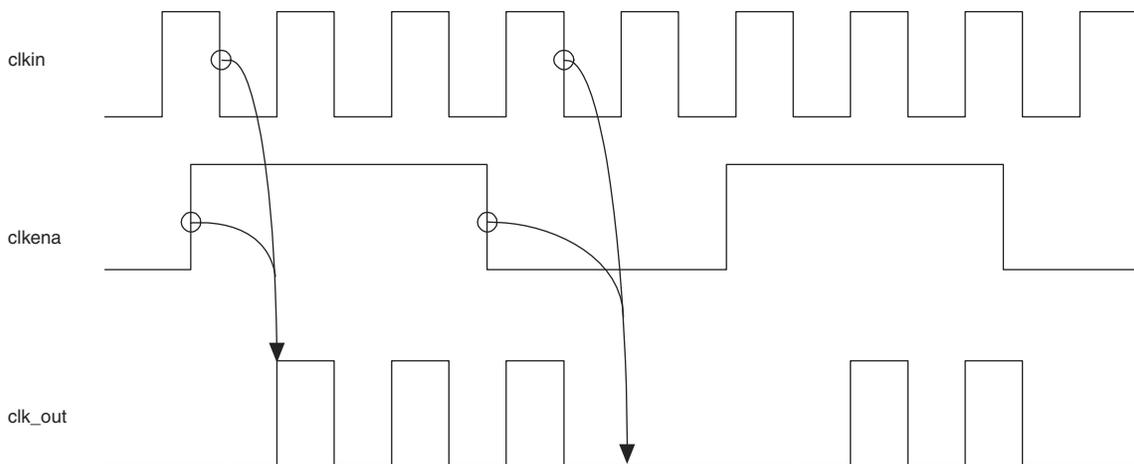


 The `clkena` circuitry controlling the output C0 of the PLL to an output pin is implemented with two registers instead of a single register, as shown in Figure 5-7.

Figure 5-8 shows the waveform example for a clock output enable. The `clkena` signal is sampled on the falling edge of the clock (`clkkin`).

 This feature is useful for applications that require low power or sleep mode.

Figure 5-8. `clkena` Implementation: Output Enable



The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during PLL resynchronization.

Altera recommends using the `clkena` signals when switching the clock source to the PLLs or the GCLK. The recommended sequence is:

1. Disable the primary output clock by de-asserting the `clkena` signal.
2. Switch to the secondary clock using the dynamic select signals of the clock control block.
3. Allow some clock cycles of the secondary clock to pass before reasserting the `clkena` signal. The exact number of clock cycles you must wait before enabling the secondary clock is design-dependent. You can build custom logic to ensure glitch-free transition when switching between different clock sources.

Deterministic Latency Compensation Mode

The deterministic latency mode compensates for the delay of the multipurpose PLLs through the clock network and serializer in Common Public Radio Interface (CPRI) applications. In this mode, the PLL PFD feedback path compensates the latency uncertainty in Tx dataout and Tx clkout paths relative to the reference clock.

Hardware Features

Cyclone IV PLLs support several features for general-purpose clock management. This section discusses clock multiplication and division implementation, phase shifting implementations, and programmable duty cycles.

Clock Multiplication and Division

Each Cyclone IV PLL provides clock synthesis for PLL output ports using $M/(N \times \text{post-scale counter})$ scaling factors. The input clock is divided by a pre-scale factor, N , and is then multiplied by the M feedback factor. The control loop drives the VCO to match $f_{IN} (M/N)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO value is the least common multiple of the output frequencies that meets its frequency specifications. For example, if output frequencies required from one PLL are 33 and 66 MHz, the Quartus II software sets the VCO to 660 MHz (the least common multiple of 33 and 66 MHz in the VCO range). Then, the post-scale counters scale down the VCO frequency for each output port.

There is one pre-scale counter, N , and one multiply counter, M , per PLL, with a range of 1 to 512 for both M and N . The N counter does not use duty cycle control because the purpose of this counter is only to calculate frequency division. There are five generic post-scale counters per PLL that can feed GCLKs or external clock outputs. These post-scale counters range from 1 to 512 with a 50% duty cycle setting. The post-scale counters range from 1 to 256 with any non-50% duty cycle setting. The sum of the high/low count values chosen for a design selects the divide value for a given counter.

The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered into the ALTPLL megafunction.



Phase alignment between output counters is determined using the t_{PLL_PSERR} specification.

Table 6-9. Cyclone IV GX I/O, Differential, and XCVRs Channel Count

Device	4CGX15			4CGX22			4CGX30			4CGX50		4CGX75			4CGX110			4CGX150		
	169-FBGA	169-FBGA	324-FBGA	169-FBGA	324-FBGA	484-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	896-FBGA	484-FBGA	672-FBGA	896-FBGA		
User I/O ⁽³⁾	72	72	150	72	150	290	290	310	290	310	270	393	475	270	393	475				
User I/O banks	9 ⁽⁴⁾	11 ⁽⁵⁾	11 ^{(5), (6)}																	
LVDS ^{(7), (9)}	9	9	16	9	16	45	45	51	45	51	38	52	63	38	52	63				
Emulated LVDS ^{(8), (9)}	16	16	48	16	48	85	85	89	85	89	82	129	157	82	129	157				
XCVRs	2	2	4	2	4	4	4	8	4	8	4	8	8	4	8	8				

Notes to Table 6-9:

- (1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as outputs only.
- (2) For differential pad placement guidelines, refer to “Pad Placement” on page 6-23.
- (3) The I/O pin count includes all GPIOs, dedicated clock pins, and dual-purpose configuration pins. Transceivers pins and dedicated configuration pins are not included in the pin count.
- (4) Includes one configuration I/O bank and two dedicated clock input I/O banks for HSSI input reference clock.
- (5) Includes one configuration I/O bank and four dedicated clock input I/O banks for HSSI input reference clock.
- (6) Single-ended clock input support is available for dedicated clock input I/O banks 3B (pins CLKIO20 and CLKIO22) and 8B (pins CLKIO17 and CLKIO19).
- (7) The true LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in right I/O banks 5 and 6.
- (8) The emulated LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in column I/O banks 3, 4, 7, and 8.
- (9) LVDS input and output buffers are sharing the same p and n pins. One LVDS I/O channel can only be either transmitter or receiver at a time.

High-Speed I/O Standards Support

This section provides information about the high-speed I/O standards and the HSSI input reference clock supported in Cyclone IV devices.

High Speed Serial Interface (HSSI) Input Reference Clock Support

Cyclone IV GX devices support the same I/O features for GPIOs with additional new features where current I/O banks 3A and 8A consist of dual-purpose clock input pins (CLKIN) and 3B and 8B consist of dedicated CLKIN that can be used to support the high-speed transceiver input reference clock (REFCLK) features on top of the general-purpose clock input function.

The EP4CGX15, EP4CGX22, and EP4CGX30 devices contain two pairs of CLKIN/REFCLK pins located in I/O banks 3A and 8A. I/O banks 3B and 8B are not available in EP4CGX15, EP4CGX22, and EP4CGX30 devices. The EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have a total of four pairs of CLKIN/REFCLK pins located in I/O banks 3A, 3B, 8A, and 8B. I/O banks 3B and 8B can also support single-ended clock inputs. For more information about the CLKIN/REFCLK pin location, refer to Figure 6-10 on page 6-18 and Figure 6-11 on page 6-19.

Power-On Reset (POR) Circuit

The POR circuit keeps the device in reset state until the power supply voltage levels have stabilized during device power up. After device power up, the device does not release $nSTATUS$ until V_{CCINT} , V_{CCA} , and V_{CCIO} (for I/O banks in which the configuration and JTAG pins reside) are above the POR trip point of the device. V_{CCINT} and V_{CCA} are monitored for brown-out conditions after device power up.

 V_{CCA} is the analog power to the phase-locked loop (PLL).

In some applications, it is necessary for a device to wake up very quickly to begin operation. Cyclone IV devices offer the fast POR time option to support fast wake-up time applications. The fast POR time option has stricter power-up requirements when compared with the standard POR time option. You can select either the fast option or the standard POR option with the $MSEL$ pin settings.

 If your system exceeds the fast or standard POR time, you must hold $nCONFIG$ low until all the power supplies are stable.

 For more information about the POR specifications, refer to the *Cyclone IV Device Datasheet*.

 For more information about the wake-up time and POR circuit, refer to the *Power Requirements for Cyclone IV Devices* chapter.

Configuration File Size

Table 8–2 lists the approximate uncompressed configuration file sizes for Cyclone IV devices. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

Table 8–2. Uncompressed Raw Binary File (.rbf) Sizes for Cyclone IV Devices (Part 1 of 2)

	Device	Data Size (bits)
Cyclone IV E	EP4CE6	2,944,088
	EP4CE10	2,944,088
	EP4CE15	4,086,848
	EP4CE22	5,748,552
	EP4CE30	9,534,304
	EP4CE40	9,534,304
	EP4CE55	14,889,560
	EP4CE75	19,965,752
	EP4CE115	28,571,696

Table 8-20. Dedicated Configuration Pins on the Cyclone IV Device (Part 4 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
DATA [7..2]	I/O	FPP, AP ⁽²⁾	Inputs (FPP). Bidirectional (AP) ⁽²⁾	In an AS or PS configuration scheme, DATA [7..2] function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA [7..2] are available as user I/O pins and the state of these pin depends on the Dual-Purpose Pin settings. In an AP configuration scheme, for Cyclone IV E devices only, the byte-wide or word-wide configuration data is presented to the target Cyclone IV E device on DATA [7..0] or DATA [15..0], respectively. After AP configuration, DATA [7..2] are dedicated bidirectional pins with optional user control. ⁽²⁾
DATA [15..8]	I/O	AP ⁽²⁾	Bidirectional	Data inputs. Word-wide configuration data is presented to the target Cyclone IV E device on DATA [15..0]. In a PS, FPP, or AS configuration scheme, DATA [15:8] function as user I/O pins during configuration, which means they are tri stated. After AP configuration, DATA [15:8] are dedicated bidirectional pins with optional user control.
PADD [23..0]	I/O	AP ⁽²⁾	Output	In AP mode, it is a 24-bit address bus from the Cyclone IV E device to the parallel flash. Connects to the A[24:1] bus on the Micron P30 or P33 flash.
nRESET	I/O	AP ⁽²⁾	Output	Active-low reset output. Driving the nRESET pin low resets the parallel flash. Connects to the RST# pin on the Micron P30 or P33 flash.
nAVD	I/O	AP ⁽²⁾	Output	Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that a valid address is present on the PADD [23..0] address bus. Connects to the ADV# pin on the Micron P30 or P33 flash.
nOE	I/O	AP ⁽²⁾	Output	Active-low output enable to the parallel flash. During the read operation, driving the nOE pin low enables the parallel flash outputs (DATA [15..0]). Connects to the OE# pin on the Micron P30 or P33 flash.
nWE	I/O	AP ⁽²⁾	Output	Active-low write enable to the parallel flash. During the write operation, driving the nWE pin low indicates to the parallel flash that data on the DATA [15..0] bus is valid. Connects to the WE# pin on the Micron P30 or P33 flash.

Note to Table 8-20:

- (1) If you are accessing the EPCS device with the ALTASML_PARALLEL megafunction or your own user logic in user mode, in the **Device and Pin Options** window of the Quartus II software, in the **Dual-Purpose Pins** category, select **Use as regular I/O** for this pin.
- (2) The AP configuration scheme is for Cyclone IV E devices only.

Configuration error detection determines if the configuration data received through an external memory device is corrupted during configuration. To validate the configuration data, the Quartus® II software uses a function to calculate the CRC value for each configuration data frame and stores the frame-based CRC value in the configuration data as part of the configuration bit stream.

During configuration, Cyclone IV devices use the same methodology to calculate the CRC value based on the frame of data that is received and compares it against the frame CRC value in the data stream. Configuration continues until either the device detects an error or all the values are calculated.

In addition to the frame-based CRC value, the Quartus II software generates a 32-bit CRC value for the whole configuration bit stream. This 32-bit CRC value is stored in the 32-bit storage register at the end of the configuration and is used for user mode error detection that is discussed in “User Mode Error Detection”.

User Mode Error Detection

 User mode error detection is available in Cyclone IV GX and Cyclone IV E devices with 1.2-V core voltage. Cyclone IV E devices with 1.0-V core voltage do not support user mode error detection.

Soft errors are changes in a configuration random-access memory (CRAM) bit state due to an ionizing particle. Cyclone IV devices have built-in error detection circuitry to detect data corruption by soft errors in the CRAM cells.

This error detection capability continuously computes the CRC of the configured CRAM bits based on the contents of the device and compares it with the pre-calculated CRC value obtained at the end of the configuration. If the CRCs match, there is no error in the current configuration CRAM bits. The process of error detection continues until the device is reset (by setting `nCONFIG` to low).

The Cyclone IV device error detection feature does not check memory blocks and I/O buffers. These device memory blocks support parity bits that are used to check the contents of memory blocks for any error. The I/O buffers are not verified during error detection because the configuration data uses flip-flops as storage elements that are more resistant to soft errors. Similar flip-flops are used to store the pre-calculated CRC and other error detection circuitry option bits.

The error detection circuitry in Cyclone IV devices uses a 32-bit CRC IEEE 802 standard and a 32-bit polynomial as the CRC generator. Therefore, a single 32-bit CRC calculation is performed by the device. If a soft error does not occur, the resulting 32-bit signature value is `0x00000000`, that results in a 0 on the `CRC_ERROR` output signal. If a soft error occurs in the device, the resulting signature value is non-zero and the `CRC_ERROR` output signal is 1.

You can inject a soft error by changing the 32-bit CRC storage register in the CRC circuitry. After verifying the induced failure, you can restore the 32-bit CRC value to the correct CRC value with the same instruction and inserting the correct value.

 Before updating it with a known bad value, Altera recommends reading out the correct value.

Table 9-6 lists the estimated time for each CRC calculation with minimum and maximum clock frequencies for Cyclone IV devices.

Table 9-6. CRC Calculation Time

Device		Minimum Time (ms) ⁽¹⁾	Maximum Time (s) ⁽²⁾
Cyclone IV E	EP4CE6 ⁽³⁾	5	2.29
	EP4CE10 ⁽³⁾	5	2.29
	EP4CE15 ⁽³⁾	7	3.17
	EP4CE22 ⁽³⁾	9	4.51
	EP4CE30 ⁽³⁾	15	7.48
	EP4CE40 ⁽³⁾	15	7.48
	EP4CE55 ⁽³⁾	23	11.77
	EP4CE75 ⁽³⁾	31	15.81
	EP4CE115 ⁽³⁾	45	22.67
Cyclone IV GX	EP4CGX15	6	2.93
	EP4CGX22	12	5.95
	EP4CGX30	12	5.95
		34 ⁽⁴⁾	17.34 ⁽⁴⁾
	EP4CGX50	34	17.34
	EP4CGX75	34	17.34
	EP4CGX110	62	31.27
	EP4CGX150	62	31.27

Notes to Table 9-6:

- (1) The minimum time corresponds to the maximum error detection clock frequency and may vary with different processes, voltages, and temperatures (PVT).
- (2) The maximum time corresponds to the minimum error detection clock frequency and may vary with different PVT.
- (3) Only applicable for device with 1.2-V core voltage
- (4) Only applicable for the F484 device package.

Software Support

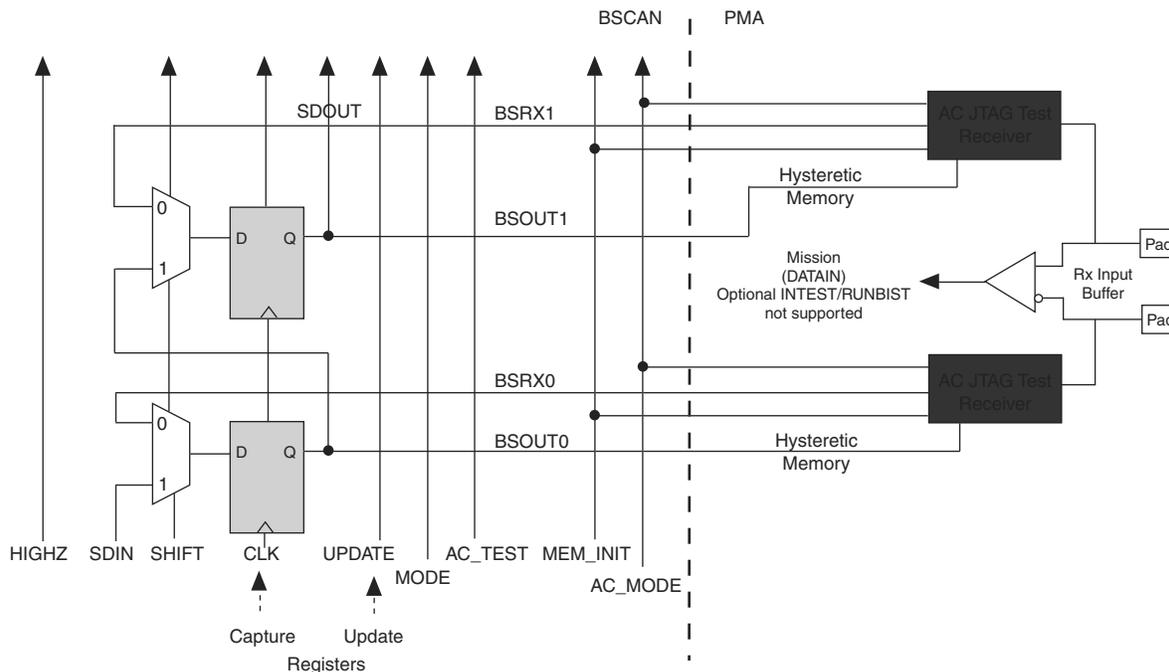
Enabling the CRC error detection feature in the Quartus II software generates the CRC_ERROR output to the optional dual purpose CRC_ERROR pin.

To enable the error detection feature using CRC, perform the following steps:

1. Open the Quartus II software and load a project using Cyclone IV devices.
2. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
3. In the Category list, select **Device**. The **Device** page appears.
4. Click **Device and Pin Options**. The **Device and Pin Options** dialog box appears as shown in Figure 9-2.
5. In the **Device and Pin Options** dialog box, click the **Error Detection CRC** tab.
6. Turn on **Enable error detection CRC**.
7. In the **Divide error check frequency by** box, enter a valid divisor as documented in Table 9-5 on page 9-5.

Figure 10-2 shows the Cyclone IV GX HSSI receiver BSC.

Figure 10-2. HSSI Receiver BSC with IEEE Std. 1149.6 BST Circuitry for the Cyclone IV GX Devices



For more information about Cyclone IV devices user I/O boundary-scan cells, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone III Devices* chapter.

BST Operation Control

Table 10-1 lists the boundary-scan register length for Cyclone IV devices.

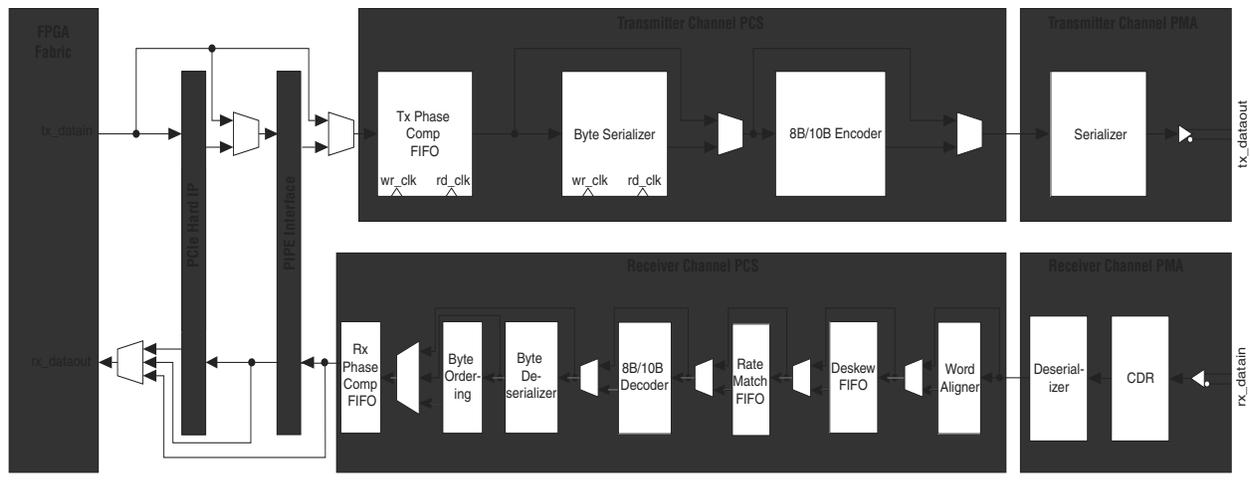
Table 10-1. Boundary-Scan Register Length for Cyclone IV Devices (Part 1 of 2)

Device	Boundary-Scan Register Length
EP4CE6	603
EP4CE10	603
EP4CE15	1080
EP4CE22	732
EP4CE30	1632
EP4CE40	1632
EP4CE55	1164
EP4CE75	1314
EP4CE115	1620
EP4CGX15	260
EP4CGX22	494
EP4CGX30 ⁽¹⁾	494
EP4CGX50	1006

Architectural Overview

Figure 1-3 shows the Cyclone IV GX transceiver channel datapath.

Figure 1-3. Transceiver Channel Datapath for Cyclone IV GX Devices



Each transceiver channel consists of a transmitter and a receiver datapath. Each datapath is further structured into the following:

- Physical media attachment (PMA)—includes analog circuitry for I/O buffers, clock data recovery (CDR), serializer/deserializer (SERDES), and programmable pre-emphasis and equalization to optimize serial data channel performance.
- Physical coding sublayer (PCS)—includes hard logic implementation of digital functionality within the transceiver that is compliant with supported protocols.

Outbound parallel data from the FPGA fabric flows through the transmitter PCS and PMA, is transmitted as serial data. Received inbound serial data flows through the receiver PMA and PCS into the FPGA fabric. The transceiver supports the following interface widths:

- FPGA fabric-transceiver PCS—8, 10, 16, or 20 bits
- PMA-PCS—8 or 10 bits

- The transceiver channel interfaces through the PIPE when configured for PCIe protocol implementation. The PIPE is compliant with version 2.00 of the *PHY Interface for the PCI Express Architecture* specification.

When the byte serializer is enabled, the low-speed clock frequency is halved before feeding into the read clock of TX phase compensation FIFO. The low-speed clock is available in the FPGA fabric as `tx_clkout` port, which can be used in the FPGA fabric to send transmitter data and control signals.

Figure 1–33. Transmitter Only Datapath Clocking in Non-Bonded Channel Configuration

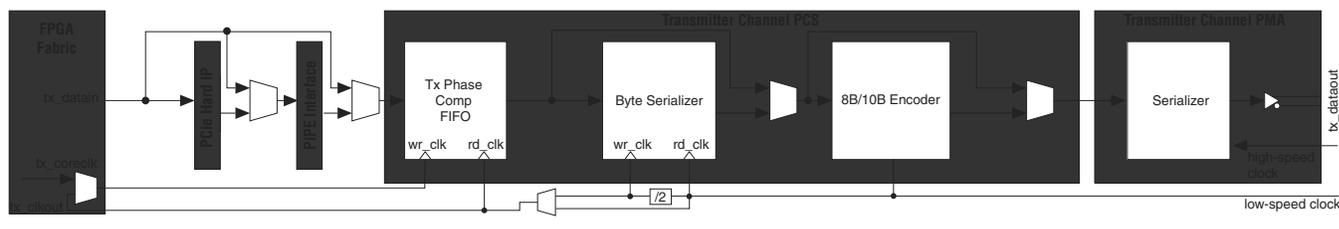
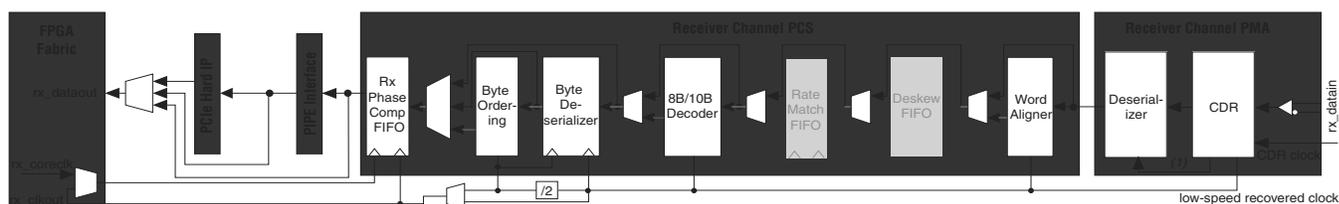


Figure 1–34 shows the datapath clocking in receiver only operation. In this mode, the receiver PCS supports configuration without the rate match FIFO. The CDR unit in the channel recovers the clock from the received serial data and generates the high-speed recovered clock for the deserializer, and low-speed recovered clock for forwarding to the receiver PCS. The low-speed recovered clock feeds to the following blocks in the receiver PCS:

- word aligner
- 8B/10B decoder
- write clock of byte deserializer
- byte ordering
- write clock of RX phase compensation FIFO

When the byte deserializer is enabled, the low-speed recovered clock frequency is halved before feeding into the write clock of the RX phase compensation FIFO. The low-speed recovered clock is available in the FPGA fabric as `rx_clkout` port, which can be used in the FPGA fabric to capture receiver data and status signals.

Figure 1–34. Receiver Only Datapath Clocking without Rate Match FIFO in Non-Bonded Channel Configuration



Note to Figure 1–34:

- (1) High-speed recovered clock.

When the transceiver is configured for transmitter and receiver operation in non-bonded channel configuration, the receiver PCS supports configuration with and without the rate match FIFO. The difference is only at the receiver datapath clocking. The transmitter datapath clocking is identical to transmitter only operation mode as shown in Figure 1–33.

Table 3-5. rx_dataoutfull[31..0] FPGA Fabric-Transceiver Channel Interface Signal Descriptions (Part 3 of 3)

FPGA Fabric-Transceiver Channel Interface Description	Receive Signal Description (Based on Cyclone IV GX Supported FPGA Fabric-Transceiver Channel Interface Widths)
20-bit FPGA fabric-Transceiver Channel Interface with PCS-PMA set to 10 bits	Two 10-bit Data (rx_dataout) rx_dataoutfull[9:0] - rx_dataout (LSByte) and rx_dataoutfull[25:16] - rx_dataout (MSByte)
	Two Receiver Sync Status Bits rx_dataoutfull[10] - rx_syncstatus (LSB) and rx_dataoutfull[26] - rx_syncstatus (MSB)
	rx_dataoutfull[11] and rx_dataoutfull[27]: 8B/10B disparity error indicator (rx_disperr)
	Two Receiver Pattern Detect Bits rx_dataoutfull[12] - rx_patterndetect (LSB) and rx_dataoutfull[28] - rx_patterndetect (MSB)
	rx_dataoutfull[13] and rx_dataoutfull[29]: Rate Match FIFO deletion status indicator (rx_rmfifodatadeleted) in non-PCI Express (PIPE) functional modes
	rx_dataoutfull[14] and rx_dataoutfull[30]: Rate Match FIFO insertion status indicator (rx_rmfifodatainserted) in non-PCI Express (PIPE) functional modes
	rx_dataoutfull[15] and rx_dataoutfull[31]: 8B/10B running disparity indicator (rx_runningdisp)

Data Rate Reconfiguration Mode Using RX Local Divider

The RX local divider resides in the RX PMA block for every channels. This is a hardware feature where a /2 divider is available in each of the receiver channel for the supported device. You can use this RX local divider to reconfigure the data rate at the receiver channel. This can be used for protocols such as SDI that has data rates in divisions of 2.

By using this RX local divider, you can support two different data rates without using additional transceiver PLLs. This dynamic reconfiguration mode is available only for the receiver and not applicable to the transmitter. This reconfiguration mode using the RX local divider (/2) is only supported and available in EP4CGX30 (F484 package), EP4CGX50, and EP4CGX75 devices.



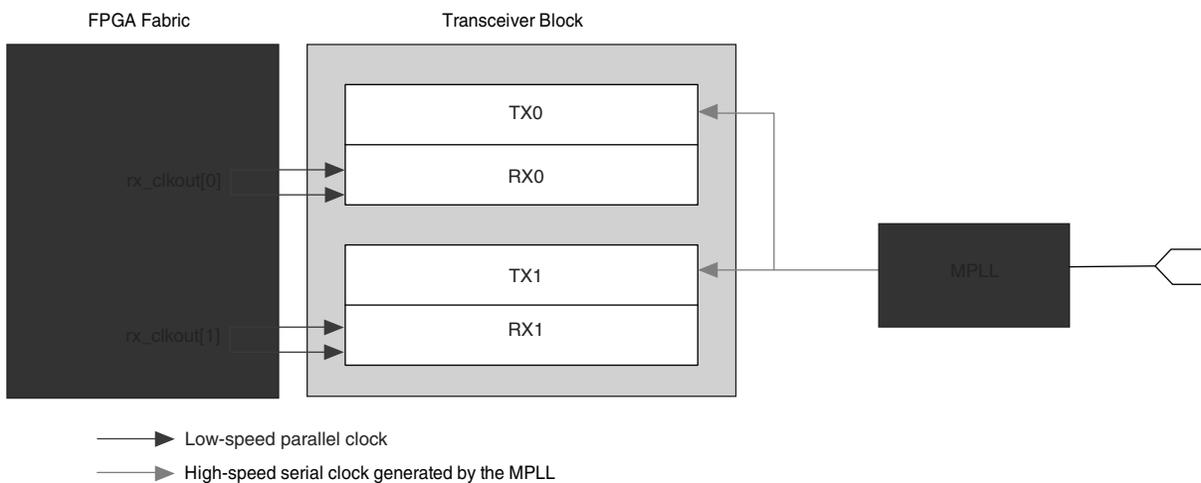
For more information about this RX local divider, refer to the *Cyclone IV GX Transceiver Architecture* chapter.

Option 3: Use the Respective Channel Receiver Core Clocks

- Enable this option if you want the individual channel's rx_clkout signal to provide the read clock to its respective Receive Phase Compensation FIFO.
- This option is typically enabled when the channel is reconfigured from a Basic or Protocol configuration with or without rate matching to another Basic or Protocol configuration with or without rate matching.

Figure 3–15 shows the respective rx_clkout of each channel clocking the respective receiver channels of a transceiver block.

Figure 3–15. Option 3 for Receiver Core Clocking (Channel Reconfiguration Mode)



PLL Reconfiguration Mode

Cyclone IV GX device support the PLL reconfiguration support through the ALTPLL_RECONFIG MegaWizard. You can use this mode to reconfigure the multipurpose PLL or general purpose PLL used to clock the transceiver channel without affecting the remaining blocks of the channel. When you reconfigure the multipurpose PLL or general purpose PLL of a transceiver block to run at a different data rate, all the transceiver channels listening to this multipurpose PLL or general purpose PLL also get reconfigured to the new data rate. Channel settings are not affected. When you reconfigure the multipurpose PLL or general purpose PLL to support a different data rate, you must ensure that the functional mode of the transceiver channel supports the reconfigured data rate.

The PLL reconfiguration mode can be enabled by selecting the **Enable PLL Reconfiguration** option in the ALTGX MegaWizard under **Reconfiguration Setting** tab. For multipurpose PLL or general purpose PLL reconfiguration, **.mif** files are required to dynamically reconfigure the PLL setting in order to change the output frequency of the transceiver PLL to support different data rates.

Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA_GXB}	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
V_I	DC input voltage	—	-0.5	—	3.6	V
V_O	DC output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	-40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) ⁽⁷⁾	50 μ s	—	50 ms	—
		Fast POR ⁽⁸⁾	50 μ s	—	3 ms	—
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1-4:

- All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.
- Power supplies must rise monotonically.
- V_{CCIO} for all I/O banks must be powered up during device operation. Configuration pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- You must set V_{CC_CLKIN} to 2.5 V if you use $CLKIN$ as a high-speed serial interface (HSSI) $refclk$ or as a $DIFFCLK$ input.
- The $CLKIN$ pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1-5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V_{ESDHBM}	ESD voltage using the HBM (GPIOs) ⁽¹⁾	± 2000	V
	ESD using the HBM (HSSI I/Os) ⁽²⁾	± 1000	V
V_{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) ⁽²⁾	± 250	V

Notes to Table 1-5:

- The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ± 1000 V.
- This value is applicable only to Cyclone IV GX devices.

Table 1-21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (F324 and smaller package) ⁽¹⁵⁾	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package) ⁽¹⁵⁾	—	600	—	3125	600	—	3125	600	—	2500	Mbps
Absolute V _{MAX} for a receiver pin ⁽³⁾	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V _{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V _{MIN} for a receiver pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage V _{ID} (diff p-p)	V _{ICM} = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps	0.1	—	2.7	0.1	—	2.7	0.1	—	2.7	V
V _{ICM}	V _{ICM} = 0.82 V setting	—	820 ± 10%	—	—	820 ± 10%	—	—	820 ± 10%	—	mV
Differential on-chip termination resistors	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI	Compliant									—
Programmable ppm detector ⁽⁴⁾	—	± 62.5, 100, 125, 200, 250, 300									ppm
Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)	—	—	—	±300 ⁽⁵⁾ , ±350 ^{(6), (7)}	—	—	±300 ⁽⁵⁾ , ±350 ^{(6), (7)}	—	—	±300 ⁽⁵⁾ , ±350 ^{(6), (7)}	ppm
CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) ⁽⁸⁾	—	—	—	350 to -5350 ^{(7), (9)}	—	—	350 to -5350 ^{(7), (9)}	—	—	350 to -5350 ^{(7), (9)}	ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	No Equalization	—	—	1.5	—	—	1.5	—	—	1.5	dB
	Medium Low	—	—	4.5	—	—	4.5	—	—	4.5	dB
	Medium High	—	—	5.5	—	—	5.5	—	—	5.5	dB
	High	—	—	7	—	—	7	—	—	7	dB

