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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                               |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                        |
| Number of LABs/CLBs            | 1803                                                                                                                          |
| Number of Logic Elements/Cells | 28848                                                                                                                         |
| Total RAM Bits                 | 608256                                                                                                                        |
| Number of I/O                  | 328                                                                                                                           |
| Number of Gates                | -                                                                                                                             |
| Voltage - Supply               | 1.15V ~ 1.25V                                                                                                                 |
| Mounting Type                  | Surface Mount                                                                                                                 |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                            |
| Package / Case                 | 484-BGA                                                                                                                       |
| Supplier Device Package        | 484-FBGA (23x23)                                                                                                              |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/ep4ce30f23i7">https://www.e-xfl.com/product-detail/intel/ep4ce30f23i7</a> |

# Package Matrix

Table 1–3 lists Cyclone IV E device package offerings.

**Table 1–3. Package Offerings for the Cyclone IV E Device Family <sup>(1)</sup>, <sup>(2)</sup>**

| Package    | E144     |                     | M164     |                     | M256     |                     | U256     |                     | F256     |                     | F324     |                     | U484     |                     | F484     |                     | F780     |                     |
|------------|----------|---------------------|----------|---------------------|----------|---------------------|----------|---------------------|----------|---------------------|----------|---------------------|----------|---------------------|----------|---------------------|----------|---------------------|
| Size (mm)  | 22 × 22  |                     | 8 × 8    |                     | 9 × 9    |                     | 14 × 14  |                     | 17 × 17  |                     | 19 × 19  |                     | 19 × 19  |                     | 23 × 23  |                     | 29 × 29  |                     |
| Pitch (mm) | 0.5      |                     | 0.5      |                     | 0.5      |                     | 0.8      |                     | 1.0      |                     | 1.0      |                     | 0.8      |                     | 1.0      |                     | 1.0      |                     |
| Device     | User I/O | LVDS <sup>(3)</sup> | User I/O | LVDS <sup>(3)</sup> | User I/O | LVDS <sup>(3)</sup> | User I/O | LVDS <sup>(3)</sup> | User I/O | LVDS <sup>(3)</sup> | User I/O | LVDS <sup>(3)</sup> | User I/O | LVDS <sup>(3)</sup> | User I/O | LVDS <sup>(3)</sup> | User I/O | LVDS <sup>(3)</sup> |
| EP4CE6     | ↑91      | 21                  | —        | —                   | —        | —                   | ↑179     | 66                  | ↑179     | 66                  | —        | —                   | —        | —                   | —        | —                   | —        | —                   |
| EP4CE10    | ↑91      | 21                  | —        | —                   | —        | —                   | ↑179     | 66                  | ↑179     | 66                  | —        | —                   | —        | —                   | —        | —                   | —        | —                   |
| EP4CE15    | ↓81      | 18                  | 89       | 21                  | 165      | 53                  | ↓165     | 53                  | ↓165     | 53                  | —        | —                   | —        | —                   | ↑343     | 137                 | —        | —                   |
| EP4CE22    | ↓79      | 17                  | —        | —                   | —        | —                   | ↓153     | 52                  | ↓153     | 52                  | —        | —                   | —        | —                   | —        | —                   | —        | —                   |
| EP4CE30    | —        | —                   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | ↑193     | 68                  | —        | —                   | ↑328     | 124                 | ↑532     | 224                 |
| EP4CE40    | —        | —                   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | ↓193     | 68                  | ↑328     | 124                 | ↑328     | 124                 | ↑532     | 224                 |
| EP4CE55    | —        | —                   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | ↓324     | 132                 | ↑324     | 132                 | ↑374     | 160                 |
| EP4CE75    | —        | —                   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | ↓292     | 110                 | ↑292     | 110                 | ↑426     | 178                 |
| EP4CE115   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | —        | —                   | ↓280     | 103                 | ↓528     | 230                 |

**Notes to Table 1–3:**

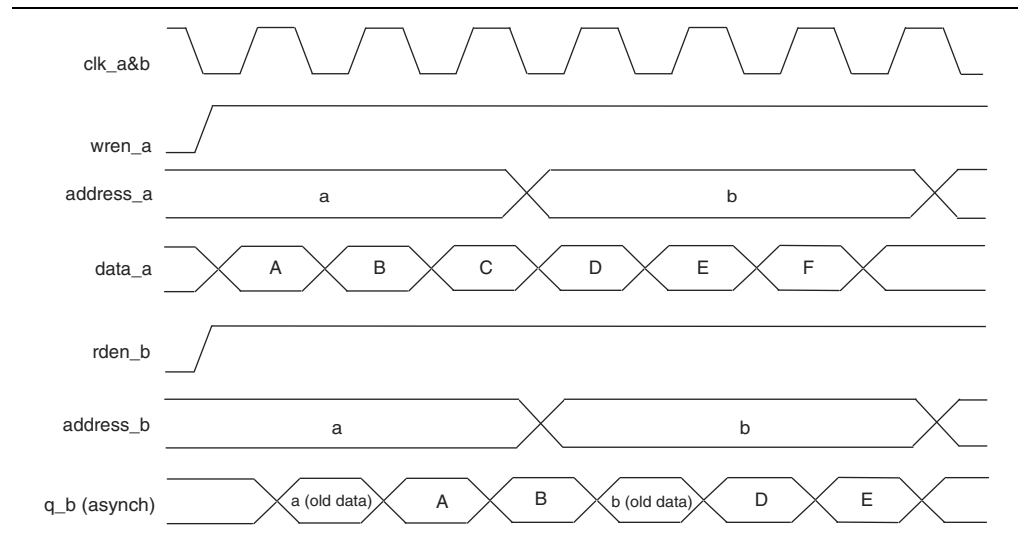
- (1) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane of your PCB. Use this exposed pad for electrical connectivity and not for thermal purposes.
- (2) Use the Pin Migration View window in Pin Planner of the Quartus II software to verify the pin migration compatibility when you perform device migration. For more information, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.
- (3) This includes both dedicated and emulated LVDS pairs. For more information, refer to the *I/O Features in Cyclone IV Devices* chapter.

In this mode, you also have two output choices: **Old Data** mode or **Don't Care** mode. In **Old Data** mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In **Don't Care** mode, the same operation results in a “Don't Care” or unknown value on the RAM outputs.

For more information about how to implement the desired behavior, refer to the *RAM Megafunction User Guide*.

Figure 3-16 shows a sample functional waveform of mixed port read-during-write behavior for **Old Data** mode. In **Don't Care** mode, the old data is replaced with “Don't Care”.

**Figure 3-16. Mixed Port Read-During-Write: Old Data Mode**



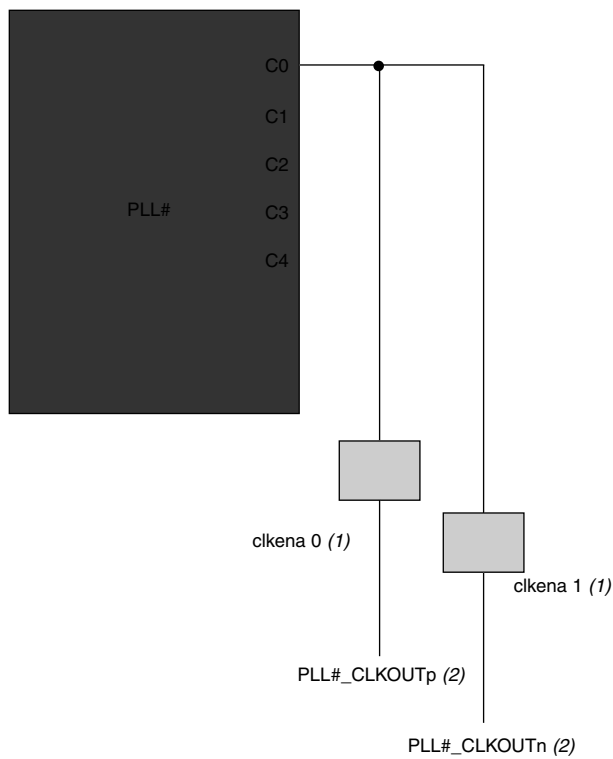
For mixed-port read-during-write operation with dual clocks, the relationship between the clocks determines the output behavior of the memory. If you use the same clock for the two clocks, the output is the old data from the address location. However, if you use different clocks, the output is unknown during the mixed-port read-during-write operation. This unknown value may be the old or new data at the address location, depending on whether the read happens before or after the write.

## Conflict Resolution

When you are using M9K memory blocks in true dual-port mode, it is possible to attempt two write operations to the same memory location (address). Because there is no conflict resolution circuitry built into M9K memory blocks, this results in unknown data being written to that location. Therefore, you must implement conflict-resolution logic external to the M9K memory block.

Figure 5–11 shows the external clock outputs for PLLs.

**Figure 5–11. External Clock Outputs for PLLs**



**Notes to Figure 5–11:**

- (1) These external clock enable signals are available only when using the ALTCLKCTRL megafunction.
- (2) `PLL#_CLKOUTp` and `PLL#_CLKOUTn` pins are dual-purpose I/O pins that you can use as one single-ended clock output or one differential clock output. When using both pins as single-ended I/Os, one of them can be the clock output while the other pin is configured as a regular user I/O.

Each pin of a differential output pair is 180° out of phase. The Quartus II software places the NOT gate in your design into the I/O element to implement 180° phase with respect to the other pin in the pair. The clock output pin pairs support the same I/O standards as standard output pins.



To determine which I/O standards are supported by the PLL clock input and output pins, refer to the *Cyclone IV Device I/O Features* chapter.

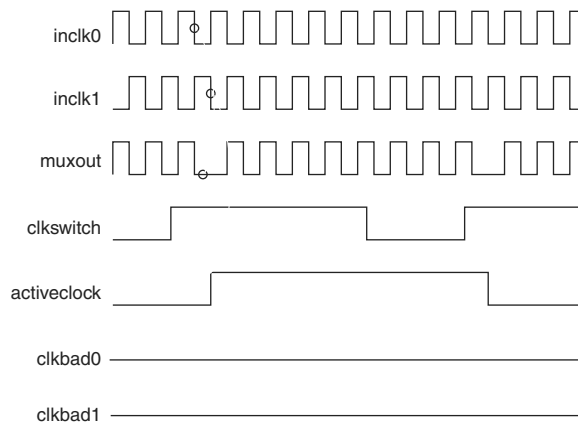
Cyclone IV PLLs can drive out to any regular I/O pin through the GCLK. You can also use the external clock output pins as GPIO pins if external PLL clocking is not required.

In this mode, the `activeclock` signal mirrors the `clkswitch` signal. As both blocks are still functional during the manual switch, neither `clkbad` signals go high. Because the switchover circuit is positive edge-sensitive, the falling edge of the `clkswitch` signal does not cause the circuit to switch back from `inclk1` to `inclk0`. When the `clkswitch` signal goes high again, the process repeats. The `clkswitch` signal and the automatic switch only works depending on the availability of the clock that is switched to. If the clock is unavailable, the state machine waits until the clock is available.



When `CLKSWITCH = 1`, it overrides the automatic switch-over function. As long as `clkswitch` signal is high, further switch-over action is blocked.

**Figure 5–19. Clock Switchover Using the `clkswitch` Control <sup>(1)</sup>**



**Note to Figure 5–19:**

(1) Both `inclk0` and `inclk1` must be running when the `clkswitch` signal goes high to start a manual clock switchover event.

## Manual Clock Switchover

PLLs of Cyclone IV devices support manual switchover, in which the `clkswitch` signal controls whether `inclk0` or `inclk1` is the input clock to the PLL. The characteristics of a manual switchover are similar to the manual override feature in an automatic clock switchover, in which the switchover circuit is edge-sensitive. When the `clkswitch` signal goes high, the switchover sequence starts. The falling edge of the `clkswitch` signal does not cause the circuit to switch back to the previous input clock.



For more information about PLL software support in the Quartus II software, refer to the *ALTPLL Megafunction User Guide*.

## Guidelines

Use the following guidelines to design with clock switchover in PLLs:

- Clock loss detection and automatic clock switchover require the `inclk0` and `inclk1` frequencies be within 20% of each other. Failing to meet this requirement causes the `clkbad0` and `clkbad1` signals to function improperly.

## Programmable Bandwidth

The PLL bandwidth is the measure of the PLL's ability to track the input clock and its associated jitter. PLLs of Cyclone IV devices provide advanced control of the PLL bandwidth using the programmable characteristics of the PLL loop, including loop filter and charge pump. The closed-loop gain 3-dB frequency in the PLL determines the PLL bandwidth. The bandwidth is approximately the unity gain point for open loop PLL response.

## Phase Shift Implementation

Phase shift is used to implement a robust solution for clock delays in Cyclone IV devices. Phase shift is implemented with a combination of the VCO phase output and the counter starting time. The VCO phase output and counter starting time are the most accurate methods of inserting delays, because they are based only on counter settings that are independent of process, voltage, and temperature.

You can phase shift the output clocks from the PLLs of Cyclone IV devices in one of two ways:

- Fine resolution using VCO phase taps
- Coarse resolution using counter starting time

Fine resolution phase shifts are implemented by allowing any of the output counters (C[4..0]) or the M counter to use any of the eight phases of the VCO as the reference clock. This allows you to adjust the delay time with a fine resolution.

Equation 5-1 shows the minimum delay time that you can insert using this method.

### Equation 5-1. Fine Resolution Phase Shift

$$\Phi_{\text{fine}} = \frac{T_{\text{VCO}}}{8} = \frac{1}{8f_{\text{VCO}}} = \frac{N}{8Mf_{\text{REF}}}$$

in which  $f_{\text{REF}}$  is the input reference clock frequency.

For example, if  $f_{\text{REF}}$  is 100 MHz,  $N = 1$ , and  $M = 8$ , then  $f_{\text{VCO}} = 800$  MHz, and  $\Phi_{\text{fine}} = 156.25$  ps. The PLL operating frequency defines this phase shift, a value that depends on reference clock frequency and counter settings.

Coarse resolution phase shifts are implemented by delaying the start of the counters for a predetermined number of counter clocks. Equation 5-2 shows the coarse phase shift.

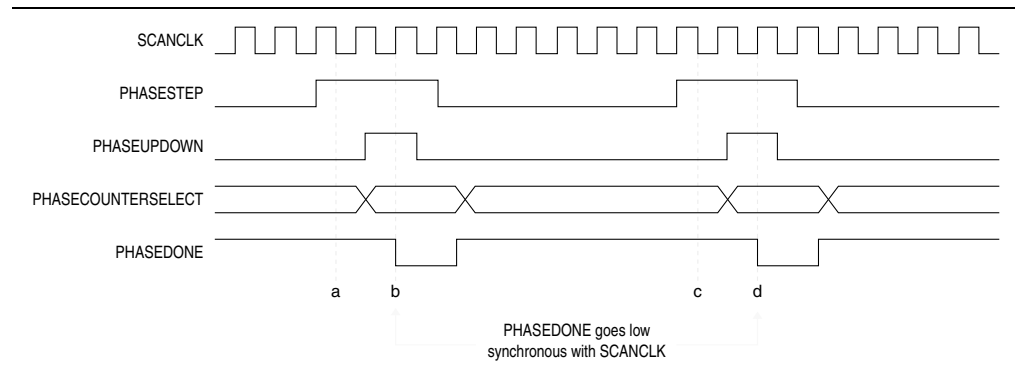
### Equation 5-2. Coarse Resolution Phase Shift

$$\Phi_{\text{coarse}} = \frac{C-1}{f_{\text{VCO}}} = \frac{(C-1)N}{Mf_{\text{REF}}}$$

$C$  is the count value set for the counter delay time (this is the initial setting in the PLL usage section of the compilation report in the Quartus II software). If the initial value is 1,  $C - 1 = 0^\circ$  phase shift.

Figure 5-26 shows the dynamic phase shifting waveform.

**Figure 5-26. PLL Dynamic Phase Shift**



The PHASESTEP signal is latched on the negative edge of SCANCLK (a,c) and must remain asserted for at least two SCANCLK cycles. Deassert PHASESTEP after PHASEDONE goes low. On the second SCANCLK rising edge (b,d) after PHASESTEP is latched, the values of PHASEUPDOWN and PHASECOUNTERSELECT are latched and the PLL starts dynamic phase-shifting for the specified counters, and in the indicated direction. PHASEDONE is deasserted synchronous to SCANCLK at the second rising edge (b,d) and remains low until the PLL finishes dynamic phase-shifting. Depending on the VCO and SCANCLK frequencies, PHASEDONE low time may be greater than or less than one SCANCLK cycle.

You can perform another dynamic phase-shift after the PHASEDONE signal goes from low to high. Each PHASESTEP pulse enables one phase shift. PHASESTEP pulses must be at least one SCANCLK cycle apart.



For information about the ALTPLL\_RECONFIG MegaWizard™ Plug-In Manager, refer to the *ALTPLL\_RECONFIG Megafunction User Guide*.

## Spread-Spectrum Clocking

Cyclone IV devices can accept a spread-spectrum input with typical modulation frequencies. However, the device cannot automatically detect that the input is a spread-spectrum signal. Instead, the input signal looks like deterministic jitter at the input of the PLL. PLLs of Cyclone IV devices can track a spread-spectrum input clock as long as it is in the input jitter tolerance specifications and the modulation frequency of the input clock is below the PLL bandwidth, that is specified in the fitter report. Cyclone IV devices cannot generate spread-spectrum signals internally.

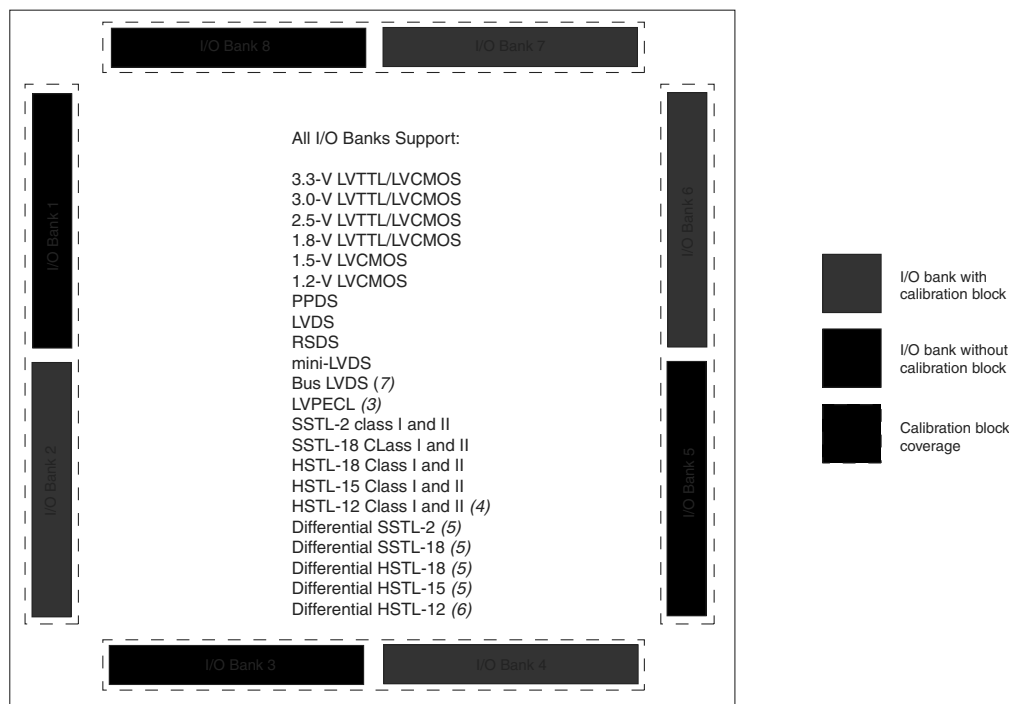
## PLL Specifications



For information about PLL specifications, refer to the *Cyclone IV Device Datasheet* chapter.

Figure 6-9 shows the overview of Cyclone IV E I/O banks.

**Figure 6-9. Cyclone IV E I/O Banks (1), (2)**



**Notes to Figure 6-9:**

- (1) This is a top view of the silicon die. This is only a graphical representation. For exact pin locations, refer to the pin list and the Quartus II software.
- (2) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only. External resistors are needed for the differential outputs in column I/O banks.
- (3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
- (4) The HSTL-12 Class II is supported in column I/O banks 3, 4, 7, and 8 only.
- (5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. Differential SSTL-18, differential HSTL-18, and HSTL-15 I/O standards do not support Class II output.
- (6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 3, 4, 7, and 8.
- (7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses true LVDS input buffer.

When designing LVTTL/LVCMOS inputs with Cyclone IV devices, refer to the following guidelines:

- All pins accept input voltage ( $V_I$ ) up to a maximum limit (3.6 V), as stated in the recommended operating conditions provided in the *Cyclone IV Device Datasheet* chapter.
- Whenever the input level is higher than the bank  $V_{CCIO}$ , expect higher leakage current.
- The LVTTL/LVCMOS I/O standard input pins can only meet the  $V_{IH}$  and  $V_{IL}$  levels according to bank voltage level.

Voltage-referenced standards are supported in an I/O bank using any number of single-ended or differential standards, as long as they use the same  $V_{REF}$  and  $V_{CCIO}$  values. For example, if you choose to implement both SSTL-2 and SSTL-18 in your Cyclone IV devices, I/O pins using these standards—because they require different  $V_{REF}$  values—must be in different banks from each other. However, the same I/O bank can support SSTL-2 and 2.5-V LVCMOS with the  $V_{CCIO}$  set to 2.5 V and the  $V_{REF}$  set to 1.25 V.

 When using Cyclone IV devices as a receiver in 3.3-, 3.0-, or 2.5-V LVTTL/LVCMOS systems, you are responsible for managing overshoot or undershoot to stay in the absolute maximum ratings and the recommended operating conditions, provided in the *Cyclone IV Device Datasheet* chapter.

 The PCI clamping diode is enabled by default in the Quartus II software for input signals with bank  $V_{CCIO}$  at 2.5, 3.0, or 3.3 V.

## High-Speed Differential Interfaces

Cyclone IV devices can send and receive data through LVDS signals. For the LVDS transmitter and receiver, the input and output pins of Cyclone IV devices support serialization and deserialization through internal logic.

The BLVDS extends the benefits of LVDS to multipoint applications such as bidirectional backplanes. The loading effect and the need to terminate the bus at both ends for multipoint applications require BLVDS to drive out a higher current than LVDS to produce a comparable voltage swing. All the I/O banks of Cyclone IV devices support BLVDS for user I/O pins.

The RSDS and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI).

The PPDS standard is the next generation of the RSDS standard introduced by National Semiconductor Corporation. Cyclone IV devices meet the National Semiconductor Corporation PPDS Interface Specification and support the PPDS standard for outputs only. All the I/O banks of Cyclone IV devices support the PPDS standard for output pins only.

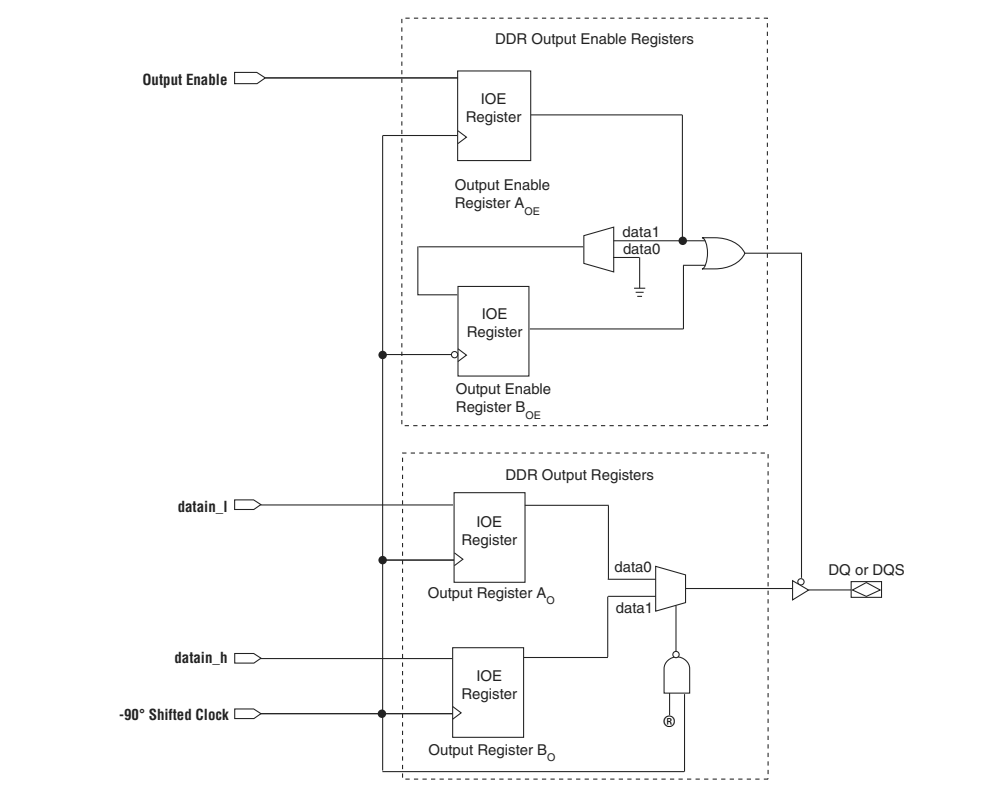
The LVDS standard does not require an input reference voltage, but it does require a 100- $\Omega$  termination resistor between the two signals at the input buffer. An external resistor network is required on the transmitter side for the top and bottom I/O banks.

## DDR Output Registers

A dedicated write DDIO block is implemented in the DDR output and output enable paths.

Figure 7-8 shows how a Cyclone IV dedicated write DDIO block is implemented in the I/O element (IOE) registers.

**Figure 7-8. Cyclone IV Dedicated Write DDIO**



The two DDR output registers are located in the I/O element (IOE) block. Two serial data streams routed through `datain_l` and `datain_h`, are fed into two registers, output register `AO` and output register `BO`, respectively, on the same clock edge. The output from output register `AO` is captured on the falling edge of the clock, while the output from output register `BO` is captured on the rising edge of the clock. The registered outputs are multiplexed by the common clock to drive the DDR output pin at twice the data rate.

The DDR output enable path has a similar structure to the DDR output path in the IOE block. The second output enable register provides the write preamble for the `DQS` strobe in DDR external memory interfaces. This active-low output enable register extends the high-impedance state of the pin by half a clock cycle to provide the external memory's `DQS` write preamble time specification.



For more information about Cyclone IV IOE registers, refer to the *Cyclone IV Device I/O Features* chapter.

## Programming Parallel Flash Memories

Supported parallel flash memories are external non-volatile configuration devices. They are industry standard microprocessor flash memories. For more information about the supported families for the commodity parallel flash, refer to Table 8-10 on page 8-22.

Cyclone IV E devices in a single- or multiple-device chain support in-system programming of a parallel flash using the JTAG interface with the flash loader megafunction. The board intelligent host or download cable uses the four JTAG pins on Cyclone IV E devices to program the parallel flash in system, even if the host or download cable cannot access the configuration pins of the parallel flash.

-  For more information about using the JTAG pins on Cyclone IV E devices to program the parallel flash in-system, refer to *AN 478: Using FPGA-Based Parallel Flash Loader (PFL) with the Quartus II Software*.

In the AP configuration scheme, the default configuration boot address is 0x010000 when represented in 16-bit word addressing in the supported parallel flash memory (Figure 8-12). In the Quartus II software, the default configuration boot address is 0x020000 because it is represented in 8-bit byte addressing. Cyclone IV E devices configure from word address 0x010000, which is equivalent to byte address 0x020000.

-  The Quartus II software uses byte addressing for the default configuration boot address. You must set the start address field to **0x020000**.

This chapter provides additional information about the document and Altera.

## About this Handbook

This handbook provides comprehensive information about the Altera® Cyclone® IV family of devices.

## How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

| Contact <sup>(1)</sup>                                 | Contact Method | Address                   |
|--------------------------------------------------------|----------------|---------------------------|
| Technical support                                      | Website        | www.altera.com/support    |
| Technical training                                     | Website        | www.altera.com/training   |
|                                                        | Email          | custrain@altera.com       |
| Product literature                                     | Website        | www.altera.com/literature |
| Nontechnical support (general)<br>(software licensing) | Email          | nacomp@altera.com         |
|                                                        | Email          | authorization@altera.com  |

**Note to Table:**

(1) You can also contact your local Altera sales office or sales representative.

## Typographic Conventions

The following table shows the typographic conventions this document uses.

| Visual Cue                                      | Meaning                                                                                                                                                                                                                |
|-------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Bold Type with Initial Capital Letters</b>   | Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, <b>Save As</b> dialog box. For GUI elements, capitalization matches the GUI.                                         |
| <b>bold type</b>                                | Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, \qdesigns directory, <b>D:</b> drive, and <b>chiptrip.gdf</b> file. |
| <i>Italic Type with Initial Capital Letters</i> | Indicate document titles. For example, <i>Stratix IV Design Guidelines</i> .                                                                                                                                           |
| <i>italic type</i>                              | Indicates variables. For example, $n + 1$ .<br>Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>.pdf file.                                                              |
| Initial Capital Letters                         | Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.                                                                                                                               |
| "Subheading Title"                              | Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."                                                                            |

This section provides a complete overview of all features relating to the Cyclone® IV device transceivers. This section includes the following chapters:

- Chapter 1, Cyclone IV Transceivers Architecture
- Chapter 2, Cyclone IV Reset Control and Power Down
- Chapter 3, Cyclone IV Dynamic Reconfiguration

## Revision History

Refer to the chapter for its own specific revision history. For information about when the chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.



Table 1–4 lists the synchronization state machine parameters for the word aligner in this mode.

**Table 1–4. Synchronization State Machine Parameters**

| Parameter                                                                       | Allowed Values |
|---------------------------------------------------------------------------------|----------------|
| Number of erroneous code groups received to lose synchronization                | 1–64           |
| Number of continuous good code groups received to reduce the error count by one | 1–256          |

After deassertion of the `rx_digitalreset` signal in automatic synchronization state machine mode, the word aligner starts looking for the synchronization code groups, word alignment pattern or its complement in the received data stream. When the programmed number of valid synchronization code groups or ordered sets are received, the `rx_syncstatus` signal is driven high to indicate that synchronization is acquired. The `rx_syncstatus` signal is constantly driven high until the programmed number of erroneous code groups are received without receiving intermediate good groups; after which the `rx_syncstatus` signal is driven low. The word aligner indicates loss of synchronization (`rx_syncstatus` signal remains low) until the programmed number of valid synchronization code groups are received again.

In addition to restoring word boundaries, the word aligner supports the following features:

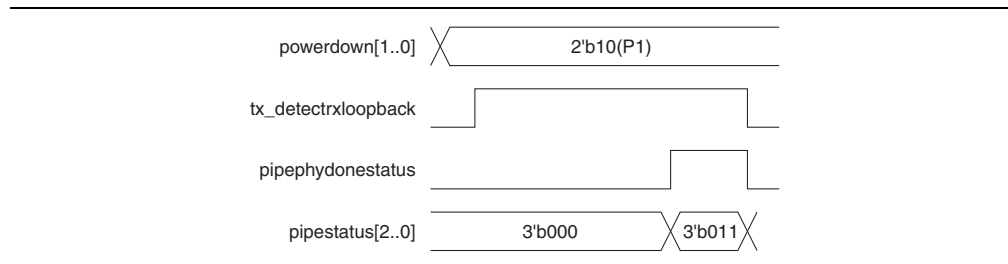
- Programmable run length violation detection—detects consecutive 1s or 0s in the data stream, and asserts run length violation signal (`rx_rlv`) when a preset run length threshold (maximum number of consecutive 1s or 0s) is detected. The `rx_rlv` signal in each channel is clocked by its parallel recovered clock and is asserted for a minimum of two recovered clock cycles to ensure that the FPGA fabric clock can latch the `rx_rlv` signal reliably because the FPGA fabric clock might have phase differences, ppm differences (in asynchronous systems), or both, with the recovered clock. Table 1–5 lists the run length violation circuit detection capabilities.

**Table 1–5. Run Length Violation Circuit Detection Capabilities**

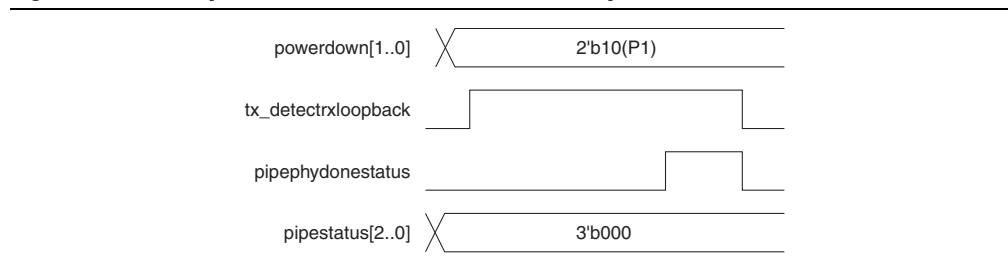
| Supported Data Width | Detector Range |         | Increment Step Settings |
|----------------------|----------------|---------|-------------------------|
|                      | Minimum        | Maximum |                         |
| 8-bit                | 4              | 128     | 4                       |
| 10-bit               | 5              | 160     | 5                       |

Figure 1–50 and Figure 1–51 show the detection mechanism example for a successful and unsuccessful receiver detection scenarios respectively. The tx\_forcelecidle port must be asserted at least 10 parallel clock cycles prior to assertion of tx\_detectrxloopback port to ensure the transmitter buffer is properly tri-stated. Detection completion is indicated by pipephydonestatus assertion, with detection successful indicated by 3'b011 on pipestatus[2..0] port, or detection unsuccessful by 3'b000 on pipestatus[2..0] port.

**Figure 1–50. Example of Successful Receiver Detect Operation**



**Figure 1–51. Example of Unsuccessful Receiver Detect Operation**

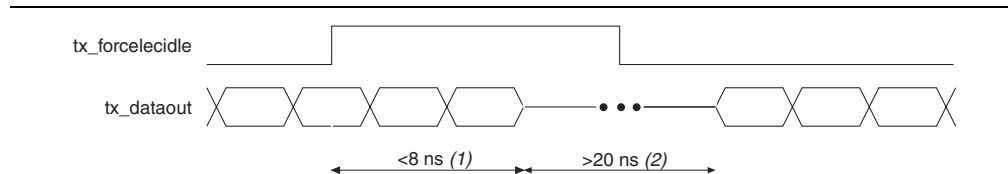


## Electrical Idle Control

The Cyclone IV GX transceivers support transmitter buffer in electrical idle state using the tx\_forcelecidle port. During electrical idle, the transmitter buffer differential and common mode output voltage levels are compliant to the PCIe Base Specification 2.0 for Gen1 signaling rate.

Figure 1–52 shows the relationship between assertion of the tx\_forcelecidle port and the transmitter buffer output on the tx\_dataout port.

**Figure 1–52. Transmitter Buffer Electrical Idle State**



### Notes to Figure 1–52:

- (1) The protocol requires the transmitter buffer to transition to a valid electrical idle after sending an electrical idle ordered set within 8 ns.
- (2) The protocol requires transmitter buffer to stay in electrical idle for a minimum of 20 ns for Gen1 signaling rate.

## Receive Bit-Slip Indication

The number of bits slipped in the word aligner for synchronization in manual alignment mode is provided with the `rx_bitslipboundaryselectout[4..0]` signal. For example, if one bit is slipped in word aligner to achieve synchronization, the output on `rx_bitslipboundaryselectout[4..0]` signal shows a value of 1 (5'00001). The information from this signal helps in latency calculation through the receiver as the number of bits slipped in the word aligner varies at each synchronization.

## Transmit Bit-Slip Control

The transmitter datapath supports bit-slip control to delay the serial data transmission by a number of specified bits in PCS with `tx_bitslipboundaryselect[4..0]` port. With 8- or 10-bit channel width, the transmitter supports zero to nine bits of data slip. This feature helps to maintain a fixed round trip latency by compensating latency variation from word aligner when providing the appropriate values on `tx_bitslipboundaryselect[4..0]` port based on values on `rx_bitslipboundaryselectout[4..0]` signal.

## PLL PFD feedback

In Deterministic Latency mode, when transmitter input reference clock frequency is the same as the low-speed clock, the PLL that clocks the transceiver supports PFD feedback. When enabled, the PLL compensates for delay uncertainty in the low-speed clock (`tx_clkout` in  $\times 1$  configuration or `coreclkout` in  $\times 4$  configuration) path relative to input reference and the transmitter datapath latency is fixed relative to the transmitter input reference clock.

## SDI Mode

SDI mode provides the non-bonded ( $\times 1$ ) transceiver channel datapath configuration for HD- and 3G-SDI protocol implementations.

Cyclone IV GX transceivers configured in SDI mode provides the serialization and deserialization functions that supports the SDI data rates as listed in Table 1–24.

**Table 1–24. Supported SDI Data Rates**

| SMPTE Standard <sup>(1)</sup> | Configuration         | Data Rate (Mbps) | FPGA Fabric-to-Transceiver Width | Byte SERDES Usage |
|-------------------------------|-----------------------|------------------|----------------------------------|-------------------|
| 292M                          | High definition (HD)  | 1483.5           | 20-bit                           | Used              |
|                               |                       |                  | 10-bit                           | Not used          |
|                               |                       | 1485             | 20-bit                           | Used              |
|                               |                       |                  | 10-bit                           | Not used          |
| 424M                          | Third-generation (3G) | 2967             | 20-bit                           | Used              |
|                               |                       | 2970             |                                  |                   |

**Note to Table 1–24:**

(1) Society of Motion Picture and Television Engineers (SMPTE).



SDI functions such as scrambling/de-scrambling, framing, and cyclic redundancy check (CRC) must be implemented in the user logic.

**Table 1-27. Receiver Ports in ALTGX Megafunction for Cyclone IV GX (Part 2 of 3)**

| Block  | Port Name                 | Input/<br>Output | Clock Domain                                                             | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--------|---------------------------|------------------|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RX PCS | rx_rmfifo full            | Output           | Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes) | Rate match FIFO full status indicator.<br><ul style="list-style-type: none"> <li>A high level indicates the rate match FIFO is full.</li> <li>Driven for a minimum of two serial clock cycles in configurations without a byte serializer and a minimum of three recovered clock cycles in configurations with a byte serializer.</li> </ul>                                                                                                                                                                                             |
|        | rx_rmfifo empty           | Output           | Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes) | Rate match FIFO empty status indicator.<br><ul style="list-style-type: none"> <li>A high level indicates the rate match FIFO is empty.</li> <li>Driven for a minimum of two serial clock cycles in configurations without a byte serializer and a minimum of three recovered clock cycles in configurations with a byte serializer.</li> </ul>                                                                                                                                                                                           |
|        | rx_ctrl detect            | Output           | Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes) | 8B/10B decoder control or data identifier.<br><ul style="list-style-type: none"> <li>A high level indicates received code group is a /Kx.y/ control code group.</li> <li>A low level indicates received code group is a /Dx.y/ data code group.</li> </ul>                                                                                                                                                                                                                                                                               |
|        | rx_err detect             | Output           | Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes) | 8B/10B code group violation or disparity error indicator.<br><ul style="list-style-type: none"> <li>A high level indicates that a code group violation or disparity error was detected on the associated received code group.</li> <li>Use with the rx_disperr signal to differentiate between a code group violation or a disparity error as follows: [rx_errdetect:rx_disperr] <ul style="list-style-type: none"> <li>2'b00—no error</li> <li>2'b10—code group violation</li> <li>2'b11—disparity error or both</li> </ul> </li> </ul> |
|        | rx_disperr                | Output           | Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes) | 8B/10B disparity error indicator.<br><ul style="list-style-type: none"> <li>A high level indicates that a disparity error was detected on the associated received code group.</li> </ul>                                                                                                                                                                                                                                                                                                                                                 |
|        | rx_running disp           | Output           | Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes) | 8B/10B current running disparity indicator.<br><ul style="list-style-type: none"> <li>A high level indicates a positive current running disparity at the end of the decoded byte</li> <li>A low level indicates a negative current running disparity at the end of the decoded byte</li> </ul>                                                                                                                                                                                                                                           |
|        | rx_enbyteord              | Input            | Asynchronous signal                                                      | Enable byte ordering control<br><ul style="list-style-type: none"> <li>A low-to-high transition triggers the byte ordering block to restart byte ordering operation.</li> </ul>                                                                                                                                                                                                                                                                                                                                                          |
|        | rx_byteorder align status | Output           | Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes) | Byte ordering status indicator.<br><ul style="list-style-type: none"> <li>A high level indicates that the byte ordering block has detected the programmed byte ordering pattern in the least significant byte of the received data from the byte deserializer.</li> </ul>                                                                                                                                                                                                                                                                |
|        | rx_dataout                | Output           | Synchronous to tx_clkout (non-bonded modes) or coreclkout (bonded modes) | Parallel data output from the receiver to the FPGA fabric.<br><ul style="list-style-type: none"> <li>Bus width depends on channel width multiplied by number of channels per instance.</li> </ul>                                                                                                                                                                                                                                                                                                                                        |

## Schmitt Trigger Input

Cyclone IV devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF\_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate. Table 1–14 lists the hysteresis specifications across the supported  $V_{CCIO}$  range for Schmitt trigger inputs in Cyclone IV devices.

**Table 1–14. Hysteresis Specifications for Schmitt Trigger Input in Cyclone IV Devices**

| Symbol        | Parameter                            | Conditions (V)   | Minimum | Unit |
|---------------|--------------------------------------|------------------|---------|------|
| $V_{SCHMITT}$ | Hysteresis for Schmitt trigger input | $V_{CCIO} = 3.3$ | 200     | mV   |
|               |                                      | $V_{CCIO} = 2.5$ | 200     | mV   |
|               |                                      | $V_{CCIO} = 1.8$ | 140     | mV   |
|               |                                      | $V_{CCIO} = 1.5$ | 110     | mV   |

## I/O Standard Specifications

The following tables list input voltage sensitivities ( $V_{IH}$  and  $V_{IL}$ ), output voltage ( $V_{OH}$  and  $V_{OL}$ ), and current drive characteristics ( $I_{OH}$  and  $I_{OL}$ ), for various I/O standards supported by Cyclone IV devices. Table 1–15 through Table 1–20 provide the I/O standard specifications for Cyclone IV devices.

**Table 1–15. Single-Ended I/O Standard Specifications for Cyclone IV Devices <sup>(1), (2)</sup>**

| I/O Standard                | $V_{CCIO}$ (V) |     |       | $V_{IL}$ (V) |                        | $V_{IH}$ (V)           |                  | $V_{OL}$ (V)           | $V_{OH}$ (V)           | $I_{OL}$ (mA)<br>(4) | $I_{OH}$ (mA)<br>(4) |
|-----------------------------|----------------|-----|-------|--------------|------------------------|------------------------|------------------|------------------------|------------------------|----------------------|----------------------|
|                             | Min            | Typ | Max   | Min          | Max                    | Min                    | Max              | Max                    | Min                    |                      |                      |
| 3.3-V LVTTTL <sup>(3)</sup> | 3.135          | 3.3 | 3.465 | —            | 0.8                    | 1.7                    | 3.6              | 0.45                   | 2.4                    | 4                    | –4                   |
| 3.3-V LVCMOS <sup>(3)</sup> | 3.135          | 3.3 | 3.465 | —            | 0.8                    | 1.7                    | 3.6              | 0.2                    | $V_{CCIO} - 0.2$       | 2                    | –2                   |
| 3.0-V LVTTTL <sup>(3)</sup> | 2.85           | 3.0 | 3.15  | –0.3         | 0.8                    | 1.7                    | $V_{CCIO} + 0.3$ | 0.45                   | 2.4                    | 4                    | –4                   |
| 3.0-V LVCMOS <sup>(3)</sup> | 2.85           | 3.0 | 3.15  | –0.3         | 0.8                    | 1.7                    | $V_{CCIO} + 0.3$ | 0.2                    | $V_{CCIO} - 0.2$       | 0.1                  | –0.1                 |
| 2.5 V <sup>(3)</sup>        | 2.375          | 2.5 | 2.625 | –0.3         | 0.7                    | 1.7                    | $V_{CCIO} + 0.3$ | 0.4                    | 2.0                    | 1                    | –1                   |
| 1.8 V                       | 1.71           | 1.8 | 1.89  | –0.3         | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | 2.25             | 0.45                   | $V_{CCIO} - 0.45$      | 2                    | –2                   |
| 1.5 V                       | 1.425          | 1.5 | 1.575 | –0.3         | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2                    | –2                   |
| 1.2 V                       | 1.14           | 1.2 | 1.26  | –0.3         | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2                    | –2                   |
| 3.0-V PCI                   | 2.85           | 3.0 | 3.15  | —            | $0.3 \times V_{CCIO}$  | $0.5 \times V_{CCIO}$  | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$  | $0.9 \times V_{CCIO}$  | 1.5                  | –0.5                 |
| 3.0-V PCI-X                 | 2.85           | 3.0 | 3.15  | —            | $0.35 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$  | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$  | $0.9 \times V_{CCIO}$  | 1.5                  | –0.5                 |

**Notes to Table 1–15:**

- (1) For voltage-referenced receiver input waveform and explanation of terms used in Table 1–15, refer to “Glossary” on page 1–37.
- (2) AC load  $CL = 10$  pF
- (3) For more information about interfacing Cyclone IV devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O standards, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O Systems*.
- (4) To meet the  $I_{OL}$  and  $I_{OH}$  specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTTL** specification (4 mA), set the current strength settings to 4 mA or higher. Setting at lower current strength may not meet the  $I_{OL}$  and  $I_{OH}$  specifications in the handbook.

For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

**Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices <sup>(1)</sup>**

| I/O Standard           | $V_{CCIO}$ (V) |     |       | $V_{Swing(DC)}$ (V) |            | $V_{X(AC)}$ (V)      |     |                      | $V_{Swing(AC)}$ (V) |            | $V_{OX(AC)}$ (V)     |     |                      |
|------------------------|----------------|-----|-------|---------------------|------------|----------------------|-----|----------------------|---------------------|------------|----------------------|-----|----------------------|
|                        | Min            | Typ | Max   | Min                 | Max        | Min                  | Typ | Max                  | Min                 | Max        | Min                  | Typ | Max                  |
| SSTL-2<br>Class I, II  | 2.375          | 2.5 | 2.625 | 0.36                | $V_{CCIO}$ | $V_{CCIO}/2 - 0.2$   | —   | $V_{CCIO}/2 + 0.2$   | 0.7                 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.125$ | —   | $V_{CCIO}/2 + 0.125$ |
| SSTL-18<br>Class I, II | 1.7            | 1.8 | 1.90  | 0.25                | $V_{CCIO}$ | $V_{CCIO}/2 - 0.175$ | —   | $V_{CCIO}/2 + 0.175$ | 0.5                 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.125$ | —   | $V_{CCIO}/2 + 0.125$ |

**Note to Table 1–18:**(1) Differential SSTL requires a  $V_{REF}$  input.**Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices <sup>(1)</sup>**

| I/O Standard           | $V_{CCIO}$ (V) |     |       | $V_{DIF(DC)}$ (V) |            | $V_{X(AC)}$ (V)        |     |                        | $V_{CM(DC)}$ (V)       |     |                        | $V_{DIF(AC)}$ (V) |                        |
|------------------------|----------------|-----|-------|-------------------|------------|------------------------|-----|------------------------|------------------------|-----|------------------------|-------------------|------------------------|
|                        | Min            | Typ | Max   | Min               | Max        | Min                    | Typ | Max                    | Min                    | Typ | Max                    | Min               | Max                    |
| HSTL-18<br>Class I, II | 1.71           | 1.8 | 1.89  | 0.2               | —          | 0.85                   | —   | 0.95                   | 0.85                   | —   | 0.95                   | 0.4               | —                      |
| HSTL-15<br>Class I, II | 1.425          | 1.5 | 1.575 | 0.2               | —          | 0.71                   | —   | 0.79                   | 0.71                   | —   | 0.79                   | 0.4               | —                      |
| HSTL-12<br>Class I, II | 1.14           | 1.2 | 1.26  | 0.16              | $V_{CCIO}$ | $0.48 \times V_{CCIO}$ | —   | $0.52 \times V_{CCIO}$ | $0.48 \times V_{CCIO}$ | —   | $0.52 \times V_{CCIO}$ | 0.3               | $0.48 \times V_{CCIO}$ |

**Note to Table 1–19:**(1) Differential HSTL requires a  $V_{REF}$  input.**Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices <sup>(1)</sup> (Part 1 of 2)**

| I/O Standard                           | $V_{CCIO}$ (V) |     |       | $V_{ID}$ (mV) |     | $V_{ICM}$ (V) <sup>(2)</sup> |                                               |      | $V_{OD}$ (mV) <sup>(3)</sup> |     |     | $V_{OS}$ (V) <sup>(3)</sup> |      |       |
|----------------------------------------|----------------|-----|-------|---------------|-----|------------------------------|-----------------------------------------------|------|------------------------------|-----|-----|-----------------------------|------|-------|
|                                        | Min            | Typ | Max   | Min           | Max | Min                          | Condition                                     | Max  | Min                          | Typ | Max | Min                         | Typ  | Max   |
| LVPECL<br>(Row I/Os) <sup>(6)</sup>    | 2.375          | 2.5 | 2.625 | 100           | —   | 0.05                         | $D_{MAX} \leq 500$ Mbps                       | 1.80 | —                            | —   | —   | —                           | —    | —     |
|                                        |                |     |       |               |     | 0.55                         | $500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps | 1.80 |                              |     |     |                             |      |       |
|                                        |                |     |       |               |     | 1.05                         | $D_{MAX} > 700$ Mbps                          | 1.55 |                              |     |     |                             |      |       |
| LVPECL<br>(Column I/Os) <sup>(6)</sup> | 2.375          | 2.5 | 2.625 | 100           | —   | 0.05                         | $D_{MAX} \leq 500$ Mbps                       | 1.80 | —                            | —   | —   | —                           | —    | —     |
|                                        |                |     |       |               |     | 0.55                         | $500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps | 1.80 |                              |     |     |                             |      |       |
|                                        |                |     |       |               |     | 1.05                         | $D_{MAX} > 700$ Mbps                          | 1.55 |                              |     |     |                             |      |       |
| LVDS (Row I/Os)                        | 2.375          | 2.5 | 2.625 | 100           | —   | 0.05                         | $D_{MAX} \leq 500$ Mbps                       | 1.80 | 247                          | —   | 600 | 1.125                       | 1.25 | 1.375 |
|                                        |                |     |       |               |     | 0.55                         | $500 \text{ Mbps} \leq D_{MAX} \leq 700$ Mbps | 1.80 |                              |     |     |                             |      |       |
|                                        |                |     |       |               |     | 1.05                         | $D_{MAX} > 700$ Mbps                          | 1.55 |                              |     |     |                             |      |       |

Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

**Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices <sup>(1), (2)</sup>**

| Symbol/<br>Description                                            | Conditions         | C6     |     |       | C7, I7 |     |       | C8     |     |       | Unit |
|-------------------------------------------------------------------|--------------------|--------|-----|-------|--------|-----|-------|--------|-----|-------|------|
|                                                                   |                    | Min    | Typ | Max   | Min    | Typ | Max   | Min    | Typ | Max   |      |
| PCIe Transmit Jitter Generation <sup>(3)</sup>                    |                    |        |     |       |        |     |       |        |     |       |      |
| Total jitter at 2.5 Gbps (Gen1)                                   | Compliance pattern | —      | —   | 0.25  | —      | —   | 0.25  | —      | —   | 0.25  | UI   |
| PCIe Receiver Jitter Tolerance <sup>(3)</sup>                     |                    |        |     |       |        |     |       |        |     |       |      |
| Total jitter at 2.5 Gbps (Gen1)                                   | Compliance pattern | > 0.6  |     |       | > 0.6  |     |       | > 0.6  |     |       | UI   |
| GIGE Transmit Jitter Generation <sup>(4)</sup>                    |                    |        |     |       |        |     |       |        |     |       |      |
| Deterministic jitter (peak-to-peak)                               | Pattern = CRPAT    | —      | —   | 0.14  | —      | —   | 0.14  | —      | —   | 0.14  | UI   |
| Total jitter (peak-to-peak)                                       | Pattern = CRPAT    | —      | —   | 0.279 | —      | —   | 0.279 | —      | —   | 0.279 | UI   |
| GIGE Receiver Jitter Tolerance <sup>(4)</sup>                     |                    |        |     |       |        |     |       |        |     |       |      |
| Deterministic jitter tolerance (peak-to-peak)                     | Pattern = CJPAT    | > 0.4  |     |       | > 0.4  |     |       | > 0.4  |     |       | UI   |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT    | > 0.66 |     |       | > 0.66 |     |       | > 0.66 |     |       | UI   |

**Notes to Table 1–23:**

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers specified are valid for the stated conditions only.
- (3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.
- (4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

## Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

### Clock Tree Specifications

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

**Table 1–24. Clock Tree Performance for Cyclone IV Devices (Part 1 of 2)**

| Device  | Performance |       |     |                    |                    |       |                    |     | Unit |
|---------|-------------|-------|-----|--------------------|--------------------|-------|--------------------|-----|------|
|         | C6          | C7    | C8  | C8L <sup>(1)</sup> | C9L <sup>(1)</sup> | I7    | I8L <sup>(1)</sup> | A7  |      |
| EP4CE6  | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE10 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE15 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE22 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE30 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |
| EP4CE40 | 500         | 437.5 | 402 | 362                | 265                | 437.5 | 362                | 402 | MHz  |