Intel - EP4CE30F23I7N Datasheet





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Details

Product Status	Active
Number of LABs/CLBs	1803
Number of Logic Elements/Cells	28848
Total RAM Bits	608256
Number of I/O	328
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce30f23i7n

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Chapter 11. Power Requirements for Cyclone IV Devices

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Cyclone IV Device Family Speed Grades

Table 1–5 lists the Cyclone IV GX devices speed grades.

Device	F169	F324	F484	F672	F896
EP4CGX15	C6, C7, C8, I7	—	—	—	—
EP4CGX22	C6, C7, C8, I7	C6, C7, C8, I7	—	—	—
EP4CGX30	C6, C7, C8, I7	C6, C7, C8, I7	C6, C7, C8, I7	—	—
EP4CGX50	—	—	C6, C7, C8, I7	C6, C7, C8, I7	—
EP4CGX75	—	—	C6, C7, C8, I7	C6, C7, C8, I7	—
EP4CGX110	—	—	C7, C8, I7	C7, C8, I7	C7, C8, I7
EP4CGX150	—	—	C7, C8, I7	C7, C8, I7	C7, C8, I7

Table 1–5. Speed Grades for the Cyclone IV GX Device Family

Table 1–6 lists the Cyclone IV E devices speed grades.

Table 1–6. Speed Grades for the Cyclone IV E Device Family
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Device	E144	M164	M256	U256	F256	F324	U484	F484	F780
EP4CE6	C8L, C9L, I8L C6, C7, C8, I7, A7	_	_	I7N	C8L, C9L, I8L C6, C7, C8, I7, A7	_	_	_	_
EP4CE10	C8L, C9L, I8L C6, C7, C8, I7, A7	_	_	I7N	C8L, C9L, I8L C6, C7, C8, I7, A7	_	_	_	_
EP4CE15	C8L, C9L, I8L C6, C7, C8, I7	I7N	C7N, 17N	7N, I7N I7N C8L, C9L, I8L C6, C7, C8, I7, C6, C7 A7 C8, C7, C8, C7, C8, C7, C8, C6, C7		C8L, C9L, I8L C6, C7, C8, I7, A7	_		
EP4CE22	C8L, C9L, I8L C6, C7, C8, I7, A7		_	I7N	C8L, C9L, I8L C6, C7, C8, I7, A7			_	_
EP4CE30	_	_	_	_	_	A7N	_	C8L, C9L, I8L C6, C7, C8, I7, A7	C8L, C9L, I8L C6, C7, C8, I7
EP4CE40	_	_	_	_	_	— A7N		C8L, C9L, I8L C6, C7, C8, I7, A7	C8L, C9L, I8L C6, C7, C8, I7
EP4CE55	_	_	—	_	_	_	17N	C8L, C9L, I8L C6, C7, C8, I7	C8L, C9L, I8L C6, C7, C8, I7
EP4CE75	_	_	_	_	_	— — I7N C8L, C6, C		C8L, C9L, I8L C6, C7, C8, I7	C8L, C9L, I8L C6, C7, C8, I7
EP4CE115	_	_	—	_	—	_	_	C8L, C9L, I8L C7, C8, I7	C8L, C9L, I8L C7, C8, I7

Notes to Table 1-6:

(1) C8L, C9L, and I8L speed grades are applicable for the 1.0-V core voltage.

(2) C6, C7, C8, I7, and A7 speed grades are applicable for the 1.2-V core voltage.

Logic Array Blocks

Logic array blocks (LABs) contain groups of LEs.

Topology

Each LAB consists of the following features:

- 16 LEs
- LAB control signals
- LE carry chains
- Register chains
- Local interconnect

The local interconnect transfers signals between LEs in the same LAB. Register chain connections transfer the output of one LE register to the adjacent LE register in an LAB. The Quartus II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local and register chain connections for performance and area efficiency.

Figure 2–4 shows the LAB structure for Cyclone IV devices.



Figure 2–4. Cyclone IV Device LAB Structure

GCLK Network Clock									GC	LK N	etwo	rks								
Sources	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
DPCLK2 (4)																				
CDPCLK1, Or	—	—	—	\checkmark	\checkmark	—	—	-	—	—	-	—	—	—	—				—	—
CDPCLK2 (2), (5)																				
DPCLK5 (4)																				
DPCLK7 (2)	_	_	_	_		~	_	_	_	_	_	_	_	_	_					_
DPCLK4 (4)																				
DPCLK6 (2)	_	_	_	_		_	~	_	_	_	_	_	_	_	_					_
DPCLK6 (4)																				
CDPCLK5, Or	—	—	—	—	—	—	—	\checkmark	—	—	—	—	—	—	—		_	—	_	—
CDPCLK6 (2), (5)																				
DPCLK3 (4)																				
CDPCLK4, Or	—	—	—	—	—	—	—	-	\checkmark	\checkmark	-	—	—	—	—			—	—	—
CDPCLK3 (2), (5)																				
DPCLK8	—	—	—	—	—	—	—	—	—	—	\checkmark	—	—	—	—	—	—	—	—	—
DPCLK11	—	—	—	—	_	—	—	—	—	_	—	\checkmark	—	—	—	_	_	_	_	_
DPCLK9	—	—	—	—	—	—	—	—	—	—	—	—	\checkmark	—	—			—	—	—
DPCLK10	—	—	—	—	—	—	—	—	—	—	—	—	—	\checkmark	\checkmark			—	—	—
DPCLK5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	\checkmark	—	—	—	—
DPCLK2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	\checkmark	—	—	—
DPCLK4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	\checkmark	—	—
DPCLK3	—	—	—	—		—	—	—	—	—	—	—	—	—	—				\checkmark	\checkmark

Table 5–3. GCLK Network Connections for Cyclone IV E Devices ⁽¹⁾ (Part 3 of 3)

Notes to Table 5-3:

(1) EP4CE6 and EP4CE10 devices only have GCLK networks 0 to 9.

(2) These pins apply to all Cyclone IV E devices except EP4CE6 and EP4CE10 devices.

(3) EP4CE6 and EP4CE10 devices only have PLL_1 and PLL_2.

(4) This pin applies only to EP4CE6 and EP4CE10 devices.

(5) Only one of the two CDPCLK pins can feed the clock control block. You can use the other pin as a regular I/O pin.

6. I/O Features in Cyclone IV Devices

This chapter describes the I/O and high speed I/O capabilities and features offered in Cyclone $^{\textcircled{B}}$ IV devices.

The I/O capabilities of Cyclone IV devices are driven by the diversification of I/O standards in many low-cost applications, and the significant increase in required I/O performance. Altera's objective is to create a device that accommodates your key board design needs with ease and flexibility.

The I/O flexibility of Cyclone IV devices is increased from the previous generation low-cost FPGAs by allowing all I/O standards to be selected on all I/O banks. Improvements to on-chip termination (OCT) support and the addition of true differential buffers have eliminated the need for external resistors in many applications, such as display system interfaces.

High-speed differential I/O standards have become popular in high-speed interfaces because of their significant advantages over single-ended I/O standards. The Cyclone IV devices support LVDS, BLVDS, RSDS, mini-LVDS, and PPDS. The transceiver reference clocks and the existing general-purpose I/O (GPIO) clock input features also support the LVDS I/O standards.

The Quartus[®] II software completes the solution with powerful pin planning features that allow you to plan and optimize I/O system designs even before the design files are available.

This chapter includes the following sections:

- "Cyclone IV I/O Elements" on page 6–2
- "I/O Element Features" on page 6–3
- "OCT Support" on page 6–6
- "I/O Standards" on page 6–11
- "Termination Scheme for I/O Standards" on page 6–13
- "I/O Banks" on page 6–16

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Figure 8–10 shows the AP configuration with multiple bus masters.

Figure 8–10. AP Configuration with Multiple Bus Masters



Notes to Figure 8–10:

- (1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL [3..0], refer to Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (4) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.
- (5) When cascading Cyclone IV E devices in a multi-device AP configuration, connect the repeater buffers between the master device and slave devices for DATA [15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8–5.
- (6) The other master device must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8-5.
- (7) The other master device can control the AP configuration bus by driving the nCE to high with an output high on the I/O pin.
- (8) The other master device can pulse nCONFIG if it is under system control and not tied to V_{CCIO}.

If you configure a master device with an SFL design, the master device enters user mode even though the slave devices in the multiple device chain are not being configured. The master device enters user mode with a SFL design even though the CONF_DONE signal is externally held low by the other slave devices in chain. Figure 8–29 shows the JTAG configuration of a single Cyclone IV device with a SFL design.





Notes to Figure 8-29:

- (1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL for AS configuration schemes, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (3) Pin 6 of the header is a V₁₀ reference voltage for the MasterBlaster output driver. The V₁₀ must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. When using the ByteBlasterMV download cable, this pin is a no connect. When using USB-Blaster, ByteBlaster II, and EthernetBlaster cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) You must connect the nCE pin to GND or driven low for successful JTAG configuration.
- (5) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (6) Power up the V_{CC} of the EthernetBlaster, ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5- V V_{CCA} supply. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.
- (7) Connect the series resistor at the near end of the serial configuration device.
- (8) These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as DATA[1] pin in AP and FPP modes.
- (9) Resistor value can vary from 1 k Ω to 10 k Ω .
- (10) Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK.

ISP of the Configuration Device

In the second stage, the SFL design in the master device allows you to write the configuration data for the device chain into the serial configuration device with the Cyclone IV device JTAG interface. The JTAG interface sends the programming data for the serial configuration device to the Cyclone IV device first. The Cyclone IV device then uses the ASMI pins to send the data to the serial configuration device.

Figure 10–3 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.



Figure 10–3. JTAG Chain of Mixed Voltages

Boundary-Scan Description Language Support

The boundary-scan description language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1/IEEE Std. 1149.6 BST-capable device that can be tested.

- For more information about how to download BSDL files for IEEE Std. 1149.1-compliant Cyclone IV E devices, refer to *IEEE Std.* 1149.1 BSDL Files.
- For more information about how to download BSDL files for IEEE Std.
 1149.6-compliant Cyclone IV GX devices, refer to IEEE Std. 1149.6 BSDL Files.
- You can also generate BSDL files (pre-configuration and post-configuration) for IEEE Std. 1149.1/IEEE Std. 1149.6-compliant Cyclone IV devices with the Quartus[®] II software version 9.1 SP1 and later. For more information about the procedure to generate BSDL files using the Quartus II software, refer to *BSDL Files Generation in Quartus II*.

Document Revision History

Table 10–3 lists the revision history for this chapter.

Table 10–3. Document Revision History

Date	Version	Changes
December 2013	1.3	 Updated the "EXTEST_PULSE" section.
November 2011 1.2		 Updated the "BST Operation Control" section.
		■ Updated Table 10–2.
	1.1	 Added Cyclone IV E devices in Table 10–1 and Table 10–2 for the Quartus II software version 9.1 SP1 release.
February 2010		■ Updated Figure 10–1 and Figure 10–2.
		 Minor text edits.
November 2009	1.0	Initial release.

Transmitter Output Buffer

Figure 1–11 shows the transmitter output buffer block diagram.





Note to Figure 1-11:

(1) Receiver detect function is specific for PCIe protocol implementation only. For more information, refer to "PCI Express (PIPE) Mode" on page 1–52.

The Cyclone IV GX transmitter output buffers support the **1.5-V PCML** I/O standard and are powered by VCCH_GXB power pins with 2.5-V supply. The 2.5-V supply on VCCH_GXB pins are regulated internally to 1.5-V for the transmitter output buffers. The transmitter output buffers support the following additional features:

- Programmable differential output voltage (V_{OD})—customizes the V_{OD} up to 1200 mV to handle different trace lengths, various backplanes, and various receiver requirements.
- Programmable pre-emphasis—boosts high-frequency components in the transmitted signal to maximize the data eye opening at the far-end. The high-frequency components might be attenuated in the transmission media due to data-dependent jitter and intersymbol interference (ISI) effects. The requirement for pre-emphasis increases as the data rates through legacy backplanes increase.
- Programmable differential on-chip termination (OCT)—provides calibrated OCT at differential 100 Ω or 150 Ω with on-chip transmitter common mode voltage (V_{CM}) at 0.65 V. V_{CM} is tri-stated when you disable the OCT to use external termination.
- Disable OCT to use external termination if the link requires a 85 Ω termination, such as when you are interfacing with certain PCIe Gen1 or Gen2 capable devices.
- The Cyclone IV GX transmitter output buffers are current-mode drivers. The resulting V_{OD} voltage is therefore a function of the transmitter termination value. For lists of supported V_{OD} settings, refer to the *Cyclone IV Device Data Sheet*.

Table 1–4 lists the synchronization state machine parameters for the word aligner in this mode.

Parameter	Allowed Values
Number of erroneous code groups received to lose synchronization	1–64
Number of continuous good code groups received to reduce the error count by one	1–256

 Table 1–4.
 Synchronization State Machine Parameters

After deassertion of the rx_digitalreset signal in automatic synchronization state machine mode, the word aligner starts looking for the synchronization code groups, word alignment pattern or its complement in the received data stream. When the programmed number of valid synchronization code groups or ordered sets are received, the rx_syncstatus signal is driven high to indicate that synchronization is acquired. The rx_syncstatus signal is constantly driven high until the programmed number of erroneous code groups are received without receiving intermediate good groups; after which the rx_syncstatus signal is driven low. The word aligner indicates loss of synchronization (rx_syncstatus signal remains low) until the programmed number of valid synchronization code groups are received again.

In addition to restoring word boundaries, the word aligner supports the following features:

Programmable run length violation detection—detects consecutive 1s or 0s in the data stream, and asserts run length violation signal (rx_rlv) when a preset run length threshold (maximum number of consecutive 1s or 0s) is detected. The rx_rlv signal in each channel is clocked by its parallel recovered clock and is asserted for a minimum of two recovered clock cycles to ensure that the FPGA fabric clock can latch the rx_rlv signal reliably because the FPGA fabric clock might have phase differences, ppm differences (in asynchronous systems), or both, with the recovered clock. Table 1–5 lists the run length violation circuit detection capabilities.

Supported Data Width	Detecto	Increment Step			
Supported Data Wittin	Minimum	Maximum	Settings		
8-bit	4	128	4		
10-bit	5	160	5		

Table 1–5. Run Length Violation Circuit Detection Capabilities

Figure 1–31 and Figure 1–32 show the high- and low-speed clock distribution for transceivers in F324 and smaller packages, and in F484 and larger packages in non-bonded channel configuration.

Figure 1–31. Clock Distribution in Non-Bonded Channel Configuration for Transceivers in F324 and Smaller Packages



Notes to Figure 1-31:

- (1) Transceiver channels 2 and 3 are not available for devices in F169 and smaller packages.
- (2) High-speed clock.
- (3) Low-speed clock.

Figure 1–67 shows the transceiver configuration in Deterministic Latency mode.

Functional Mode				Determinis	tic Latency			
Channel Bonding				×1	, ×4			
Low-Latency PCS				Disa	bled			
Word Aligner (Pattern Length)		Manual / (10	Alignment -Bit)			Bit (10	Slip -Bit)	
8B/10B Encoder/Decoder	Enab	led	Disa	bled	Ena	bled	Dise	abled
Rate Match FIFO	Disab	led	Disa	bled	Disa	abled	Dise	lbled
Byte SERDES	Enabled	Disabled	Enabled	Disabled	Enabled	Disabled	Enabled	Disabled
Data Rate (Gbps)	0.6- 3.125	0.6- 1.5625	0.6- 3.125	0.6- 1.5625	0.6- 3.125	0.6- 1.5625	0.6- 3.125	0.6- 1.5625
Byte Ordering	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
FPGA Fabric-to-Transceiver Interface Width	▼ 16-Bit	8-Bit	20-Bit	10-Bit	16-Bit	8-Bit	20-Bit	10-Bit
FPGA Fabric-to-Transceiver Interface Frequency (MHz)	60- 156.25	30- 156.25	60- 156.25	▼ 30- 156.25	60- 156.25	30- 156.25	60- 156.25	30- 156.25
TX PCS Latency (FPGA Fabric-Transceiver Interface Clock Cycles)	2.5 - 3.5	4 - 5	2.5 - 3.5	4 - 5	2.5 - 3	4	2.5 - 3	4
RX PCS Latency (FPGA Fabric-Transceiver Interface	5-6	8-9	5-6	8-9	5-6	8-9	5-6	8-9

Figure 1–67. Transceiver Configuration in Deterministic Latency Mode

Both CPRI and OBSAI protocols define the serial interface connecting the base station component (specifically channel cards) and remote radio heads (specifically radio frequency cards) in a radio base station system with fiber optics. The protocols require the accuracy of round trip delay measurement for single-hop and multi-hop connections to be within \pm 16.276 ns. The Cyclone IV GX transceivers support the following CPRI and OBSAI line rates using Deterministic Latency mode:

- CPRI —614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps, and 3.072 Gbps
- OBSAI—768 Mbps, 1.536 Gbps, and 3.072 Gbps

• For more information about deterministic latency implementation, refer to *AN 610: Implementing Deterministic Latency for CPRI and OBSAI Protocols in Stratix IV, HardCopy IV, Arria II GX, and Cyclone IV Devices.*

Registered Mode Phase Compensation FIFO

In Deterministic Latency mode, the RX phase compensation FIFO is set to registered mode while the TX phase compensation FIFO supports optional registered mode. When set into registered mode, the phase compensation FIFO acts as a register and eliminates the latency uncertainty through the FIFOs.

Serial loopback mode can only be dynamically enabled or disabled during user mode by performing a dynamic channel reconfiguration.

Figure 1–71. Serial Loopback Path⁽¹⁾



Note to Figure 1–71:

(1) Grayed-Out Blocks are Not Active in this mode.

Reverse Serial Loopback

The reverse serial loopback mode is available for all functional modes except for XAUI mode. The two reverse serial loopback options from the receiver to the transmitter are:

- Pre-CDR mode where data received through the RX input buffer is looped back to the TX output buffer using the **Reverse serial loopback (pre-CDR)** option
- Post-CDR mode where retimed data through the receiver CDR from the RX input buffer is looped back to the TX output buffer using the Reverse serial loopback option

The received data is also available to the FPGA logic. In the transmitter channel, only the transmitter buffer is active.

- The transmitter pre-emphasis feature is not available in reverse serial loopback (pre-CDR) mode.
- Reverse serial loopback modes can only be dynamically enabled or disabled during user mode by performing a dynamic channel reconfiguration.

Figure 1–72 shows the two paths in reverse serial loopback mode.

Figure 1–72. Reverse Serial Loopback ⁽¹⁾



Notes to Figure 1-72:

- (1) Grayed-Out Blocks are Not Active in this mode.
- (2) Post-CDR reverse serial loopback path.
- (3) Pre-CDR reverse serial loopback path.

Self Test Modes

Each transceiver channel in the Cyclone IV GX device contains modules for pattern generator and verifier. Using these built-in features, you can verify the functionality of the functional blocks in the transceiver channel without requiring user logic. The self test functionality is provided as an optional mechanism for debugging transceiver channels.

There are three types of supported pattern generators and verifiers:

- Built-in self test (BIST) incremental data generator and verifier—test the complete transmitter PCS and receiver PCS datapaths for bit errors with parallel loopback before the PMA blocks.
- Pseudo-random binary sequence (PRBS) generator and verifier—the PRBS generator and verifier interface with the serializer and deserializer in the PMA blocks. The advantage of using a PRBS data stream is that the randomness yields an environment that stresses the transmission medium. In the data stream, you can observe both random jitter and deterministic jitter using a time interval analyzer, bit error rate tester, or oscilloscope.
- High frequency and low frequency pattern generator—the high frequency patterns generate alternate ones and zeros and the low frequency patterns generate five ones and five zeroes. These patterns do not have a corresponding verifier.

The self-test features are only supported in Basic mode.

User Reset and Power-Down Signals

Each transceiver channel in the Cyclone IV GX device has individual reset signals to reset its physical coding sublayer (PCS) and physical medium attachment (PMA). The transceiver block also has a power-down signal that affects the multipurpose phase-locked loops (PLLs), general purpose PLLs, and all the channels in the transceiver block.



Table 2–1 lists the reset signals available for each transceiver channel.

Signal	ALTGX MegaWizard Plug-In Manager Configurations	Description
ty digital reset (1)	 Transmitter Only Receiver and Transmitter 	Provides asynchronous reset to all digital logic in the transmitter PCS, including the XAUI transmit state machine.
tx_uigitaileset		The minimum pulse width for this signal is two parallel clock cycles.
rx_digitalreset ⁽¹⁾	 Receiver Only Receiver and Transmitter 	 Resets all digital logic in the receiver PCS, including: XAUI receiver state machines GIGE receiver state machines XAUI channel alignment state machine BIST-PRBS verifier BIST-incremental verifier The minimum pulse width for this signal is two parallel clock evologies
rx_analogreset	 Receiver Only Receiver and Transmitter 	Resets the receiver CDR present in the receiver channel. The minimum pulse width is two parallel clock cycles.

Table 2–1. Transceiver Channel Reset Signals

Note to Table 2–1:

(1) Assert this signal until the clocks coming out of the multipurpose PLL and receiver CDR are stabilized. Stable parallel clocks are essential for proper operation of transmitter and receiver phase-compensation FIFOs in the PCS.

Port Name	Input/ Output	Description						
		This is an optional equalizer DC gain write control.						
		The width of this signal is fixed to 2 bits if you enable either the Use 'logical_channel_address' port for Analog controls reconfiguration option or the Use same control signal for all the channels option in the Analog controls screen. Otherwise, the width of this signal is 2 bits per channel.						
		The following values are the legal settings allowed for this signal:						
		rx_eqdcgain[10] Corresponding ALTGX Corresponding						
rx_eqdcgain [10] ⁽¹⁾	Input	(dB) DC Gain value						
		2′b00 0 0						
		2'b01 1 3 ⁽²⁾						
		2'b10 2 6						
		All other values => N/A						
		For more information, refer to the "Programmable Equalization and DC Gain" section of the <i>Cyclone IV GX Device Datasheet</i> chapter.						
<pre>tx_vodctrl_out [20]</pre>	Output	This is an optional transmit V_{OD} read control signal. This signal reads out the value written into the V_{OD} control register. The width of this output signal depends on the number of channels controlled by the dynamic reconfiguration controller and also the configuration of the Use 'logical_channel_address' port for Analog controls reconfiguration option and the Use same control signal for all the channels option.						
tx_preemp_out [40]	Output	This is an optional pre-emphasis read control signal. This signal reads out the value written by its input control signal. The width of this output signal depends on the number of channels controlled by the dynamic reconfiguration controller and also the configuration of the Use 'logical_channel_address' port for Analog controls reconfiguration option and the Use same control signal for all the channels option.						
rx_eqctrl_out [30]	Output	This is an optional read control signal to read the setting of equalization setting of the ALTGX instance. The width of this output signal depends on the number of channels controlled by the dynamic reconfiguration controller and also the configuration of the Use 'logical_channel_address' port for Analog controls reconfiguration option and the Use same control signal for all the channels option.						
rx_eqdcgain_out [10]	Output	This is an optional equalizer DC gain read control signal. This signal reads out the settings of the ALTGX instance DC gain. The width of this output signal depends on the number of channels controlled by the dynamic reconfiguration controller and also the configuration of the Use 'logical_channel_address' port for Analog controls reconfiguration option and the Use same control signal for all the channels option.						
Transceiver Channel Re	Transceiver Channel Reconfiguration Control/Status Signals							
		Set the following values at this signal to activate the appropriate dynamic reconfiguration mode:						
rogonfig mode		3'b000 = PMA controls reconfiguration mode. This is the default value.						
sel[20] ⁽³⁾	Input	3'b001 = Channel reconfiguration mode						
		All other values => N/A						
		reconfig_mode_sel[] is available as an input only when you enable more than one dynamic reconfiguration mode.						

Table 3–2. Dynamic Reconfiguration Controller Port List (ALTGX_RECONFIG Instance) (Part 6 of 7)

This chapter provides additional information about the document and Altera.

About this Handbook

This handbook provides comprehensive information about the Altera[®] Cyclone[®] IV family of devices.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact ⁽¹⁾	Contact Method	Address				
Technical support	Website	www.altera.com/support				
Technical training	Website	www.altera.com/training				
recinical training	Email	custrain@altera.com				
Product literature	Website	www.altera.com/literature				
Nontechnical support (general)	Email	nacomp@altera.com				
(software licensing)	Email	authorization@altera.com				

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning							
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box. For GUI elements, capitalization matches the GUI.							
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, \qdesigns directory, D : drive, and chiptrip.gdf file.							
Italic Type with Initial Capital Letters	Indicate document titles. For example, Stratix IV Design Guidelines.							
	Indicates variables. For example, $n + 1$.							
italic type	Variable names are enclosed in angle brackets (< >). For example, <i><file name=""></file></i> and <i><project name="">.pof</project></i> file.							
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.							
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."							

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

 Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices (1), (2) (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{ccint} (3)	Supply voltage for internal logic, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply voltage for internal logic, 1.0-V operation	—	0.97	1.0	1.03	V
	Supply voltage for output buffers, 3.3-V operation	—	3.135	3.3	3.465	V
	Supply voltage for output buffers, 3.0-V operation	_	2.85	3	3.15	V
\ <i>(</i> (3). (4)	Supply voltage for output buffers, 2.5-V operation	_	2.375	2.5	2.625	V
VCCIO (57, (57	Supply voltage for output buffers, 1.8-V operation	_	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
V _{CCA} (3)	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
V _{CCD_PLL} (3)	Supply (digital) voltage for PLL, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply (digital) voltage for PLL, 1.0-V operation	—	0.97	1.0	1.03	V
VI	Input voltage	—	-0.5		3.6	V
V ₀	Output voltage	—	0		V _{CCIO}	V
TJ		For commercial use	0		85	°C
	Operating junction temperature	For industrial use	-40		100	°C
		For extended temperature	-40		125	°C
		For automotive use	-40		125	°C
t _{RAMP}	Power supply ramp time	Standard power-on reset (POR) ⁽⁵⁾	50 µs	_	50 ms	_
		Fast POR (6)	50 µs		1.25 1.03 3.465 3.15 2.625 1.89 1.575 1.26 2.625 1.26 2.625 1.26 2.625 1.26 2.625 1.26 2.625 1.25 1.03 3.6 V _{CCI0} 85 100 125 50 ms 3 ms	

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Ilmit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
f _{HSCLK} (input	×10	5	420	5	370	5	320	5	320	5	250	MHz
	×8	5	420	5	370	5	320	5	320	5	250	MHz
	×7	5	420	5	370	5	320	5	320	5	250	MHz
frequency)	×4	5	420	5	370	5	320	5	320	5	250	MHz
	×2	5	420	5	370	5	320	5	320	5	250	MHz
	×1	5	420	5	402.5	5	402.5	5	362	5	265	MHz
	×10	100	840	100	740	100	640	100	640	100	500	Mbps
	×8	80	840	80	740	80	640	80	640	80	500	Mbps
	×7	70	840	70	740	70	640	70	640	70	500	Mbps
חטוטח	×4	40	840	40	740	40	640	40	640	40	500	Mbps
	×2	20	840	20	740	20	640	20	640	20	500	Mbps
	×1	10	420	10	402.5	10	402.5	10	362	10	265	Mbps
t _{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	_	200		200	_	200	_	200	_	200	ps
Output jitter (peak to peak)	_	_	500	_	500	_	550	_	600	_	700	ps
t _{LOCK} (2)	—		1	—	1	_	1	_	1	_	1	ms

Table 1–34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)}

Notes to Table 1-34:

(1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices ^{(1), (3)} (Part 1 of 2)

Symbol	Modes	C6		C7, 17		C8, A7		C8L, I8L		C9L		11
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	UIIIT
	×10	5	320	5	320	5	275	5	275	5	250	MHz
	×8	5	320	5	320	5	275	5	275	5	250	MHz
f _{HSCLK} (input	×7	5	320	5	320	5	275	5	275	5	250	MHz
frequency)	×4	5	320	5	320	5	275	5	275	5	250	MHz
	×2	5	320	5	320	5	275	5	275	5	250	MHz
	×1	5	402.5	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	640	100	640	100	550	100	550	100	500	Mbps
	×8	80	640	80	640	80	550	80	550	80	500	Mbps
	×7	70	640	70	640	70	550	70	550	70	500	Mbps
	×4	40	640	40	640	40	550	40	550	40	500	Mbps
	×2	20	640	20	640	20	550	20	550	20	500	Mbps
	×1	10	402.5	10	402.5	10	402.5	10	362	10	265	Mbps