Intel - EP4CE30F29C7 Datasheet





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Details

Product Status	Active
Number of LABs/CLBs	1803
Number of Logic Elements/Cells	28848
Total RAM Bits	608256
Number of I/O	532
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce30f29c7

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20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. Choose the secondary clock frequency so the VCO operates in the recommended frequency range. Also, set the M, N, and C counters accordingly to keep the VCO operating frequency in the recommended range.

Figure 5–18 shows a waveform example of the switchover feature when using automatic loss of clock detection. Here, the inclk0 signal remains low. After the inclk0 signal remains low for approximately two clock cycles, the clock-sense circuitry drives the clkbad0 signal high. Also, because the reference clock signal is not toggling, the switchover state machine controls the multiplexer through the clksw signal to switch to inclk1.





Note to Figure 5–18:

(1) Switchover is enabled on the falling edge of inclk1 or inclk1, depending on which clock is available. In this figure, switchover is enabled on the falling edge of inclk1.

Manual Override

If you are using the automatic switchover, you must switch input clocks with the manual override feature with the clkswitch input.

Figure 5–19 shows an example of a waveform illustrating the switchover feature when controlled by clkswitch. In this case, both clock sources are functional and inclk0 is selected as the reference clock. A low-to-high transition of the clkswitch signal starts the switchover sequence. The clkswitch signal must be high for at least three clock cycles (at least three of the longer clock period if inclk0 and inclk1 have different frequencies). On the falling edge of inclk0, the reference clock of the counter, muxout, is gated off to prevent any clock glitching. On the falling edge of inclk1, the reference clock multiplexer switches from inclk0 to inclk1 as the PLL reference, and the activeclock signal changes to indicate which clock is currently feeding the PLL.

- Low time count = 1 cycle
- rselodd = 1 effectively equals:
 - High time count = 1.5 cycles
 - Low time count = 1.5 cycles
 - Duty cycle = (1.5/3)% high time count and (1.5/3)% low time count

Scan Chain Description

Cyclone IV PLLs have a 144-bit scan chain.

Table 5–7 lists the number of bits for each component of the PLL.

Table 5–7.	Cyclone	IV PLL	Reprogramming Bits
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Dissk Nome	Number of Bits				
DIUCK Name	Counter	Other	Total		
C4 (1)	16	2 (2)	18		
C3	16	2 (2)	18		
C2	16	2 (2)	18		
C1	16	2 (2)	18		
CO	16	2 (2)	18		
М	16	2 (2)	18		
Ν	16	2 (2)	18		
Charge Pump	9	0	9		
Loop Filter ⁽³⁾	9	0	9		
Total number of bits:	otal number of bits: 144				

Notes to Table 5-7:

(1) LSB bit for C4 low-count value is the first bit shifted into the scan chain.

- (2) These two control bits include <code>rbypass</code>, for bypassing the counter, and <code>rselodd</code>, to select the output clock duty cycle.
- (3) MSB bit for loop filter is the last bit shifted into the scan chain.

Figure 5–24 shows the scan chain order of the PLL components.

Figure 5–24. PLL Component Scan Chain Order



Table 6–2 on page 6–7 shows the possible settings for I/O standards with current strength control. These programmable current strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for IOH and IOL of the corresponding I/O standard.

 \square When you use programmable current strength, on-chip series termination (R_S OCT) is not available.

Slew Rate Control

The output buffer for each Cyclone IV I/O pin provides optional programmable output slew-rate control. Table 6–2 on page 6–7 shows the possible slew rate option and the Quartus II default slew rate setting. However, these fast transitions may introduce noise transients in the system. A slower slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Because each I/O pin has an individual slew-rate control, you can specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges. Slew rate control is available for single-ended I/O standards with current strength of 8 mA or higher.

- You cannot use the programmable slew rate feature when using OCT with calibration.
- You cannot use the programmable slew rate feature when using the 3.0-V PCI, 3.0-V PCI-X, 3.3-V LVTTL, or 3.3-V LVCMOS I/O standards. Only the fast slew rate (default) setting is available.

Open-Drain Output

Cyclone IV devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that are asserted by multiple devices in your system.

Bus Hold

Each Cyclone IV device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry holds the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage in which noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than $V_{\rm CCIO}$ to prevent overdriving signals.

IF you enable the bus-hold feature, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus-hold circuitry is not available on dedicated clock pins.

Bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Figure 6–14 shows a typical BLVDS topology with multiple transmitter and receiver pairs.



Figure 6-14. BLVDS Topology with Cyclone IV Devices Transmitters and Receivers

The BLVDS I/O standard is supported on the top, bottom, and right I/O banks of Cyclone IV devices. The BLVDS transmitter uses two single-ended output buffers with the second output buffer programmed as inverted, while the BLVDS receiver uses a true LVDS input buffer. The transmitter and receiver share the same pins. An output-enabled (OE) signal is required to tristate the output buffers when the LVDS input buffer receives a signal.

• For more information, refer to the *Cyclone IV Device Datasheet* chapter.

Designing with BLVDS

The BLVDS bidirectional communication requires termination at both ends of the bus in BLVDS. The termination resistor (R_T) must match the bus differential impedance, which in turn depends on the loading on the bus. Increasing the load decreases the bus differential impedance. With termination at both ends of the bus, termination is not required between the two signals at the input buffer. A single series resistor (R_S) is required at the output buffer to match the output buffer impedance to the transmission line impedance. However, this series resistor affects the voltage swing at the input buffer. The maximum data rate achievable depends on many factors.

- Altera recommends that you perform simulation using the IBIS model while considering factors such as bus loading, termination values, and output and input buffer location on the bus to ensure that the required performance is achieved.
- ***** For more information about BLVDS interface support in Altera devices, refer to *AN 522: Implementing Bus LVDS Interface in Supported Altera Device Families.*

- "FPP Configuration" on page 8–40
- "JTAG Configuration" on page 8–45
- "Device Configuration Pins" on page 8–62

Configuration Features

Table 8–1 lists the configuration methods you can use in each configuration scheme.

Table 8–1. Configuration Features in Cyclone IV Devices

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade ⁽¹⁾
AS	Serial Configuration Device	~	\checkmark
AP	Supported Flash Memory (2)	_	\checkmark
DC	External Host with Flash Memory	\checkmark	✓ (3)
	Download Cable	~	_
FPP	External Host with Flash Memory	_	✓ (3)
ITAC based configuration	External Host with Flash Memory	—	_
o rAd based connyuration	Download Cable	—	_

Notes to Table 8-1:

(1) Remote update mode is supported when you use the Remote System Upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus® II software.

(2) For more information about the supported device families for the Micron commodity parallel flash, refer to Table 8–10 on page 8–22.

(3) Remote update mode is supported externally using the Parallel Flash Loader (PFL) with the Quartus II software.

Configuration Data Decompression

Cyclone IV devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and send the compressed bitstream to Cyclone IV devices. During configuration, Cyclone IV devices decompress the bitstream in real time and program the SRAM cells.

Compression may reduce the configuration bitstream size by 35 to 55%.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time required to send the bitstream to the Cyclone IV device. The time required by a Cyclone IV device to decompress a configuration file is less than the time required to send the configuration data to the device. There are two methods for enabling compression for the Cyclone IV device bitstreams in the Quartus II software:

- Before design compilation (through the Compiler Settings menu)
- After design compilation (through the **Convert Programming Files** dialog box)

To enable compression in the compiler settings of the project in the Quartus II software, perform the following steps:

- 1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.
- 2. Click Device and Pin Options. The Device and Pin Options dialog box appears.

This four-pin interface connects to Cyclone IV device pins, as shown in Figure 8-2.



Figure 8–2. Single-Device AS Configuration

Notes to Figure 8-2:

(1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

- (2) Cyclone IV devices use the ASDO-to-ASDI path to control the configuration device.
- (3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (5) Connect the series resistor at the near end of the serial configuration device.
- (6) These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as the DATA [1] pin in AP and FPP modes.
- (7) Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK.
- To tri-state the configuration bus for AS configuration schemes, you must tie nCE high and nCONFIG low.
- The 25-Ω resistor at the near end of the serial configuration device for DATA[0] works to minimize the driver impedance mismatch with the board trace and reduce the overshoot seen at the Cyclone IV device DATA[0] input pin.

In the single-device AS configuration, the maximum board loading and board trace length between the supported serial configuration device and the Cyclone IV device must follow the recommendations in Table 8–7 on page 8–18.

The DCLK generated by the Cyclone IV device controls the entire configuration cycle and provides timing for the serial interface. Cyclone IV devices use an internal oscillator or an external clock source to generate the DCLK. For Cyclone IV E devices, you can use a 40-MHz internal oscillator to generate the DCLK and for Cyclone IV GX devices you can use a slow clock (20 MHz maximum) or a fast clock (40 MHz maximum) from the internal oscillator or an external clock from CLKUSR to generate the DCLK. There are some variations in the internal oscillator frequency because of the process, voltage, and temperature (PVT) conditions in Cyclone IV

Single SRAM Object File

The second method configures both the master device and slave devices with the same **.sof**. The serial configuration device stores one copy of the **.sof**. You must set up one or more slave devices in the chain. All the slave devices must be set up in the same way (Figure 8–5).





Notes to Figure 8-5:

- (1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (3) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the master device of the Cyclone IV device in AS mode and the slave devices in PS mode. To connect the MSEL pins for the master device in AS mode and slave devices in PS mode, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (4) Connect the series resistor at the near end of the serial configuration device.
- (5) Connect the repeater buffers between the master and slave devices for DATA[0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8–5.
- (6) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.
- (7) These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as DATA [1] pin in AP and FPP modes.
- (8) Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK.
- (9) For multi-devices AS configuration using Cyclone IV E with 1,0 V core voltage, the maximum board trace-length from the serial configuration device to the junction-split on both DCLK and Data0 line is 3.5 inches.

In this setup, all the Cyclone IV devices in the chain are connected for concurrent configuration. This reduces the AS configuration time because all the Cyclone IV devices are configured in one configuration cycle. Connect the nCE input pins of all the Cyclone IV devices to GND. You can either leave the nCEO output pins on all the Cyclone IV devices unconnected or use the nCEO output pins as normal user I/O pins. The DATA and DCLK pins are connected in parallel to all the Cyclone IV devices.

Figure 8–10 shows the AP configuration with multiple bus masters.

Figure 8–10. AP Configuration with Multiple Bus Masters



Notes to Figure 8–10:

- (1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL [3..0], refer to Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (4) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.
- (5) When cascading Cyclone IV E devices in a multi-device AP configuration, connect the repeater buffers between the master device and slave devices for DATA [15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8–5.
- (6) The other master device must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8-5.
- (7) The other master device can control the AP configuration bus by driving the nCE to high with an output high on the I/O pin.
- (8) The other master device can pulse nCONFIG if it is under system control and not tied to V_{CCIO}.



Figure 8–24. JTAG Configuration of a Single Device Using a Download Cable (1.5-V or 1.8-V V_{CCIO} Powering the JTAG Pins)

Notes to Figure 8-24:

- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Connect the nCONFIG and MSEL pins to support a non-JTAG configuration scheme. If you only use JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.
- (3) In the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming; otherwise it is a no connect.
- (4) The nCE must be connected to GND or driven low for successful JTAG configuration.
- (5) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (6) Power up the V_{CC} of the EthernetBlaster, ByteBlaster II or USB-Blaster cable with supply from V_{CCI0}. The Ethernet-Blaster, ByteBlaster II, and USB-Blaster cables do not support a target supply voltage of 1.2 V. For the target supply voltage value, refer to the *ByteBlaster II Download Cable User Guide*, the USB-Blaster Download Cable User Guide, and the EthernetBlaster Communications Cable User Guide.
- (7) Resistor value can vary from 1 k Ω to 10 k Ω .

To configure a single device in a JTAG chain, the programming software places all other devices in bypass mode. In bypass mode, devices pass programming data from the TDI pin to the TDO pin through a single bypass register without being affected internally. This scheme enables the programming software to program or verify the target device. Configuration data driven into the device appears on the TDO pin one clock cycle later.

The Quartus II software verifies successful JTAG configuration after completion. At the end of configuration, the software checks the state of CONF_DONE through the JTAG port. When Quartus II generates a **.jam** for a multi-device chain, it contains instructions so that all the devices in the chain are initialized at the same time. If CONF_DONE is not high, the Quartus II software indicates that configuration has failed. If CONF_DONE is high, the software indicates that configuration was successful. After the configuration bitstream is serially sent using the JTAG TDI port, the TCK port clocks an additional clock cycles to perform device initialization.

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CONF_DONE	N/A	All	Bidirectional open-drain	 Status output—the target Cyclone IV device drives the CONF_DONE pin low before and during configuration. After all the configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE. Status input—after all the data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an
				external 10-kΩ pull-up resistor in order for the device to initialize. Driving CONF_DONE low after configuration and initialization does not affect the configured device. Do not connect hus
				holds or ADC to CONF_DONE pin.
nCE	N/A	All	Input	Active-low chip enable. The nCE pin activates the Cyclone IV device with a low signal to allow configuration. You must hold nCE pin low during configuration, initialization, and user-mode. In a single-device configuration, you must tie the nCE pin low. In a multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. You must hold the nCE pin low for successful JTAG programming of the device.
	N/A if option is on.		Output	Output that drives low when configuration is complete. In a single-device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In a multi-device configuration, this pin feeds the nCE pin of the next device. The $nCEO$ of the last device in the chain is left floating or used as a user I/O pin after configuration.
nCEO	I/O if option is off.	All	open-drain	If you use the nCEO pin to feed the nCE pin of the next device, use an external 10-k Ω pull-up resistor to pull the nCEO pin high to the V _{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor.
				If you use the nCEO pin as a user I/O pin after configuration, set the state of the pin on the Dual-Purpose Pin settings.
nCSO,				Output control signal from the Cyclone IV device to the serial configuration device in AS mode that enables the configuration device. This pin functions as nCSO in AS mode and FLASH_nCE in AP mode.
FLASH_nCE (1)	Ι/Ο	AS, AP <i>(2)</i>	Output	Output control signal from the Cyclone IV device to the parallel flash in AP mode that enables the flash. Connects to the $CE\#$ pin on the Micron P30 or P33 flash. ⁽²⁾
				This pin has an internal pull-up resistor that is always active.

Table 8-20	. Dedicated	Configuration	Pins on th	ne Cyclone	IV Device	(Part 2 of 4)
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Configuration error detection determines if the configuration data received through an external memory device is corrupted during configuration. To validate the configuration data, the Quartus[®] II software uses a function to calculate the CRC value for each configuration data frame and stores the frame-based CRC value in the configuration data as part of the configuration bit stream.

During configuration, Cyclone IV devices use the same methodology to calculate the CRC value based on the frame of data that is received and compares it against the frame CRC value in the data stream. Configuration continues until either the device detects an error or all the values are calculated.

In addition to the frame-based CRC value, the Quartus II software generates a 32-bit CRC value for the whole configuration bit stream. This 32-bit CRC value is stored in the 32-bit storage register at the end of the configuration and is used for user mode error detection that is discussed in "User Mode Error Detection".

User Mode Error Detection

User mode error detection is available in Cyclone IV GX and Cyclone IV E devices with 1.2-V core voltage. Cyclone IV E devices with 1.0-V core voltage do not support user mode error detection.

Soft errors are changes in a configuration random-access memory (CRAM) bit state due to an ionizing particle. Cyclone IV devices have built-in error detection circuitry to detect data corruption by soft errors in the CRAM cells.

This error detection capability continuously computes the CRC of the configured CRAM bits based on the contents of the device and compares it with the pre-calculated CRC value obtained at the end of the configuration. If the CRCs match, there is no error in the current configuration CRAM bits. The process of error detection continues until the device is reset (by setting nCONFIG to low).

The Cyclone IV device error detection feature does not check memory blocks and I/O buffers. These device memory blocks support parity bits that are used to check the contents of memory blocks for any error. The I/O buffers are not verified during error detection because the configuration data uses flip-flops as storage elements that are more resistant to soft errors. Similar flip-flops are used to store the pre-calculated CRC and other error detection circuitry option bits.

The error detection circuitry in Cyclone IV devices uses a 32-bit CRC IEEE 802 standard and a 32-bit polynomial as the CRC generator. Therefore, a single 32-bit CRC calculation is performed by the device. If a soft error does not occur, the resulting 32-bit signature value is 0x00000000, that results in a 0 on the CRC_ERROR output signal. If a soft error occurs in the device, the resulting signature value is non-zero and the CRC_ERROR output signal is 1.

You can inject a soft error by changing the 32-bit CRC storage register in the CRC circuitry. After verifying the induced failure, you can restore the 32-bit CRC value to the correct CRC value with the same instruction and inserting the correct value.

Before updating it with a known bad value, Altera recommends reading out the correct value.

P

Table 9–4 defines the registers shown in Figure 9–1.

 Table 9–4.
 Error Detection Registers

Register	Function
32-bit signature register	This register contains the CRC signature. The signature register contains the result of the user mode calculated CRC value compared against the pre-calculated CRC value. If no errors are detected, the signature register is all zeros. A non-zero signature register indicates an error in the configuration CRAM contents.
	The CRC_ERROR signal is derived from the contents of this register.
32-bit storage register	This register is loaded with the 32-bit pre-computed CRC signature at the end of the configuration stage. The signature is then loaded into the 32-bit CRC circuit (called the Compute and Compare CRC block, as shown in Figure 9–1) during user mode to calculate the CRC error. This register forms a 32-bit scan chain during execution of the CHANGE_EDREG JTAG instruction. The CHANGE_EDREG JTAG instruction can change the content of the storage register. Therefore, the functionality of the error detection CRC circuitry is checked in-system by executing the instruction to inject an error during the operation. The operation of the device is not halted when issuing the CHANGE_EDREG instruction.

Error Detection Timing

When the error detection CRC feature is enabled through the Quartus II software, the device automatically activates the CRC process upon entering user mode after configuration and initialization is complete.

The CRC_ERROR pin is driven low until the error detection circuitry detects a corrupted bit in the previous CRC calculation. After the pin goes high, it remains high during the next CRC calculation. This pin does not log the previous CRC calculation. If the new CRC calculation does not contain any corrupted bits, the CRC_ERROR pin is driven low. The error detection runs until the device is reset.

The error detection circuitry runs off an internal configuration oscillator with a divisor that sets the maximum frequency.

Table 9–5 lists the minimum and maximum error detection frequencies.

Table 9–5. Minimum and Maximum Error Detection Frequencies for Cyclone IV Devices

Error Detection	Maximum Error	Minimum Error	Valid Divisors (2ª)
Frequency	Detection Frequency	Detection Frequency	
80 MHz/2 ⁿ	80 MHz	312.5 kHz	0, 1, 2, 3, 4, 5, 6, 7, 8

You can set a lower clock frequency by specifying a division factor in the Quartus II software (for more information, refer to "Software Support"). The divisor is a power of two (2), where n is between 0 and 8. The divisor ranges from one through 256. Refer to Equation 9–1.

Equation 9-1.

ror detection frequency	=	80 MH
in accelering accelering		2^n

CRC calculation time depends on the device and the error detection clock frequency.

Document Revision History

Table 10–3 lists the revision history for this chapter.

Table 10–3. Document Revision History

Date	Version	Changes
December 2013	1.3	 Updated the "EXTEST_PULSE" section.
November 2011	1.0	 Updated the "BST Operation Control" section.
November 2011 1.2		■ Updated Table 10–2.
	2010 1.1	 Added Cyclone IV E devices in Table 10–1 and Table 10–2 for the Quartus II software version 9.1 SP1 release.
February 2010		■ Updated Figure 10–1 and Figure 10–2.
		 Minor text edits.
November 2009	1.0	Initial release.

 Bit reversal—reverses the transmit bit order from LSB-to-MSB (default) to MSB-to-LSB at the input to the serializer. For example, input data to serializer D[7..0] is rewired to D[0..7] for 8-bit data width, and D[9..0] is rewired to D[0..9] for 10-bit data width. Figure 1–10 shows the transmitter bit reversal feature.



Figure 1–10. Transmitter Bit Reversal Operation in Basic Single-Width Mode

- Input bit-flip—reverses the bit order at a byte level at the input of the transmitter phase compensation FIFO. For example, if the 16-bit parallel transmitter data at the tx_datain port is '10111100 10101101' (16'hBCAD), selecting this option reverses the input data to the transmitter phase compensation FIFO to '00111101 10110101' (16'h3DB5).
- Bit-slip control—delays the data transmission by a number of specified bits to the serializer with the tx_bitslipboundaryselect port. For usage details, refer to the "Transmit Bit-Slip Control" on page 1–76.

Serializer

The serializer converts the low-speed parallel 8-bit or 10-bit data from the transmitter PCS to high-speed serial data for the transmitter output buffer. The serializer operates with a high-speed clock at half of the serial data rate. The serializer transmission sequence is LSB to MSB.

Receiver polarity inversion—corrects accidental swapped positive and negative signals from the serial differential link during board layout. This feature works by inverting the polarity of every bit of the input data word to the word aligner, which has the same effect as swapping the positive and negative signals of the differential link. Inversion is dynamically controlled using rx_invpolarity port. Figure 1–19 shows the receiver polarity inversion feature.

Figure 1–19. Receiver Polarity Inversion



The generic receiver polarity inversion feature is different from the PCI Express (PIPE) 8B/10B polarity inversion feature. The generic receiver polarity inversion feature inverts the polarity of the data bits at the input of the word aligner and is not available in PCI Express (PIPE) mode. The PCI Express (PIPE) 8B/10B polarity inversion feature inverts the polarity of the data bits at the input of the 8B/10B decoder and is available only in PCI Express (PIPE) mode.

The rx_invpolarity signal is dynamic and might cause initial disparity errors in an 8B/10B encoded link. The downstream system must be able to tolerate these disparity errors.

Receiver bit reversal—by default, the Cyclone IV GX receiver assumes LSB to MSB transmission. If the link transmission order is MSB to LSB, the receiver forwards the incorrect reverse bit-ordered version of the parallel data to the FPGA fabric on the rx_dataout port. The receiver bit reversal feature is available to correct this situation. This feature is static in manual alignment and automatic

Configuring the hard IP module requires using the PCI Express Compiler. When configuring the transceiver for PCIe implementation with hard IP module, the byte serializer and deserializer are not enabled, providing an 8-bit transceiver-PIPE-hard IP data interface width running at 250 MHz clock frequency.

To For more information about PCIe implementation with hard IP module, refer to the *PCI Express Compiler User Guide*.

Figure 1–49 shows the transceiver configuration in PIPE mode.

Functional Mode	PCI Express (PIPE)
Channel Bonding	×1, ×2, ×4
Low-Latency PCS	Disabled
Word Aligner (Pattern Length)	Automatic Synchronization State Machine (10-Bit)
8B/10B Encoder/Decoder	Enabled
Rate Match FIFO	Enabled
Byte SERDES	Enabled
Data Rate (Gbps)	2.5
Byte Ordering	Disabled
FPGA Fabric-to-Transceiver Interface Width	↓ 16-Bit
FPGA Fabric-to-Transceiver Interface Frequency (MHz)	125

Figure 1–49. Transceiver Configuration in PIPE Mode

When configuring the transceiver into PIPE mode using ALTGX megafunction for PCIe implementation, the PHY-MAC, data link and transaction layers must be implemented in user logics. The PCIe hard IP block is bypassed in this configuration.

Port Name	Input/ Output		Description		
		This is an optional pre-emphasis write control for the transmit buffer. Depending on what value you set at this input, the controller dynamically writes the value to the pre-emphasis control register of the transmit buffer.			
		The width of this signal is fixed to 5 bits if you enable either the Use 'logical_channel_address' port for Analog controls reconfiguration option or the Use same control signal for all the channels option in the Analog controls screen. Otherwise, the width of this signal is 5 bits per channel.			
		tx_preemp[40]	Corresponding ALTGX instance settings	Corresponding pre- emphasis setting (mA)	
		00000	0	Disabled	
		00001	1	0.5	
tx preemp[40] (1)	Input	00101	5	1.0	
		01001	9	1.5	
		01101	13	2.0	
		10000	16	2.375	
		10001	17	2.5	
		10010	18	2.625	
		10011	19	2.75	
		10100	20	2.875	
		10101	21	3.0	
		All other values $=> N_{i}$	Ά		
		This is an optional wr the PMA.	ite control to write an equalization cont	rol value for the receive side of	
		The width of this signal is fixed to 4 bits if you enable either the Use 'logical_channel_address' port for Analog controls reconfiguration option of same control signal for all the channels option in the Analog controls screen the width of this signal is 4 bits per channel.		the Use iguration option or the Use og controls screen. Otherwise,	
rx_eqctrl[30] ⁽¹⁾	Input	<pre>rx_eqctrl[30]</pre>	Corresponding ALTGX instance setting	ngs	
		0001	Low		
		0101	Medium Low		
		0100	Medium High		
		0111	High		
All other values => N/A					

Table 3–2. Dynamic Reconfiguration Controller Port List (ALTGX_RECONFIG Instance) (Part 5 of 7)

Read Transaction

If you want to read the existing values from a specific channel connected to the ALTGX_RECONFIG instance, observe the corresponding byte positions of the PMA control output port after the read transaction is completed.

For example, if the number of channels controlled by the ALTGX_RECONFIG is two, the tx_vodctrl_out is 6 bits wide. The tx_vodctrl_out[2:0] signal corresponds to channel 1 and the tx vodctrl_out[5:3] signal corresponds to channel 2.

To complete a read transaction to the $\rm V_{OD}$ values of the second channel, perform the following steps:

- 1. Before you initiate a read transaction, set the rx_tx_duplex_sel port to **2'b10** so that only the transmit PMA controls are read from the transceiver channel.
- 2. Ensure that the busy signal is low before you start a read transaction.
- 3. Assert the read signal for one reconfig_clk clock cycle. This initiates the read transaction.
- 4. The busy output status signal is asserted high to indicate that the dynamic reconfiguration controller is busy reading the PMA control settings.
- 5. When the read transaction has completed, the busy signal goes low. The data_valid signal is asserted, indicating that the data available at the read control signal is valid.
- 6. To read the current V_{OD} values in channel 2, observe the values in tx_vodctrl_out[5:3].

In the waveform example shown in Figure 3–7, the transmit V_{OD} settings written in channels 1 and 2 prior to the read transaction are 3'b001 and 3'b010, respectively.

Figure 3-7. Read Transaction Waveform—Use the same control signal for all the channels Option Enabled



Note to Figure 3-7:

(1) In this waveform example, you want to read from only the transmitter portion of all the channels.

Simultaneous write and read transactions are not allowed.

Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.



Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

Symbol	Parameter	Min	Max	Unit
V _{CCINT}	Core voltage, PCI Express [®] (PCIe [®]) hard IP block, and transceiver physical coding sublayer (PCS) power supply	-0.5	1.8	V
V _{CCA}	Phase-locked loop (PLL) analog power supply	-0.5	3.75	V
V _{CCD_PLL}	PLL digital power supply	-0.5	1.8	V
V _{CCIO}	I/O banks power supply	-0.5	3.75	V
V_{CC_CLKIN}	Differential clock input pins power supply	-0.5	4.5	V
V_{CCH_GXB}	Transceiver output buffer power supply	-0.5	3.75	V
V _{CCA_GXB}	Transceiver physical medium attachment (PMA) and auxiliary power supply	-0.5	3.75	V
V _{CCL_GXB}	Transceiver PMA and auxiliary power supply	-0.5	1.8	V
VI	DC input voltage	-0.5	4.2	V
I _{OUT}	DC output current, per pin	-25	40	mA
T _{STG}	Storage temperature	-65	150	0°
TJ	Operating junction temperature	-40	125	O°

Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices (1)

Note to Table 1-1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.