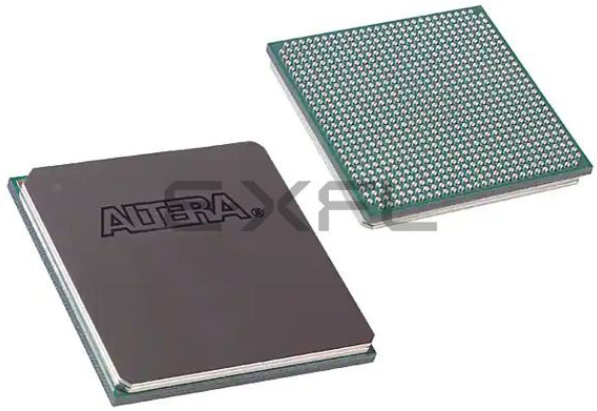

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

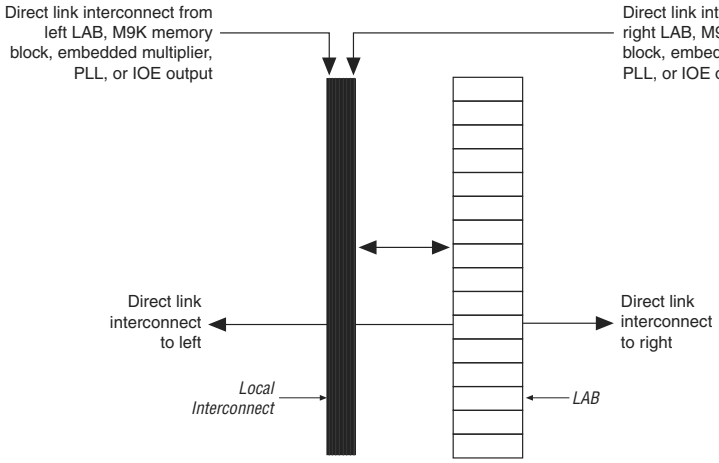
Details	
Product Status	Active
Number of LABs/CLBs	1803
Number of Logic Elements/Cells	28848
Total RAM Bits	608256
Number of I/O	532
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce30f29c7n

LAB Interconnects

The LAB local interconnect is driven by column and row interconnects and LE outputs in the same LAB. Neighboring LABs, phase-locked loops (PLLs), M9K RAM blocks, and embedded multipliers from the left and right can also drive the local interconnect of a LAB through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive up to 48 LEs through fast local and direct link interconnects.

Figure 2–5 shows the direct link connection.

Figure 2–5. Cyclone IV Device Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include:

- Two clocks
- Two clock enables
- Two asynchronous clears
- One synchronous clear
- One synchronous load

You can use up to eight control signals at a time. Register packing and synchronous load cannot be used simultaneously.

Each LAB can have up to four non-global control signals. You can use additional LAB control signals as long as they are global signals.

Synchronous clear and load signals are useful for implementing counters and other functions. The synchronous clear and synchronous load signals are LAB-wide signals that affect all registers in the LAB.

Clock Feedback Modes

Cyclone IV PLLs support up to five different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. For the supported feedback modes, refer to Table 5–5 on page 5–18 for Cyclone IV GX PLLs and Table 5–6 on page 5–19 for Cyclone IV E PLLs.

☞ Input and output delays are fully compensated by the PLL only if you are using the dedicated clock input pins associated with a given PLL as the clock sources.

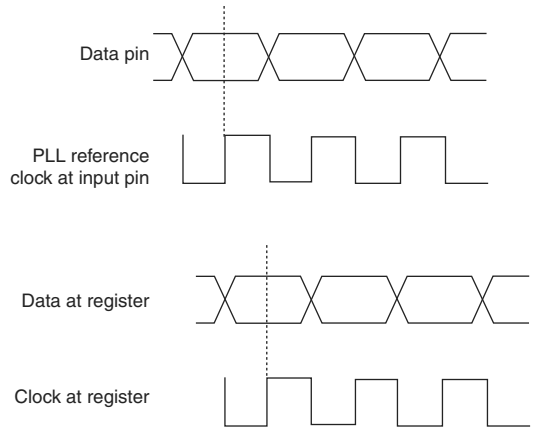
When driving the PLL using the GCLK network, the input and output delays may not be fully compensated in the Quartus II software.

Source-Synchronous Mode

If the data and clock arrive at the same time at the input pins, the phase relationship between the data and clock remains the same at the data and clock ports of any I/O element input register.

Figure 5–12 shows an example waveform of the data and clock in this mode. Use this mode for source-synchronous data transfers. Data and clock signals at the I/O element experience similar buffer delays as long as the same I/O standard is used.

Figure 5–12. Phase Relationship Between Data and Clock in Source-Synchronous Mode



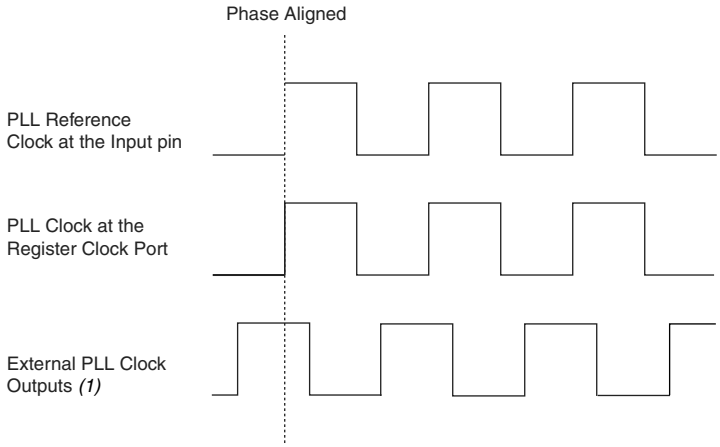
Source-synchronous mode compensates for delay of the clock network used, including any difference in the delay between the following two paths:

- Data pin to I/O element register input
- Clock input pin to the PLL phase frequency detector (PFD) input

☞ Set the input pin to the register delay chain in the I/O element to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL. Also, all data pins must use the **PLL COMPENSATED logic** option in the Quartus II software.

Figure 5–14 shows a waveform example of the phase relationship of the PLL clocks in this mode.

Figure 5–14. Phase Relationship Between PLL Clocks in Normal Mode



Note to Figure 5–14:

(1) The external clock output can lead or lag the PLL internal clock signals.

Zero Delay Buffer Mode

In zero delay buffer (ZDB) mode, the external clock output pin is phase-aligned with the clock input pin for zero delay through the device. When using this mode, use the same I/O standard on the input clock and output clocks to guarantee clock alignment at the input and output pins.

Figure 5–15 shows an example waveform of the phase relationship of the PLL clocks in ZDB mode.

Figure 5–15. Phase Relationship Between PLL Clocks in ZDB Mode

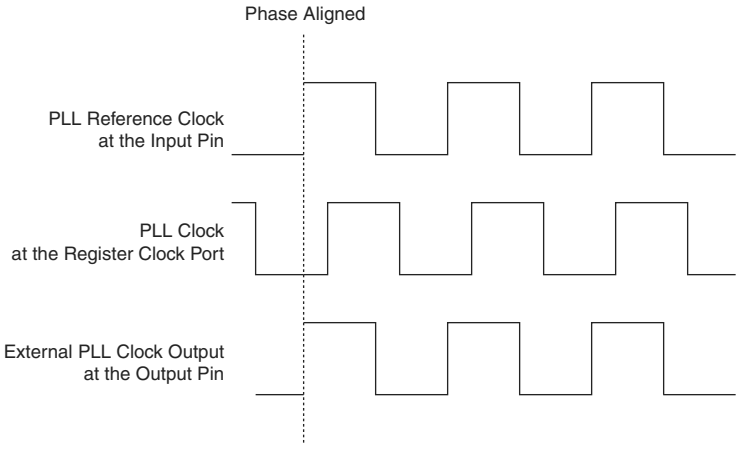


Table 5–10. Loop Filter Control of High Frequency Capacitor

LFC[1]	LFC[0]	Setting (Decimal)
0	0	0
0	1	1
1	1	3

Bypassing a PLL Counter

Bypassing a PLL counter results in a divide (N, C0 to C4 counters) factor of one.

Table 5–11 lists the settings for bypassing the counters in PLLs of Cyclone IV devices.

Table 5–11. PLL Counter Settings

PLL Scan Chain Bits [0..8] Settings									Description
LSB								MSB	
X	X	X	X	X	X	X	X	1 (1)	PLL counter bypassed
X	X	X	X	X	X	X	X	0 (1)	PLL counter not bypassed

Note to Table 5–11:

(1) Bypass bit.

To bypass any of the PLL counters, set the bypass bit to 1. The values on the other bits are then ignored.

Dynamic Phase Shifting

The dynamic phase shifting feature allows the output phase of individual PLL outputs to be dynamically adjusted relative to each other and the reference clock without sending serial data through the scan chain of the corresponding PLL. This feature simplifies the interface and allows you to quickly adjust t_{CO} delays by changing output clock phase shift in real time. This is achieved by incrementing or decrementing the VCO phase-tap selection to a given C counter or to the M counter. The phase is shifted by 1/8 the VCO frequency at a time. The output clocks are active during this phase reconfiguration process.

Table 5–12 lists the control signals that are used for dynamic phase shifting.

Table 5–12. Dynamic Phase Shifting Control Signals (Part 1 of 2)

Signal Name	Description	Source	Destination
`phasecounterselect[2..0]`	Counter Select. Three bits decoded to select either the M or one of the C counters for phase adjustment. One address map to select all C counters. This signal is registered in the PLL on the rising edge of `scanclk`.	Logic array or I/O pins	PLL reconfiguration circuit
`phaseupdown`	Selects dynamic phase shift direction; 1= UP, 0 = DOWN. Signal is registered in the PLL on the rising edge of `scanclk`.	Logic array or I/O pins	PLL reconfiguration circuit
`phasestep`	Logic high enables dynamic phase shifting.	Logic array or I/O pins	PLL reconfiguration circuit

Designing with LVDS

Cyclone IV I/O banks support the LVDS I/O standard. The Cyclone IV GX right I/O banks support true LVDS transmitters while the Cyclone IV E left and right I/O banks support true LVDS transmitters. On the top and bottom I/O banks, the emulated LVDS transmitters are supported using two single-ended output buffers with external resistors. One of the single-ended output buffers is programmed to have opposite polarity. The LVDS receiver requires an external 100-Ω termination resistor between the two signals at the input buffer.

Figure 6–12 shows a point-to-point LVDS interface using Cyclone IV devices true LVDS output and input buffers.

Figure 6–12. Cyclone IV Devices LVDS Interface with True Output Buffer on the Right I/O Banks

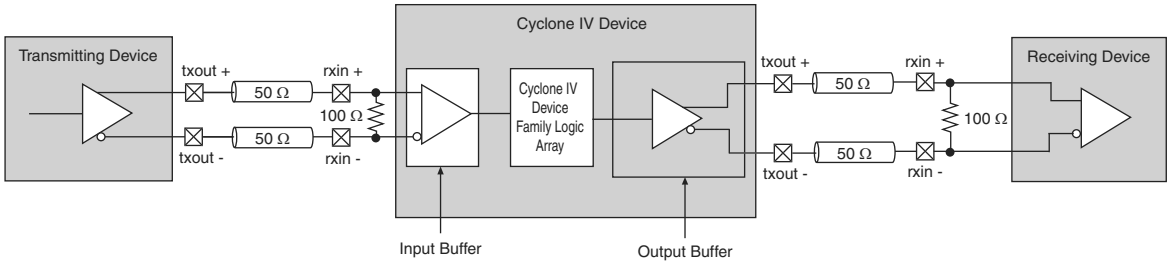
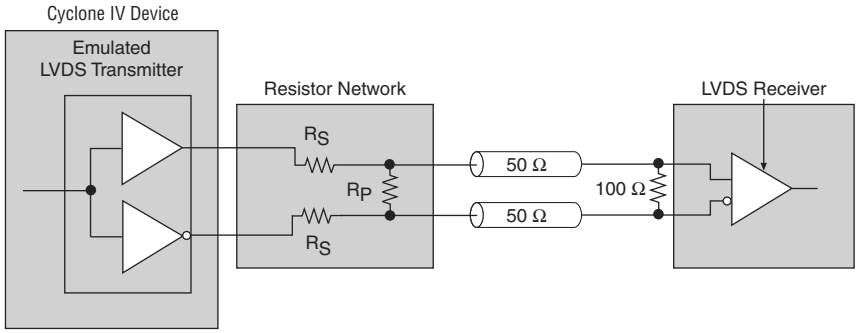


Figure 6–13 shows a point-to-point LVDS interface with Cyclone IV devices LVDS using two single-ended output buffers and external resistors.

Figure 6–13. LVDS Interface with External Resistor Network on the Top and Bottom I/O Banks *(1)*



Note to Figure 6–13:

(1) R_S = 120 Ω. R_P = 170 Ω.

BLVDS I/O Standard Support in Cyclone IV Devices

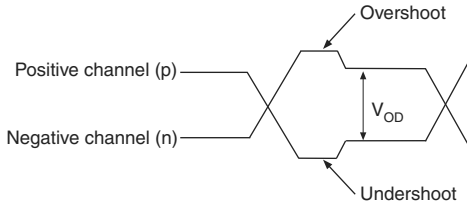
The BLVDS I/O standard is a high-speed differential data transmission technology that extends the benefits of standard point-to-point LVDS to multipoint configuration that supports bidirectional half-duplex communication. BLVDS differs from standard LVDS by providing a higher drive to achieve similar signal swings at the receiver while loaded with two terminations at both ends of the bus.

before the next edge; this may lead to pattern-dependent jitter. With pre-emphasis, the output current is momentarily boosted during switching to increase the output slew rate. The overshoot produced by this extra switching current is different from the overshoot caused by signal reflection. This overshoot happens only during switching, and does not produce ringing.

The Quartus II software allows two settings for programmable pre-emphasis control—**0** and **1**, in which **0** is pre-emphasis off and **1** is pre-emphasis on. The default setting is **1**. The amount of pre-emphasis needed depends on the amplification of the high-frequency components along the transmission line. You must adjust the setting to suit your designs, as pre-emphasis decreases the amplitude of the low-frequency component of the output signal.

Figure 6–20 shows the differential output signal with pre-emphasis.

Figure 6–20. The Output Signal with Pre-Emphasis



High-Speed I/O Timing

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Cyclone IV devices. Timing for source-synchronous signaling is based on skew between the data and clock signals.

High-speed differential data transmission requires timing parameters provided by IC vendors and requires you to consider the board skew, cable skew, and clock jitter. This section provides information about high-speed I/O standards timing parameters in Cyclone IV devices.

Table 6–11 defines the parameters of the timing diagram shown in Figure 6–21.

Table 6–11. High-Speed I/O Timing Definitions (Part 1 of 2)

Parameter	Symbol	Description
Transmitter channel-to-channel skew *(1)*	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. $T_{SW} = T_{SU} + T_{hd}$ + PLL jitter.
Time unit interval	TUI	The TUI is the data-bit timing budget allowed for skew, propagation delays, and data sampling window.
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: $RSKM = \frac{(TUI - SW - TCCS}{2}$

implements either a high-speed deserializer receiver or a high-speed serializer transmitter. There is a list of parameters in the ALTLVDS megafunction that you can set to customize your SERDES based on your design requirements. The megafunction is optimized to use Cyclone IV devices resources to create high-speed I/O interfaces in the most effective manner.

When you use Cyclone IV devices with the ALTLVDS megafunction, the interface always sends the MSB of your parallel data first.

For more details about designing your high-speed I/O systems interfaces using the ALTLVDS megafunction, refer to the *ALTLVDS Megafunction User Guide* and the *Quartus II Handbook*.

Document Revision History

Table 6–12 lists the revision history for this chapter.

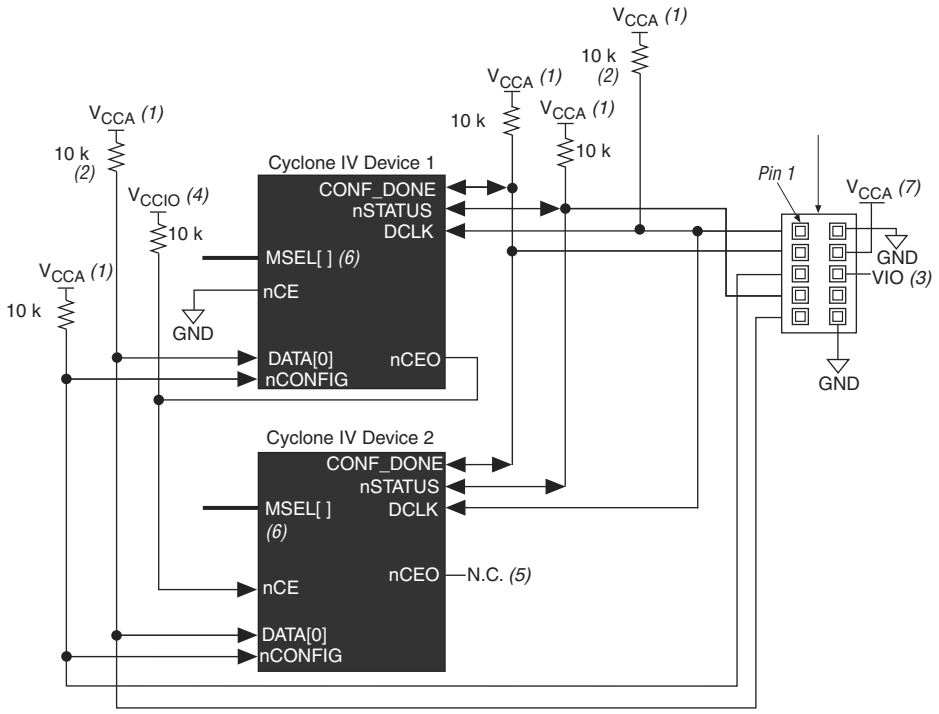
Table 6–12. Document Revision History (Part 1 of 2)

Date	Version	Changes
March 2016	2.7	■ Updated Table 6–5 and Table 6–9 to remove support for the N148 package.
May 2013	2.6	■ Updated Table 6–2 by adding Note (9). ■ Updated Table 6–4 and Table 6–8 to add new device options and packages.
February 2013	2.5	Updated Table 6–4 and Table 6–8 to add new device options and packages.
October 2012	2.4	■ Updated "I/O Banks" and "High Speed Serial Interface (HSSI) Input Reference Clock Support " sections. ■ Updated Table 6–3 and Table 6–5. ■ Updated Figure 6–10.
November 2011	2.3	■ Updated "Differential SSTL I/O Standard Support in Cyclone IV Devices" and "Differential HSTL I/O Standard Support in Cyclone IV Devices" sections. ■ Updated Table 6–1, Table 6–8, and Table 6–9. ■ Updated Figure 6–1.
December 2010	2.2	■ Updated for the Quartus II software version 10.1 release. ■ Added Cyclone IV E new device package information. ■ Added "Clock Pins Functionality" section. ■ Updated Table 6–4 and Table 6–8. ■ Minor text edits.
July 2010	2.1	■ Updated "Cyclone IV I/O Elements", "Programmable Pull-Up Resistor", "I/O Banks", "High-Speed I/O Interface", and "Designing with BLVDS" sections. ■ Updated Table 6–6 and Table 6–7. ■ Updated Figure 6–19.

You can use a download cable to configure multiple Cyclone IV device configuration pins. nCONFIG, nSTATUS, DCLK, DATA[0], and CONF_DONE are connected to every device in the chain. All devices in the chain utilize and enter user mode at the same time because all CONF_DONE pins are tied together.

In addition, the entire chain halts configuration if any device detects an error because the nSTATUS pins are tied together. Figure 8–18 shows the PS configuration for multiple Cyclone IV devices using a MasterBlaster, USB-Blaster, ByteBlaster II, or ByteBlasterMV cable.

Figure 8–18. Multi-Device PS Configuration Using a Download Cable



Notes to Figure 8–18:

(1) You must connect the pull-up resistor to the same supply voltage as the V_{CCA} supply.

(2) The pull-up resistors on DATA[0] and DCLK are only required if the download cable is the only configuration scheme used on your board. This ensures that DATA[0] and DCLK are not left floating after configuration. For example, if you also use a configuration device, the pull-up resistors on DATA[0] and DCLK are not required.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. When using the ByteBlasterMV download cable, this pin is a no connect. When using USB-Blaster, ByteBlaster II, and EthernetBlaster cables, this pin is connected to nCE when it is used for AS programming. Otherwise, it is a no connect.

(4) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.

(5) The nCEO pin of the last device in the chain is left unconnected or used as a user I/O pin.

(6) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL for PS configuration schemes, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.

(7) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5 V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

FPP Configuration

The FPP configuration in Cyclone IV devices is designed to meet the increasing demand for faster configuration time. Cyclone IV devices are designed with the capability of receiving byte-wide configuration data per clock cycle.

You can perform FPP configuration of Cyclone IV devices with an intelligent host, such as a MAX II device or microprocessor with flash memory. If your system already contains a CFI flash memory, you can use it for the Cyclone IV device configuration storage as well. The MAX II PFL feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone IV device.

For more information about the PFL, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

FPP configuration is supported in EP4CGX30 (only for F484 package), EP4CGX50, EP4CGX75, EP4CGX110, EP4CGX150, and all Cyclone IV E devices.

The FPP configuration is not supported in E144 package of Cyclone IV E devices.

Cyclone IV devices do not support enhanced configuration devices for FPP configuration.

FPP Configuration Using an External Host

FPP configuration using an external host provides a fast method to configure Cyclone IV devices. In the FPP configuration scheme, you can use an external host device to control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone IV device. You can store configuration data in an **.rbf**, **.hex**, or **.ttf** format. When using the external host, a design that controls the configuration process, such as fetching the data from flash memory and sending it to

IEEE Std. 1149.6 Boundary-Scan Register

The boundary-scan cell (BSC) for HSSI transmitters (GXB_TX[p,n]) and receivers (GXB_RX[p,n]) in Cyclone IV GX devices are different from the BSCs for I/O pins.

Figure 10–1 shows the Cyclone IV GX HSSI transmitter boundary-scan cell.

Figure 10–1. HSSI Transmitter BSC with IEEE Std. 1149.6 BST Circuitry for Cyclone IV GX Devices

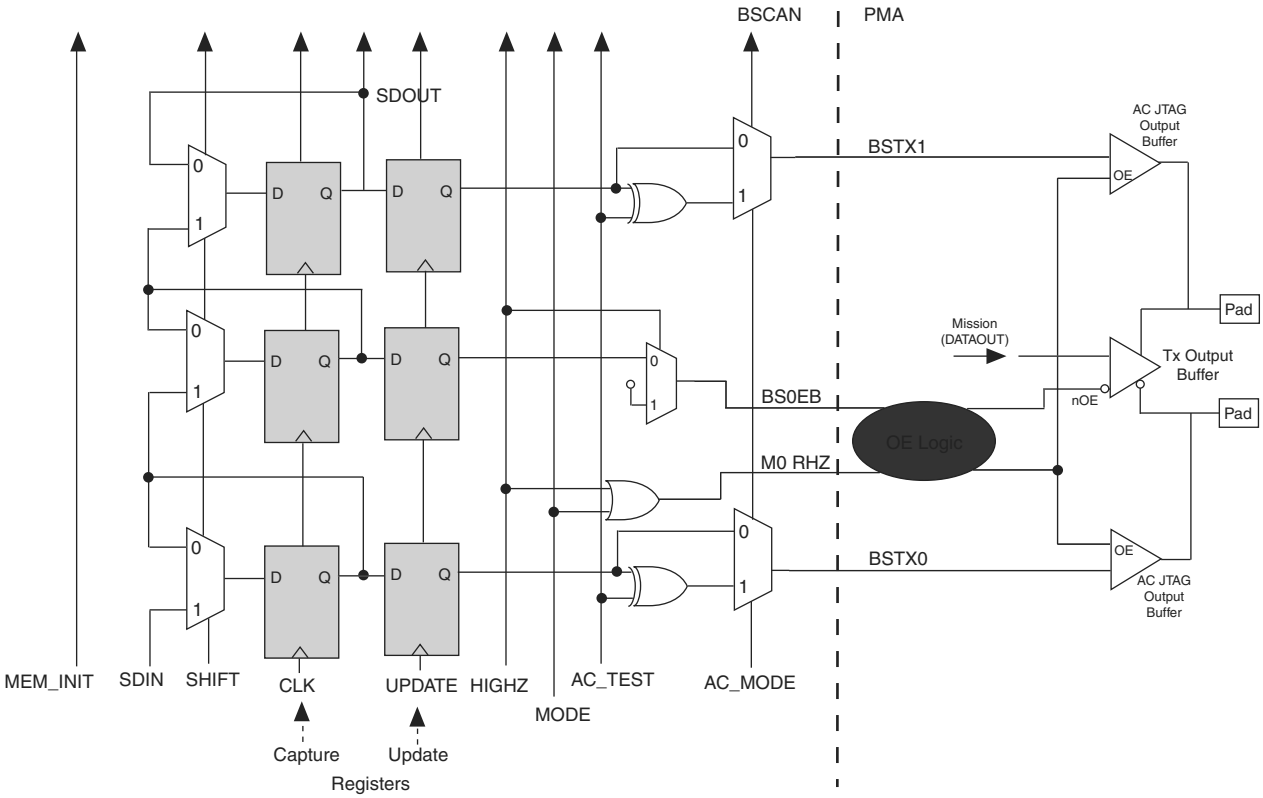
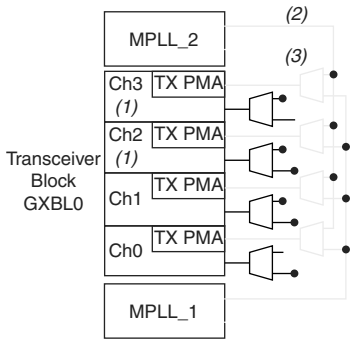


Figure 1–31 and Figure 1–32 show the high- and low-speed clock distribution for transceivers in F324 and smaller packages, and in F484 and larger packages in non-bonded channel configuration.

Figure 1–31. Clock Distribution in Non-Bonded Channel Configuration for Transceivers in F324 and Smaller Packages



Notes to Figure 1–31:

(1) Transceiver channels 2 and 3 are not available for devices in F169 and smaller packages.
(2) High-speed clock.
(3) Low-speed clock.

Fast Recovery from P0s State

The PCIe protocol defines fast training sequences for bit and byte synchronization to transition from L0s to L0 (PIPE P0s to P0) power states. The PHY must acquire bit and byte synchronization when transitioning from L0s to L0 state between 16 ns to 4 µs. Each Cyclone IV GX receiver channel has built-in fast recovery circuit that allows the receiver to meet the requirement when enabled.

Electrical Idle Inference

In PIPE mode, the Cyclone IV GX transceiver supports inferring the electrical idle condition at each receiver instead of detecting the electrical idle condition using analog circuitry, as defined in the version 2.0 of PCIe Base Specification. The inference is supported using `rx_elecidleinfersel[2..0]` port, with valid driven values as listed in Table 1–17 in each link training and status state machine substate.

Table 1–17. Electrical Idle Inference Conditions

rx_elecidleinfersel [2..0]	Link Training and Status State Machine State	Description
3'b100	L0	Absence of `update_FC` or alternatively skip ordered set in 128 µs window
3'b101	Recovery.RcvrCfg	Absence of `TS1` or `TS2` ordered set in 1280 UI interval
3'b101	Recovery.Speed when successful speed negotiation = 1'b1	Absence of `TS1` or `TS2` ordered set in 1280 UI interval
3'b110	Recovery.Speed when successful speed negotiation = 1'b0	Absence of an exit from electrical idle in 2000 UI interval
3'b111	Loopback.Active (as slave)	Absence of an exit from electrical idle in 128 µs window

The electrical idle inference module drives the `pipeelecidle` signal high in each receiver channel when an electrical idle condition is inferred. The electrical idle inference module cannot detect electrical idle exit condition based on the reception of the electrical idle exit ordered set, as specified in the PCI Express (PIPE) Base Specification.

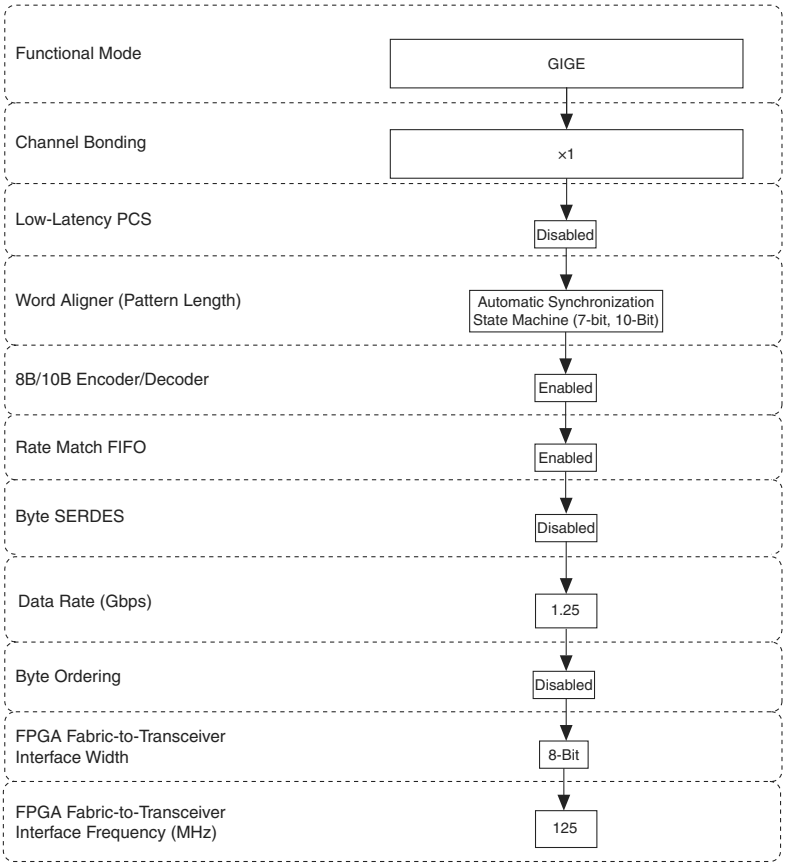
When enabled, the electrical idle inference block uses electrical idle ordered set detection from the fast recovery circuitry to drive the `pipeelecidle` signal.

Compliance Pattern Transmission

In PIPE mode, the Cyclone IV GX transceiver supports compliance pattern transmission which requires the first /K28.5/ code group of the compliance pattern to be encoded with negative current disparity. This requirement is supported using a `tx_forcedispcompliance` port that when driven with logic high, the transmitter data on the `tx_datain` port is transmitted with negative current running disparity.

Figure 1–56 shows the transceiver configuration in GIGE mode.

Figure 1–56. Transceiver Configuration in GIGE Mode



When configured in GIGE mode, three encoded comma (/K28.5/) code groups are transmitted automatically after deassertion of `tx_digitalreset` and before transmitting user data on the `tx_datain` port. This could affect the synchronization state machine behavior at the receiver.

Depending on when you start transmitting the synchronization sequence, there could be an even or odd number of encoded data (/Dx.y/) code groups transmitted between the last of the three automatically sent /K28.5/ code groups and the first /K28.5/ code group of the synchronization sequence. If there is an even number of /Dx.y/ code groups received between these two /K28.5/ code groups, the first /K28.5/ code group of the synchronization sequence begins at an odd code group boundary. An IEEE802.3-compliant GIGE synchronization state machine treats this as an error condition and goes into the Loss-of-Sync state.

Table 1–28. PIPE Interface Ports in ALTGX Megafunction for Cyclone IV GX (1) (Part 2 of 2)

Port Name	Input/ Output	Clock Domain	Description
pipestatus	Output	N/A	PIPE receiver status port. ■ Signal is 3 bits wide and is encoded as follows: ■ 3'b000: Received data OK ■ 3'b001: one SKP symbol added ■ 3'b010: one SKP symbol removed ■ 3'b011: Receiver detected ■ 3'b100: 8B/10B decoder error ■ 3'b101: Elastic buffer overflow ■ 3'b110: Elastic buffer underflow ■ 3'b111: Received disparity error
rx_elecidleinfersel	Input	N/A	Controls the electrical idle inference mechanism as specified in Table 1–17 on page 1–57

Note to Table 1–28:

(1) For equivalent signals defined in PIPE 2.00 specification, refer to Table 1–15 on page 1–54.

Table 1–29. Multipurpose PLL, General Purpose PLL and Miscellaneous Ports in ALTGX Megafunction for Cyclone IV GX (Part 1 of 2)

Block	Port Name	Input/ Output	Clock Domain	Description
PLL	pll_inclk	Input	Clock signal	Input reference clock for the PLL (multipurpose PLL or general purpose PLL) used by the transceiver instance. When configured with the transmitter and receiver channel configuration in Deterministic Latency mode, multiple `pll_inclk` ports are available as follows. Configured with PLL PFD feedback—x is the number of channels selected: ■ `pll_inclk[x-1..0]` are input reference clocks for each transmitter in the transceiver instance ■ `pll_inclk[x+1..x]` are input reference clocks for receivers in the transceiver instance Configured without PLL PFD feedback: ■ `pll_inclk[0]` is input reference clock for transmitters in the transceiver instance ■ `pll_inclk[1]` is input reference clock for receivers in the transceiver instance
	pll_locked	Output	Asynchronous signal	PLL (used by the transceiver instance) lock indicator.
	pll_areset	Input	Asynchronous signal	PLL (used by the transceiver instance) reset. ■ When asserted, the PLL is kept in reset state. ■ When deasserted, the PLL is active and locks to the input reference clock.
	coreclkout	Output	Clock signal	FPGA fabric-transceiver interface clock in bonded modes.

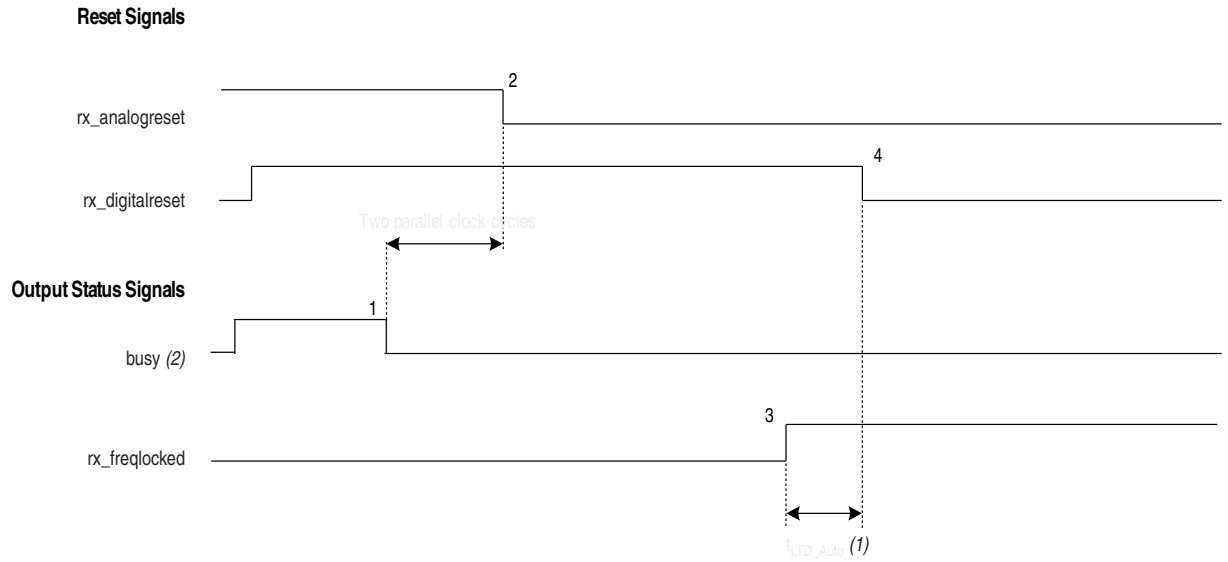
Transmitter Only Channel

This configuration contains only a transmitter channel. If you create a **Transmitter Only** instance in the ALTGX MegaWizard Plug-In Manager, use the same reset sequence shown in Figure 2–3 on page 2–7.

Receiver Only Channel—Receiver CDR in Automatic Lock Mode

This configuration contains only a receiver channel. If you create a **Receiver Only** instance in the ALTGX MegaWizard Plug-In Manager with the receiver CDR in automatic lock mode, use the reset sequence shown in Figure 2–6.

Figure 2–6. Sample Reset Sequence of Receiver Only Channel—Receiver CDR in Automatic Lock Mode



Notes to Figure 2–6:

(1) For t_{LTD_Auto} duration, refer to the *Cyclone IV Device Datasheet* chapter.

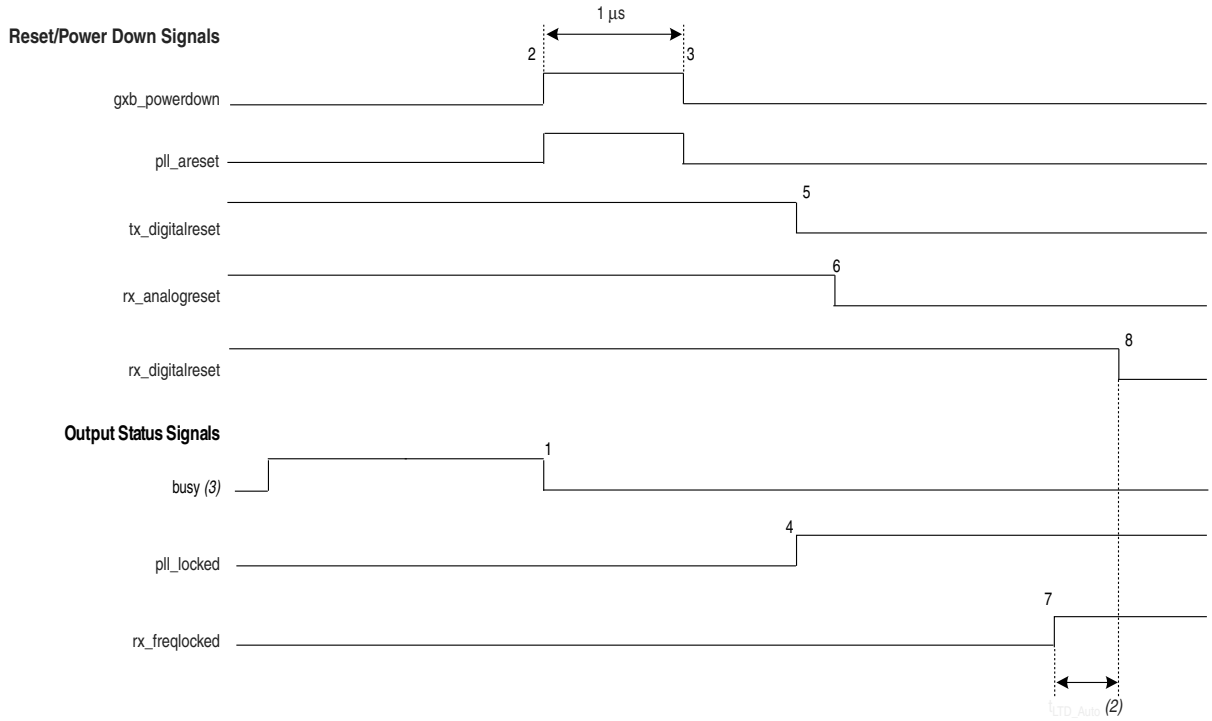
(2) The `busy` signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the `busy` signal is asserted and deasserted only if there is a read or write operation to the ALTGX_RECONFIG megafunction.

As shown in Figure 2–6, perform the following reset procedure for the receiver in CDR automatic lock mode:

1. After power up, wait for the `busy` signal to be deasserted.
2. Keep the `rx_digitalreset` and `rx_analogreset` signals asserted during this time period.
3. After the busy signal is deasserted, wait for another two parallel clock cycles, then deassert the `rx_analogreset` signal.
4. Wait for the `rx_freqlocked` signal to go high.
5. When `rx_freqlocked` goes high (marker 3), from that point onwards, wait for at least t_{LTD_Auto}, then de-assert the `rx_digitalreset` signal (marker 4). At this point, the receiver is ready to receive data.

The deassertion of the busy signal indicates proper completion of the offset cancellation process on the receiver channel.

Figure 2–13. Sample Reset Sequence of a Receiver and Transmitter Channels-Receiver CDR in Automatic Lock Mode with the Optional gxb_powerdown Signal (1)



Notes to Figure 2–13:

(1) The gxb_powerdown signal must not be asserted during the offset cancellation sequence.

(2) For t_{LTD_Auto} duration, refer to the *Cyclone IV Device Datasheet* chapter.

(3) The busy signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the busy signal is asserted and deasserted only if there is a read or write operation to the ALTGX_RECONFIG megafunction.

Simulation Requirements

The following are simulation requirements:

- The gxb_powerdown port is optional. In simulation, if the gxb_powerdown port is not instantiated, you must assert the tx_digitalreset, rx_digitalreset, and rx_analogreset signals appropriately for correct simulation behavior.
- If the gxb_powerdown port is instantiated, and the other reset signals are not used, you must assert the gxb_powerdown signal for at least 1 µs for correct simulation behavior.
- You can deassert the rx_digitalreset signal immediately after the rx_freqlocked signal goes high to reduce the simulation run time. It is not necessary to wait for t_{LTD_Auto} (as suggested in the actual reset sequence).
- The busy signal is deasserted after about 20 parallel reconfig_clk clock cycles in order to reduce simulation run time. For silicon behavior in hardware, you can follow the reset sequences described in the previous pages.

Document Revision History

Table 2–8 lists the revision history for this chapter.

Table 2–8. Document Revision History

Date	Version	Changes
September 2014	1.4	■ Removed the `rx_pll_locked` signal from the "Sample Reset Sequence of Receiver Only Channel—Receiver CDR in Manual Lock Mode" and the "Sample Reset Sequence of Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode" figures.
May 2013	1.3	■ Added rx_pll_locked to Figure 2–7 and Figure 2–9. ■ Added information on rx_pll_locked to "Receiver Only Channel—Receiver CDR in Manual Lock Mode" and "Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode".
November 2011	1.2	Updated the "All Supported Functional Modes Except the PCIe Functional Mode" section.
December 2010	1.1	■ Updated for the Quartus II software version 10.1 release. ■ Updated all `pll_powerdown` to `pll_areset`. ■ Added information about the `busy` signal in Figure 2–4, Figure 2–5, Figure 2–6, Figure 2–7, Figure 2–8, Figure 2–9, Figure 2–10, Figure 2–12, and Figure 2–13. ■ Added information for clarity ("Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode", "Receiver Only Channel—Receiver CDR in Automatic Lock Mode", "Receiver Only Channel—Receiver CDR in Manual Lock Mode", "Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode", and "Reset Sequence in Channel Reconfiguration Mode"). ■ Minor text edits.
July 2010	1.0	Initial release.

Section I. Device Datasheet

This section provides the Cyclone® IV device datasheet. It includes the following chapter:

- Chapter 1, Cyclone IV Device Datasheet

Revision History

Refer to each chapter for its own specific revision history. For information about when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

1. Cyclone IV Device Datasheet

CYIV-53001-2.1

This chapter describes the electrical and switching characteristics for Cyclone® IV devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

This chapter includes the following sections:

Operating Conditions

When Cyclone IV devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone IV devices, you must consider the operating requirements described in this chapter.

Cyclone IV devices are offered in commercial, industrial, extended industrial and, automotive grades. Cyclone IV E devices offer –6 (fastest), –7, –8, –8L, and –9L speed grades for commercial devices, –8L speed grades for industrial devices, and –7 speed grade for extended industrial and automotive devices. Cyclone IV GX devices offer –6 (fastest), –7, and –8 speed grades for commercial devices and –7 speed grade for industrial devices.

For more information about the supported speed grades for respective Cyclone IV devices, refer to the *Cyclone IV FPGA Device Family Overview* chapter.

Cyclone IV E devices are offered in core voltages of 1.0 and 1.2 V. Cyclone IV E devices with a core voltage of 1.0 V have an 'L' prefix attached to the speed grade.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with a "C" prefix, industrial with an "I" prefix, and automotive with an "A" prefix. Therefore, commercial devices are indicated as C6, C7, C8, C8L, or C9L per respective speed grade. Industrial devices are indicated as I7, I8, or I8L. Automotive devices are indicated as A7.