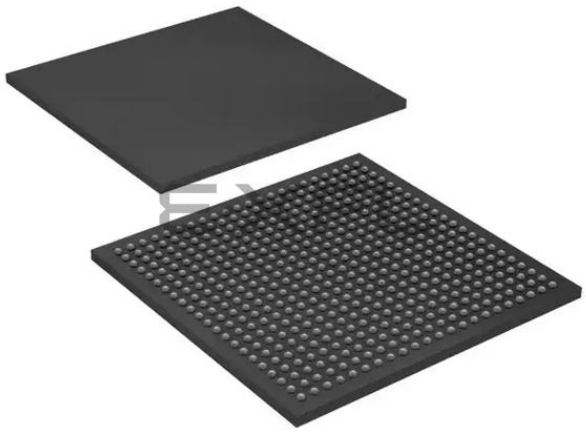

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 2475 |
| Number of Logic Elements/Cells | 39600 |
| Total RAM Bits | 1161216 |
| Number of I/O | 328 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep4ce40f23c7n |

# Document Revision History

Table 1–10 lists the revision history for this chapter.

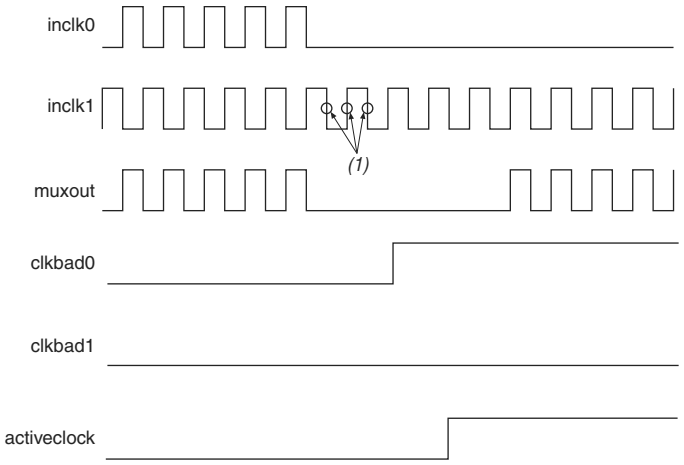
**Table 1–10. Document Revision History**

| Date | Version | Changes |
|---|---|---|
| March 2016 | 2.0 | ■ Updated Table 1–4 and Table 1–5 to remove support for the N148 package.<br>■ Updated Figure 1–2 to remove support for the N148 package. |
| April 2014 | 1.9 | Updated "Packaging Ordering Information for the Cyclone IV E Device". |
| May 2013 | 1.8 | Updated Table 1–3, Table 1–6 and Figure 1–3 to add new device options and packages. |
| February 2013 | 1.7 | Updated Table 1–3, Table 1–6 and Figure 1–3 to add new device options and packages. |
| October 2012 | 1.6 | Updated Table 1–3 and Table 1–4. |
| November 2011 | 1.5 | ■ Updated "Cyclone IV Device Family Features" section.<br>■ Updated Figure 1–2 and Figure 1–3. |
| December 2010 | 1.4 | ■ Updated for the Quartus II software version 10.1 release.<br>■ Added Cyclone IV E new device package information.<br>■ Updated Table 1–1, Table 1–2, Table 1–3, Table 1–5, and Table 1–6.<br>■ Updated Figure 1–3.<br>■ Minor text edits. |
| July 2010 | 1.3 | Updated Table 1–2 to include F484 package information. |
| March 2010 | 1.2 | ■ Updated Table 1–3 and Table 1–6.<br>■ Updated Figure 1–3.<br>■ Minor text edits. |
| February 2010 | 1.1 | ■ Added Cyclone IV E devices in Table 1–1, Table 1–3, and Table 1–6 for the Quartus II software version 9.1 SP1 release.<br>■ Added the "Cyclone IV Device Family Speed Grades" and "Configuration" sections.<br>■ Added Figure 1–3 to include Cyclone IV E Device Packaging Ordering Information.<br>■ Updated Table 1–2, Table 1–4, and Table 1–5 for Cyclone IV GX devices.<br>■ Minor text edits. |
| November 2009 | 1.0 | Initial release. |

20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. Choose the secondary clock frequency so the VCO operates in the recommended frequency range. Also, set the M, N, and C counters accordingly to keep the VCO operating frequency in the recommended range.

Figure 5–18 shows a waveform example of the switchover feature when using automatic loss of clock detection. Here, the `inclk0` signal remains low. After the `inclk0` signal remains low for approximately two clock cycles, the clock-sense circuitry drives the `clkbad0` signal high. Also, because the reference clock signal is not toggling, the switchover state machine controls the multiplexer through the `clksw` signal to switch to `inclk1`.

**Figure 5–18. Automatic Switchover Upon Clock Loss Detection** *(1)*




**Note to Figure 5–18:**

(1) Switchover is enabled on the falling edge of `inclk0` or `inclk1`, depending on which clock is available. In this figure, switchover is enabled on the falling edge of `inclk1`.

## Manual Override

If you are using the automatic switchover, you must switch input clocks with the manual override feature with the `clkswitch` input.

Figure 5–19 shows an example of a waveform illustrating the switchover feature when controlled by `clkswitch`. In this case, both clock sources are functional and `inclk0` is selected as the reference clock. A low-to-high transition of the `clkswitch` signal starts the switchover sequence. The `clkswitch` signal must be high for at least three clock cycles (at least three of the longer clock period if `inclk0` and `inclk1` have different frequencies). On the falling edge of `inclk0`, the reference clock of the counter, `muxout`, is gated off to prevent any clock glitching. On the falling edge of `inclk1`, the reference clock multiplexer switches from `inclk0` to `inclk1` as the PLL reference, and the `activeclock` signal changes to indicate which clock is currently feeding the PLL.

The IOE registers in each I/O block share the same source for the preset or clear features. You can program preset or clear for each individual IOE, but you cannot use both features simultaneously. You can also program the registers to power-up high or low after configuration is complete. If programmed to power-up low, an asynchronous clear can control the registers. If programmed to power-up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of the active-low input of another device upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

For more information about the input and output pin delay settings, refer to the *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

## PCI-Clamp Diode

Cyclone IV devices provide an optional PCI-clamp diode enabled input and output for each I/O pin. Dual-purpose configuration pins support the diode in user mode if the specific pins are not used as configuration pins for the selected configuration scheme. For example, if you are using the active serial (AS) configuration scheme, you cannot use the clamp diode on the `ASDO` and `nCSO` pins in user mode. Dedicated configuration pins do not support the on-chip diode.

The PCI-clamp diode is available for the following I/O standards:

- 3.3-V LVTTL
- 3.3-V LVCMOS
- 3.0-V LVTTL
- 3.0-V LVCMOS
- 2.5-V LVTTL/LVCMOS
- PCI
- PCI-X

If the input I/O standard is one of the listed standards, the PCI-clamp diode is enabled by default in the Quartus II software.

# OCT Support

Cyclone IV devices feature OCT to provide I/O impedance matching and termination capabilities. OCT helps prevent reflections and maintain signal integrity while minimizing the need for external resistors in high pin-count ball grid array (BGA) packages. Cyclone IV devices provide I/O driver on-chip impedance matching and $R_S$ OCT for single-ended outputs and bidirectional pins.

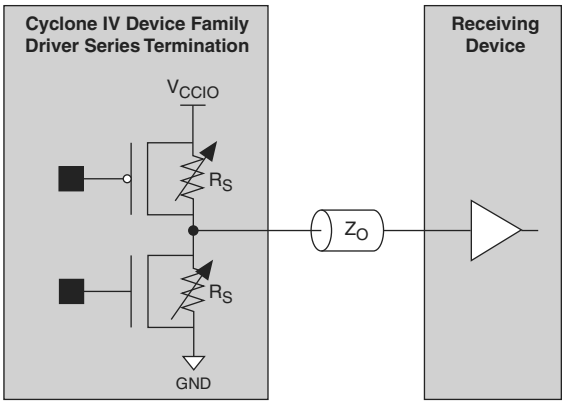
When using $R_S$ OCT, programmable current strength is not available.

There are two ways to implement OCT in Cyclone IV devices:

- OCT with calibration
- OCT without calibration

The $R_S$ shown in Figure 6–2 is the intrinsic impedance of the transistors that make up the I/O buffer.

**Figure 6–2. Cyclone IV Devices $R_S$ OCT with Calibration**




OCT with calibration is achieved using the OCT calibration block circuitry. There is one OCT calibration block in each of I/O banks 2, 4, 5, and 7 for Cyclone IV E devices and I/O banks 4, 5, and 7 for Cyclone IV GX devices. Each calibration block supports each side of the I/O banks. Because there are two I/O banks sharing the same calibration block, both banks must have the same $V_{CCIO}$ if both banks enable OCT calibration. If two related banks have different $V_{CCIO}$, only the bank in which the calibration block resides can enable OCT calibration.

Figure 6–10 on page 6–18 shows the top-level view of the OCT calibration blocks placement.

Each calibration block comes with a pair of RUP and RDN pins. When used for calibration, the RUP pin is connected to $V_{CCIO}$ through an external 25-Ω ±1% or 50-Ω ±1% resistor for an $R_S$ OCT value of 25 Ω or 50 Ω, respectively. The RDN pin is connected to GND through an external 25-Ω ±1% or 50-Ω ±1% resistor for an $R_S$ OCT value of 25 Ω or 50 Ω, respectively. The external resistors are compared with the internal resistance using comparators. The resultant outputs of the comparators are used by the OCT calibration block to dynamically adjust buffer impedance.

☞ During calibration, the resistance of the RUP and RDN pins varies.

# I/O Banks

I/O pins on Cyclone IV devices are grouped together into I/O banks. Each bank has a separate power bus.

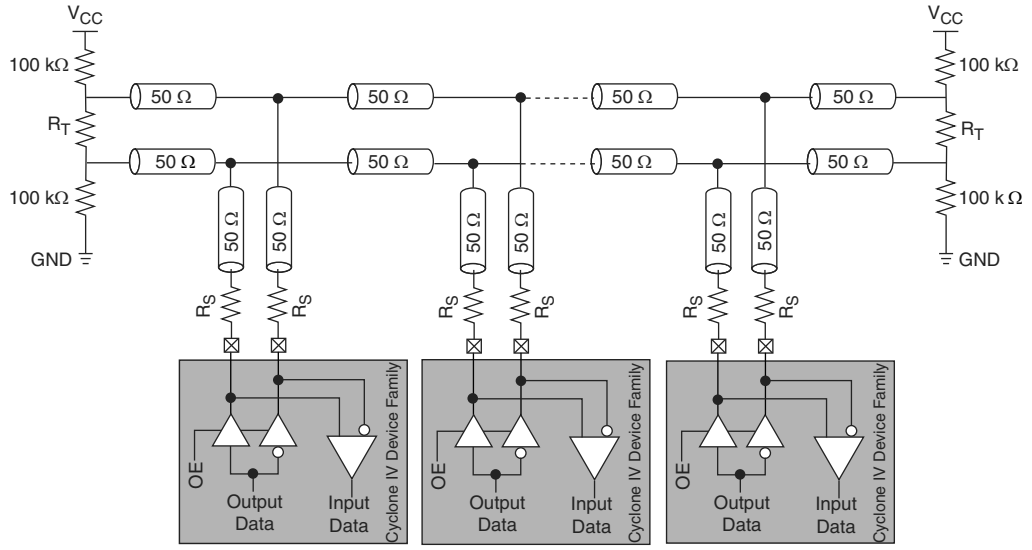
Cyclone IV E devices have eight I/O banks, as shown in Figure 6–9. Each device I/O pin is associated with one I/O bank. All single-ended I/O standards are supported in all banks except HSTL-12 Class II, which is only supported in column I/O banks. All differential I/O standards are supported in all banks. The only exception is HSTL-12 Class II, which is only supported in column I/O banks.

Cyclone IV GX devices have up to ten I/O banks and two configuration banks, as shown in Figure 6–10 on page 6–18 and Figure 6–11 on page 6–19. The Cyclone IV GX configuration I/O bank contains three user I/O pins that can be used as normal user I/O pins if they are not used in configuration modes. Each device I/O pin is associated with one I/O bank. All single-ended I/O standards are supported except HSTL-12 Class II, which is only supported in column I/O banks. All differential I/O standards are supported in top, bottom, and right I/O banks. The only exception is HSTL-12 Class II, which is only supported in column I/O banks.

The entire left side of the Cyclone IV GX devices contain dedicated high-speed transceiver blocks for high speed serial interface applications. There are a total of 2, 4, and 8 transceiver channels for Cyclone IV GX devices, depending on the density and package of the device. For more information about the transceiver channels supported, refer to Figure 6–10 on page 6–18 and Figure 6–11 on page 6–19.

Figure 6–14 shows a typical BLVDS topology with multiple transmitter and receiver pairs.

**Figure 6–14. BLVDS Topology with Cyclone IV Devices Transmitters and Receivers**




The BLVDS I/O standard is supported on the top, bottom, and right I/O banks of Cyclone IV devices. The BLVDS transmitter uses two single-ended output buffers with the second output buffer programmed as inverted, while the BLVDS receiver uses a true LVDS input buffer. The transmitter and receiver share the same pins. An output-enabled (OE) signal is required to tristate the output buffers when the LVDS input buffer receives a signal.

For more information, refer to the *Cyclone IV Device Datasheet* chapter.

## Designing with BLVDS

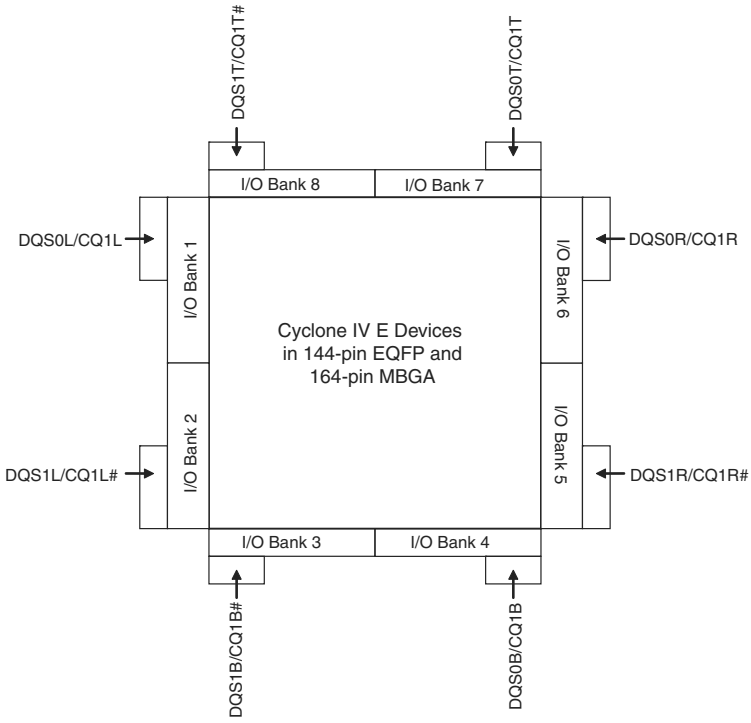
The BLVDS bidirectional communication requires termination at both ends of the bus in BLVDS. The termination resistor ($R_T$) must match the bus differential impedance, which in turn depends on the loading on the bus. Increasing the load decreases the bus differential impedance. With termination at both ends of the bus, termination is not required between the two signals at the input buffer. A single series resistor ($R_S$) is required at the output buffer to match the output buffer impedance to the transmission line impedance. However, this series resistor affects the voltage swing at the input buffer. The maximum data rate achievable depends on many factors.

Altera recommends that you perform simulation using the IBIS model while considering factors such as bus loading, termination values, and output and input buffer location on the bus to ensure that the required performance is achieved.

For more information about BLVDS interface support in Altera devices, refer to *AN 522: Implementing Bus LVDS Interface in Supported Altera Device Families*.

Figure 7–6 shows the location and numbering of the DQS, DQ, or CQ# pins in I/O banks of the Cyclone IV E device in the 144-pin EQFP and 164-pin MBGA packages.

**Figure 7–6. DQS, CQ, or CQ# Pins for Cyclone IV E Devices in the 144-Pin EQFP and 164-pin MBGA Packages**




In Cyclone IV devices, the ×9 mode uses the same DQ and DQS pins as the ×8 mode, and one additional DQ pin that serves as a regular I/O pin in the ×8 mode. The ×18 mode uses the same DQ and DQS pins as ×16 mode, with two additional DQ pins that serve as regular I/O pins in the ×16 mode. Similarly, the ×36 mode uses the same DQ and DQS pins as the ×32 mode, with four additional DQ pins that serve as regular I/O pins in the ×32 mode. When not used as DQ or DQS pins, the memory interface pins are available as regular I/O pins.

## Optional Parity, DM, and Error Correction Coding Pins

Cyclone IV devices support parity in ×9, ×18, and ×36 modes. One parity bit is available per eight bits of data pins. You can use any of the DQ pins for parity in Cyclone IV devices because the parity pins are treated and configured similarly to DQ pins.

DM pins are only required when writing to DDR2 and DDR SDRAM devices. QDR II SRAM devices use the BWS# signal to select the byte to be written into memory. A low signal on the DM or BWS# pin indicates the write is valid. Driving the DM or BWS# pin high causes the memory to mask the DQ signals. Each group of DQS and DQ signals has one DM pin. Similar to the DQ output signals, the DM signals are clocked by the -90° shifted clock.

## Configuration Scheme

A configuration scheme with different configuration voltage standards is selected by driving the MSEL pins either high or low, as shown in Table 8–3, Table 8–4, and Table 8–5.

☞ Hardwire the MSEL pins to $V_{CCA}$ or GND without pull-up or pull-down resistors to avoid problems detecting an incorrect configuration scheme. Do not drive the MSEL pins with a microprocessor or another device.

**Table 8–3. Configuration Schemes for Cyclone IV GX Devices (EP4CGX15, EP4CGX22, and EP4CGX30 [except for F484 Package])**

| Configuration Scheme | MSEL2 | MSEL1 | MSEL0 | POR Delay | Configuration Voltage Standard (V) (1) |
|---|---|---|---|---|---|
| AS | 1 | 0 | 1 | Fast | 3.3 |
| | 0 | 1 | 1 | Fast | 3.0, 2.5 |
| | 0 | 0 | 1 | Standard | 3.3 |
| | 0 | 1 | 0 | Standard | 3.0, 2.5 |
| PS | 1 | 0 | 0 | Fast | 3.3, 3.0, 2.5 |
| | 1 | 1 | 0 | Fast | 1.8, 1.5 |
| | 0 | 0 | 0 | Standard | 3.3, 3.0, 2.5 |
| JTAG-based configuration (2) | (3) | (3) | (3) | — | — |

**Notes to Table 8–3:**

(1) Configuration voltage standard applied to the $V_{CCIO}$ supply of the bank in which the configuration pins reside.

(2) JTAG-based configuration takes precedence over other configuration schemes, which means the MSEL pin settings are ignored.

(3) Do not leave the MSEL pins floating. Connect them to $V_{CCA}$ or GND. These pins support the non-JTAG configuration scheme used in production. Altera recommends connecting the MSEL pins to GND if your device is only using JTAG configuration.

**Table 8–4. Configuration Schemes for Cyclone IV GX Devices (EP4CGX30 [only for F484 package], EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150) (Part 1 of 2)**

| Configuration Scheme | MSEL3 | MSEL2 | MSEL1 | MSEL0 | POR Delay | Configuration Voltage Standard (V) (1) |
|---|---|---|---|---|---|---|
| AS | 1 | 1 | 0 | 1 | Fast | 3.3 |
| | 1 | 0 | 1 | 1 | Fast | 3.0, 2.5 |
| | 1 | 0 | 0 | 1 | Standard | 3.3 |
| | 1 | 0 | 1 | 0 | Standard | 3.0, 2.5 |
| PS | 1 | 1 | 0 | 0 | Fast | 3.3, 3.0, 2.5 |
| | 1 | 1 | 1 | 0 | Fast | 1.8, 1.5 |
| | 1 | 0 | 0 | 0 | Standard | 3.3, 3.0, 2.5 |
| | 0 | 0 | 0 | 0 | Standard | 1.8, 1.5 |
| FPP | 0 | 0 | 1 | 1 | Fast | 3.3, 3.0, 2.5 |
| | 0 | 1 | 0 | 0 | Fast | 1.8, 1.5 |
| | 0 | 0 | 0 | 1 | Standard | 3.3, 3.0, 2.5 |
| | 0 | 0 | 1 | 0 | Standard | 1.8, 1.5 |

## FPP Configuration

The FPP configuration in Cyclone IV devices is designed to meet the increasing demand for faster configuration time. Cyclone IV devices are designed with the capability of receiving byte-wide configuration data per clock cycle.

You can perform FPP configuration of Cyclone IV devices with an intelligent host, such as a MAX II device or microprocessor with flash memory. If your system already contains a CFI flash memory, you can use it for the Cyclone IV device configuration storage as well. The MAX II PFL feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone IV device.

For more information about the PFL, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

FPP configuration is supported in EP4CGX30 (only for F484 package), EP4CGX50, EP4CGX75, EP4CGX110, EP4CGX150, and all Cyclone IV E devices.

The FPP configuration is not supported in E144 package of Cyclone IV E devices.

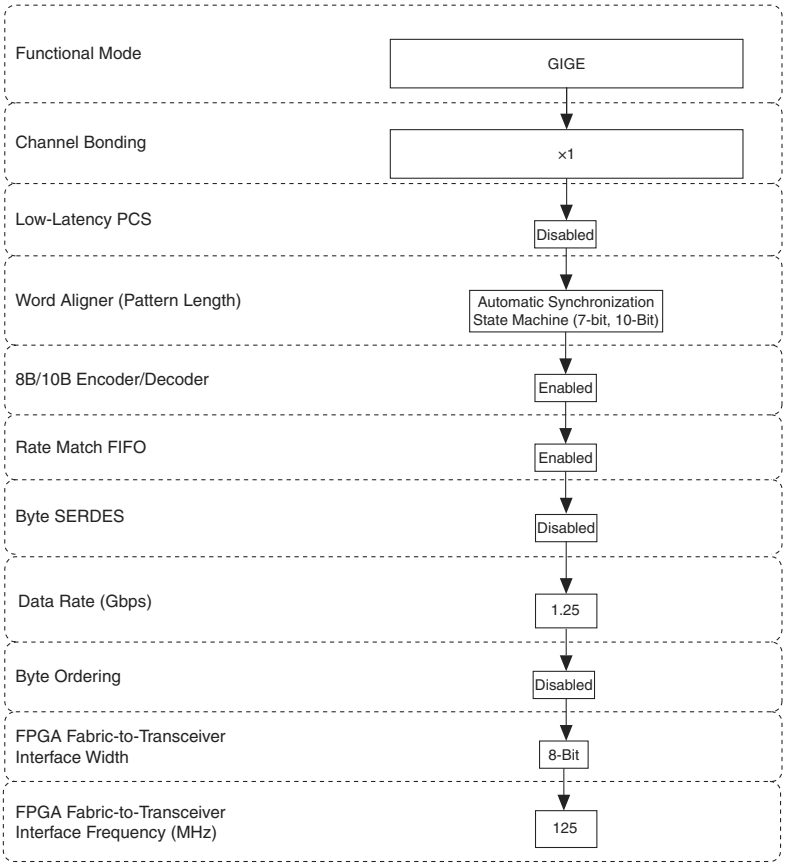
Cyclone IV devices do not support enhanced configuration devices for FPP configuration.

### FPP Configuration Using an External Host

FPP configuration using an external host provides a fast method to configure Cyclone IV devices. In the FPP configuration scheme, you can use an external host device to control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone IV device. You can store configuration data in an **.rbf**, **.hex**, or **.ttf** format. When using the external host, a design that controls the configuration process, such as fetching the data from flash memory and sending it to

Figure 1–56 shows the transceiver configuration in GIGE mode.

**Figure 1–56. Transceiver Configuration in GIGE Mode**

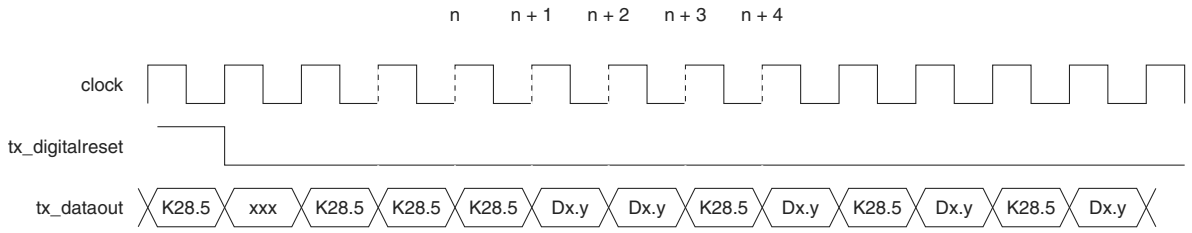



When configured in GIGE mode, three encoded comma (/K28.5/) code groups are transmitted automatically after deassertion of `tx_digitalreset` and before transmitting user data on the `tx_datain` port. This could affect the synchronization state machine behavior at the receiver.

Depending on when you start transmitting the synchronization sequence, there could be an even or odd number of encoded data (/Dx.y/) code groups transmitted between the last of the three automatically sent /K28.5/ code groups and the first /K28.5/ code group of the synchronization sequence. If there is an even number of /Dx.y/ code groups received between these two /K28.5/ code groups, the first /K28.5/ code group of the synchronization sequence begins at an odd code group boundary. An IEEE802.3-compliant GIGE synchronization state machine treats this as an error condition and goes into the Loss-of-Sync state.

Figure 1–57 shows an example of even numbers of /Dx.y/ between the last automatically sent /K28.5/ and the first user-sent /K28.5/. The first user-sent /K28.5/ code group received at an odd code group boundary in cycle $n + 3$ takes the receiver synchronization state machine in Loss-of-Sync state. The first synchronization ordered-set /K28.5/Dx.y/ in cycles $n + 3$ and $n + 4$ is discounted and three additional ordered sets are required for successful synchronization.

**Figure 1–57. Example of Reset Condition in GIGE Mode**




## Running Disparity Preservation with Idle Ordered Set

During idle ordered sets transmission in GIGE mode, the transmitter ensures a negative running disparity at the end of an idle ordered set. Any /Dx.y/, except for /D21.5/ (part of /C1/ ordered set) or /D2.2/ (part of /C2/ ordered set) following a /K28.5/ is automatically replaced with either of the following:

- A /D5.6/ (/I1/ ordered set) if the running disparity before /K28.5/ is positive
- A /D16.2/ (/I2/ ordered set) if the running disparity before /K28.5/ is negative

## Lane Synchronization

In GIGE mode, the word aligner is configured in automatic synchronization state machine mode that complies with the IEEE P802.3ae standard. A synchronization ordered set is a /K28.5/ code group followed by an odd number of valid /Dx.y/ code groups. Table 1–19 lists the synchronization state machine parameters that implements the GbE-compliant synchronization.

**Table 1–19. Synchronization State Machine Parameters (1)**

| Parameter | Value |
|---|---|
| Number of valid synchronization ordered sets received to achieve synchronization | 3 |
| Number of erroneous code groups received to lose synchronization | 4 |
| Number of continuous good code groups received to reduce the error count by one | 4 |

**Note to Table 1–19:**

(1) The word aligner supports 7-bit and 10-bit pattern lengths in GIGE mode.

**Table 1–28. PIPE Interface Ports in ALTGX Megafunction for Cyclone IV GX (1) (Part 1 of 2)**

| Port Name | Input/ Output | Clock Domain | Description |
|---|---|---|---|
| fixedclk | Input | Clock signal | 125-MHz clock for receiver detect and offset cancellation only in PIPE mode. |
| tx_detectrxloop | Input | Asynchronous signal | Receiver detect or reverse parallel loopback control.<br>■ A high level in the P1 power state and `tx_forceelecidle` signal asserted begins the receiver detection operation to determine if there is a valid receiver downstream. This signal must be deasserted when the `pipephydonestatus` signal indicates receiver detect completion.<br>■ A high level in the P0 power state with the `tx_forceelecidle` signal deasserted dynamically configures the channel to support reverse parallel loopback mode. |
| tx_forcedisp compliance | Input | Asynchronous signal | Force the 8B/10B encoder to encode with negative running disparity.<br>■ Assert only when transmitting the first byte of the PIPE-compliance pattern to force the 8B/10B encoder with a negative running disparity. |
| pipe8b10binvpolarity | Input | Asynchronous signal | Invert the polarity of every bit of the 10-bit input to the 8B/10B decoder |
| powerdn | Input | Asynchronous signal | PIPE power state control.<br>■ Signal is 2 bits wide and is encoded as follows:<br>■ 2'b00: P0 (Normal operation)<br>■ 2'b01: P0s (Low recovery time latency, low power state)<br>■ 2'b10: P1 (Longer recovery time latency, lower power state)<br>■ 2'b11: P2 (Lowest power state) |
| pipedatavalid | Output | N/A | Valid data and control on the `rx_dataout` and `rx_ctrldetect` ports indicator. |
| pipephydone status | Output | Asynchronous signal | PHY function completion indicator.<br>■ Asserted for one clock cycle to communicate completion of several PHY functions, such as power state transition and receiver detection. |
| pipeelecidle | Output | Asynchronous signal | Electrical idle detected or inferred at the receiver indicator.<br>■ When electrical idle inference is used, this signal is driven high when it infers an electrical idle condition<br>■ When electrical idle inference is not used, the `rx_signaldetect` signal is inverted and driven on this port. |

**Table 3–2. Dynamic Reconfiguration Controller Port List (ALTGX_RECONFIG Instance) (Part 5 of 7)**

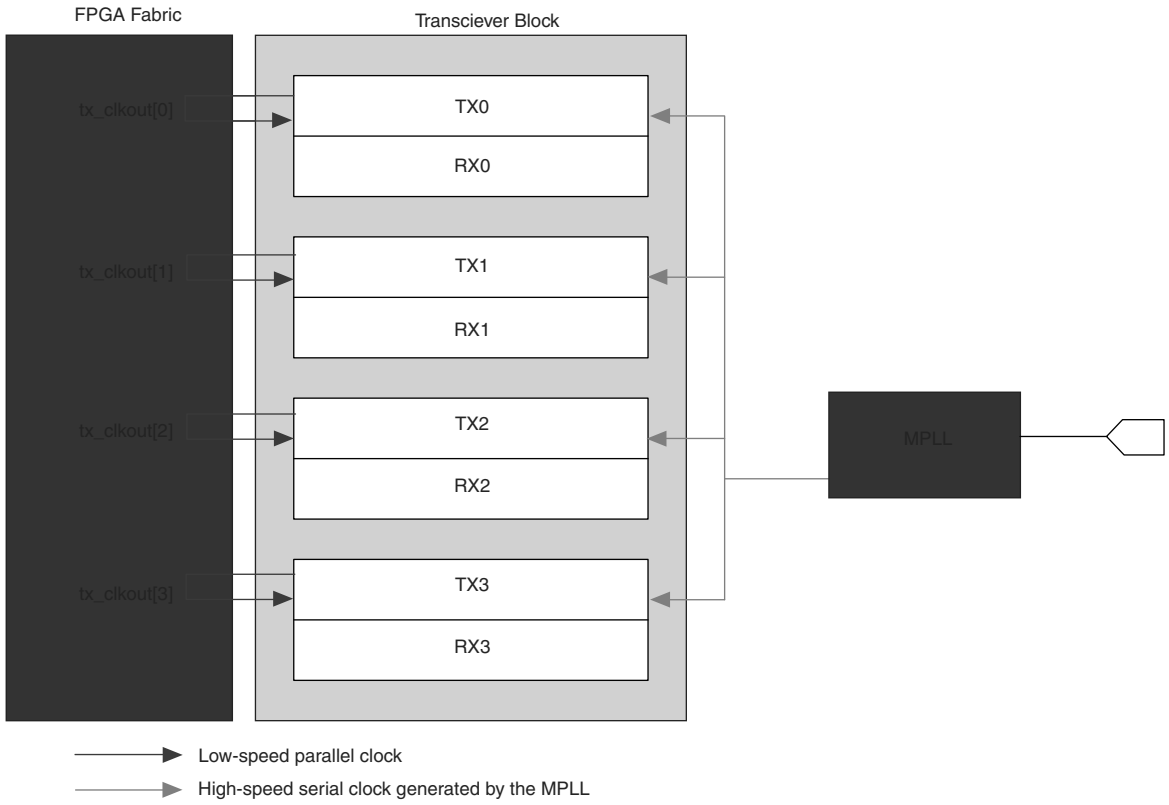
<table>
<tr><th>Port Name</th><th>Input/ Output</th><th>Description</th></tr>
<tr><td>tx_preemp[4..0] (1)</td><td>Input</td><td>This is an optional pre-emphasis write control for the transmit buffer. Depending on what value you set at this input, the controller dynamically writes the value to the pre-emphasis control register of the transmit buffer.<br>The width of this signal is fixed to 5 bits if you enable either the Use 'logical_channel_address' port for Analog controls reconfiguration option or the Use same control signal for all the channels option in the Analog controls screen. Otherwise, the width of this signal is 5 bits per channel.<br>
<table>
<tr><th>tx_preemp[4..0]</th><th>Corresponding ALTGX instance settings</th><th>Corresponding pre-emphasis setting (mA)</th></tr>
<tr><td>00000</td><td>0</td><td>Disabled</td></tr>
<tr><td>00001</td><td>1</td><td>0.5</td></tr>
<tr><td>00101</td><td>5</td><td>1.0</td></tr>
<tr><td>01001</td><td>9</td><td>1.5</td></tr>
<tr><td>01101</td><td>13</td><td>2.0</td></tr>
<tr><td>10000</td><td>16</td><td>2.375</td></tr>
<tr><td>10001</td><td>17</td><td>2.5</td></tr>
<tr><td>10010</td><td>18</td><td>2.625</td></tr>
<tr><td>10011</td><td>19</td><td>2.75</td></tr>
<tr><td>10100</td><td>20</td><td>2.875</td></tr>
<tr><td>10101</td><td>21</td><td>3.0</td></tr>
</table>
All other values => N/A</td></tr>
<tr><td>rx_eqctrl[3..0] (1)</td><td>Input</td><td>This is an optional write control to write an equalization control value for the receive side of the PMA.<br>The width of this signal is fixed to 4 bits if you enable either the Use 'logical_channel_address' port for Analog controls reconfiguration option or the Use same control signal for all the channels option in the Analog controls screen. Otherwise, the width of this signal is 4 bits per channel.<br>
<table>
<tr><th>rx_eqctrl[3..0]</th><th>Corresponding ALTGX instance settings</th></tr>
<tr><td>0001</td><td>Low</td></tr>
<tr><td>0101</td><td>Medium Low</td></tr>
<tr><td>0100</td><td>Medium High</td></tr>
<tr><td>0111</td><td>High</td></tr>
</table>
All other values => N/A</td></tr>
</table>

### Option 2: Use the Respective Channel Transmitter Core Clocks

- Enable this option if you want the individual transmitter channel `tx_clkout` signals to provide the write clock to their respective Transmit Phase Compensation FIFOs.
- This option is typically enabled when each transceiver channel is reconfigured to a different functional mode using channel reconfiguration.

Figure 3–12 shows how each transmitter channel's `tx_clkout` signal provides a clock to the Transmit Phase Compensation FIFOs of the respective transceiver channels.

**Figure 3–12. Option 2 for Transmitter Core Clocking (Channel Reconfiguration Mode)**




Receiver core clocking refers to the clock that is used to read the parallel data from the Receiver Phase Compensation FIFO into the FPGA fabric. You can use one of the following clocks to read from the Receive Phase Compensation FIFO:

- `rx_coreclk`—you can use a clock of the same frequency as `rx_clkout` from the FPGA fabric to provide the read clock to the Receive Phase Compensation FIFO. If you use `rx_coreclk`, it overrides the `rx_clkout` options in the ALTGX MegaWizard Plug-In Manager.
- `rx_clkout`—the Quartus II software automatically routes `rx_clkout` to the FPGA fabric and back into the Receive Phase Compensation FIFO.

# DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

## Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1–6 lists the I/O pin leakage current for Cyclone IV devices.

**Table 1–6. I/O Pin Leakage Current for Cyclone IV Devices** *(1), (2)*

| Symbol | Parameter | Conditions | Device | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I$ = 0 V to $V_{CCIOMAX}$ | — | –10 | — | 10 | µA |
| $I_{OZ}$ | Tristated I/O pin leakage current | $V_O$ = 0 V to $V_{CCIOMAX}$ | — | –10 | — | 10 | µA |

**Notes to Table 1–6:**

(1) This value is specified for normal device operation. The value varies during device power-up. This applies for all $V_{CCIO}$ settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

## Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–7 lists bus hold specifications for Cyclone IV devices.

**Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2)** *(1)*

| Parameter | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus hold low, sustaining current | $V_{IN} > V_{IL}$ (maximum) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus hold high, sustaining current | $V_{IN} < V_{IL}$ (minimum) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |
| Bus hold low, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus hold high, overdrive current | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up. Use Table 1–10 and Equation 1–1 to determine the final OCT resistance considering the variations after calibration at device power-up. Table 1–10 lists the change percentage of the OCT resistance with voltage and temperature.

**Table 1–10. OCT Variation After Calibration at Device Power-Up for Cyclone IV Devices** *(1)*

| Nominal Voltage | dR/dT (%/°C) | dR/dV (%/mV) |
|---|---|---|
| 3.0 | 0.262 | –0.026 |
| 2.5 | 0.234 | –0.039 |
| 1.8 | 0.219 | –0.086 |
| 1.5 | 0.199 | –0.136 |
| 1.2 | 0.161 | –0.288 |

**Note to Table 1–10:**

(1) This specification is not applicable to EP4CGX15, EP4CGX22, and EP4CGX30 devices.

**Equation 1–1. Final OCT Resistance** *(1), (2), (3), (4), (5), (6)*

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV \quad (7)$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT \quad (8)$$

$$\text{For } \Delta R_x < 0;\ MF_x = 1/ (|\Delta R_x|/100 + 1) \quad (9)$$

$$\text{For } \Delta R_x > 0;\ MF_x = \Delta R_x/100 + 1 \quad (10)$$

$$MF = MF_V \times MF_T \quad (11)$$

$$R_{final} = R_{initial} \times MF \quad (12)$$

**Notes to Equation 1–1:**

(1) $T_2$ is the final temperature.
(2) $T_1$ is the initial temperature.
(3) MF is multiplication factor.
(4) $R_{final}$ is final resistance.
(5) $R_{initial}$ is initial resistance.
(6) Subscript $_x$ refers to both $_V$ and $_T$.
(7) $\Delta R_V$ is a variation of resistance with voltage.
(8) $\Delta R_T$ is a variation of resistance with temperature.
(9) dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
(10) dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
(11) $V_2$ is final voltage.
(12) $V_1$ is the initial voltage.

**Table 1–25. PLL Specifications for Cyclone IV Devices (1), (2) (Part 2 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted) | — | — | 1 | ms |
| $t_{OUTJITTER\_PERIOD\_DEDCLK}$ (6) | Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER\_CCJ\_DEDCLK}$ (6) | Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 300 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 30 | mUI |
| $t_{OUTJITTER\_PERIOD\_IO}$ (6) | Regular I/O period jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{OUTJITTER\_CCJ\_IO}$ (6) | Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz | — | — | 650 | ps |
| | $F_{OUT} < 100$ MHz | — | — | 75 | mUI |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on areset signal. | 10 | — | — | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chains for PLLs | — | 3.5 (7) | — | SCANCLK cycles |
| $f_{SCANCLK}$ | scanclk frequency | — | — | 100 | MHz |
| $t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ (8), (9) | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz) | — | — | 425 | ps |
| | Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz) | — | — | 42.5 | mUI |

**Notes to Table 1–25:**

(1) This table is applicable for general purpose PLLs and multipurpose PLLs.

(2) You must connect $V_{CCD\_PLL}$ to $V_{CCINT}$ through the decoupling capacitor and ferrite bead.

(3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(4) The $V_{CO}$ frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the $V_{CO}$ post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.

(6) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.

(7) With 100-MHz scanclk frequency.

(8) The cascaded PLLs specification is applicable only with the following conditions:

- Upstream PLL—0.59 MHz ≤ Upstream PLL bandwidth < 1 MHz
- Downstream PLL—Downstream PLL bandwidth > 2 MHz

(9) PLL cascading is not supported for transceiver applications.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interface Handbook*.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

**Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices** *(1), (2)*

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Clock period jitter | $t_{JIT(per)}$ | –125 | 125 | ps |
| Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –200 | 200 | ps |
| Duty cycle jitter | $t_{JIT(duty)}$ | –150 | 150 | ps |

**Notes to Table 1–37:**

(1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

## Duty Cycle Distortion Specifications

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

**Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins** *(1), (2), (3)*

| Symbol | C6 | | C7, I7 | | C8, I8L, A7 | | C9L | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |

**Notes to Table 1–38:**

(1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.

(2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

## OCT Calibration Timing Specification

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

**Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices** *(1)*

| Symbol | Description | Maximum | Units |
|---|---|---|---|
| $t_{OCTCAL}$ | Duration of series OCT with calibration at device power-up | 20 | µs |

**Note to Table 1–39:**

(1) OCT calibration takes place after device configuration and before entering user mode.