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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2475
Number of Logic Elements/Cells	39600
Total RAM Bits	1161216
Number of I/O	532
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce40f29c6n

I/O Features

Cyclone IV device I/O supports programmable bus hold, programmable pull-up resistors, programmable delay, programmable drive strength, programmable slew-rate control to optimize signal integrity, and hot socketing. Cyclone IV devices support calibrated on-chip series termination (Rs OCT) or driver impedance matching (Rs) for single-ended I/O standards. In Cyclone IV GX devices, the high-speed transceiver I/Os are located on the left side of the device. The top, bottom, and right sides can implement general-purpose user I/Os.

Table 1-8 lists the I/O standards that Cyclone IV devices support.

Table 1-8. I/O Standards Support for the Cyclone IV Device Family

Type	I/O Standard
Single-Ended I/O	LVTTL, LVCMOS, SSTL, HSTL, PCI, and PCI-X
Differential I/O	SSTL, HSTL, LVPECL, BLVDS, LVDS, mini-LVDS, RSDS, and PPDS

The LVDS SERDES is implemented in the core of the device using logic elements.



For more information, refer to the *I/O Features in Cyclone IV Devices* chapter.

Clock Management

Cyclone IV devices include up to 30 global clock (GCLK) networks and up to eight PLLs with five outputs per PLL to provide robust clock management and synthesis. You can dynamically reconfigure Cyclone IV device PLLs in user mode to change the clock frequency or phase.

Cyclone IV GX devices support two types of PLLs: multipurpose PLLs and general-purpose PLLs:

- Use multipurpose PLLs for clocking the transceiver blocks. You can also use them for general-purpose clocking when they are not used for transceiver clocking.
- Use general purpose PLLs for general-purpose applications in the fabric and periphery, such as external memory interfaces. Some of the general purpose PLLs can support transceiver clocking.



For more information, refer to the *Clock Networks and PLLs in Cyclone IV Devices* chapter.

External Memory Interfaces

Cyclone IV devices support SDR, DDR, DDR2 SDRAM, and QDR II SRAM interfaces on the top, bottom, and right sides of the device. Cyclone IV E devices also support these interfaces on the left side of the device. Interfaces may span two or more sides of the device to allow more flexible board design. The Altera® DDR SDRAM memory interface solution consists of a PHY interface and a memory controller. Altera supplies the PHY IP and you can use it in conjunction with your own custom memory controller or an Altera-provided memory controller. Cyclone IV devices support the use of error correction coding (ECC) bits on DDR and DDR2 SDRAM interfaces.

Document Revision History

Table 1–10 lists the revision history for this chapter.

Table 1–10. Document Revision History

Date	Version	Changes
March 2016	2.0	■ Updated Table 1–4 and Table 1–5 to remove support for the N148 package. ■ Updated Figure 1–2 to remove support for the N148 package.
April 2014	1.9	Updated “Packaging Ordering Information for the Cyclone IV E Device”.
May 2013	1.8	Updated Table 1–3, Table 1–6 and Figure 1–3 to add new device options and packages.
February 2013	1.7	Updated Table 1–3, Table 1–6 and Figure 1–3 to add new device options and packages.
October 2012	1.6	Updated Table 1–3 and Table 1–4.
November 2011	1.5	■ Updated “Cyclone IV Device Family Features” section. ■ Updated Figure 1–2 and Figure 1–3.
December 2010	1.4	■ Updated for the Quartus II software version 10.1 release. ■ Added Cyclone IV E new device package information. ■ Updated Table 1–1, Table 1–2, Table 1–3, Table 1–5, and Table 1–6. ■ Updated Figure 1–3. ■ Minor text edits.
July 2010	1.3	Updated Table 1–2 to include F484 package information.
March 2010	1.2	■ Updated Table 1–3 and Table 1–6. ■ Updated Figure 1–3. ■ Minor text edits.
February 2010	1.1	■ Added Cyclone IV E devices in Table 1–1, Table 1–3, and Table 1–6 for the Quartus II software version 9.1 SP1 release. ■ Added the “Cyclone IV Device Family Speed Grades” and “Configuration” sections. ■ Added Figure 1–3 to include Cyclone IV E Device Packaging Ordering Information. ■ Updated Table 1–2, Table 1–4, and Table 1–5 for Cyclone IV GX devices. ■ Minor text edits.
November 2009	1.0	Initial release.

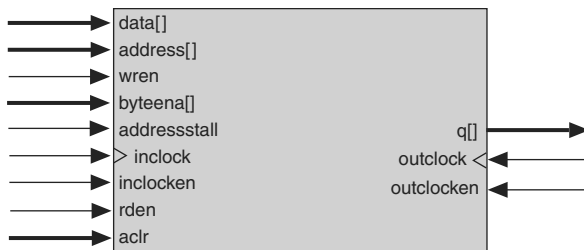


Violating the setup or hold time on the M9K memory block input registers may corrupt memory contents. This applies to both read and write operations.

Single-Port Mode

Single-port mode supports non-simultaneous read and write operations from a single address. Figure 3-6 shows the single-port memory configuration for Cyclone IV devices M9K memory blocks.

Figure 3-6. Single-Port Memory ⁽¹⁾, ⁽²⁾



Notes to Figure 3-6:

(1) You can implement two single-port memory blocks in a single M9K block.

(2) For more information, refer to “Packed Mode Support” on page 3-4.

During a write operation, the behavior of the RAM outputs is configurable. If you activate `rden` during a write operation, the RAM outputs show either the new data being written or the old data at that address. If you perform a write operation with `rden` deactivated, the RAM outputs retain the values they held during the most recent active `rden` signal.

To choose the desired behavior, set the **Read-During-Write** option to either **New Data** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about read-during-write mode, refer to “Read-During-Write Operations” on page 3-15.

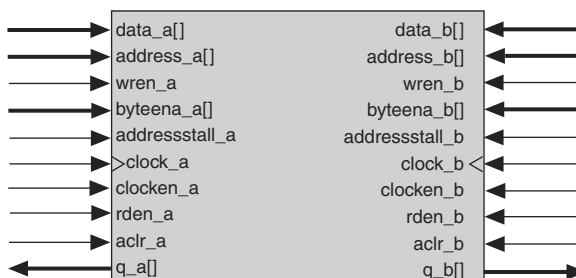
The port width configurations for M9K blocks in single-port mode are as follow:

- 8192 × 1
- 4096 × 2
- 2048 × 4
- 1024 × 8
- 1024 × 9
- 512 × 16
- 512 × 18
- 256 × 32
- 256 × 36

True Dual-Port Mode

True dual-port mode supports any combination of two-port operations: two reads, two writes, or one read and one write, at two different clock frequencies. Figure 3–10 shows Cyclone IV devices true dual-port memory configuration.

Figure 3–10. Cyclone IV Devices True Dual-Port Memory ⁽¹⁾



Note to Figure 3–10:

(1) True dual-port memory supports input or output clock mode in addition to the independent clock mode shown.

 The widest bit configuration of the M9K blocks in true dual-port mode is 512 × 16-bit (18-bit with parity).

Table 3–4 lists the possible M9K block mixed-port width configurations.

Table 3–4. Cyclone IV Devices M9K Block Mixed-Width Configurations (True Dual-Port Mode)

Read Port	Write Port						
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	1024 × 9	512 × 18
8192 × 1	✓	✓	✓	✓	✓	—	—
4096 × 2	✓	✓	✓	✓	✓	—	—
2048 × 4	✓	✓	✓	✓	✓	—	—
1024 × 8	✓	✓	✓	✓	✓	—	—
512 × 16	✓	✓	✓	✓	✓	—	—
1024 × 9	—	—	—	—	—	✓	✓
512 × 18	—	—	—	—	—	✓	✓

In true dual-port mode, M9K memory blocks support separate wren and rden signals. You can save power by keeping the rden signal low (inactive) when not reading. Read-during-write operations to the same address can either output “New Data” at that location or “Old Data”. To choose the desired behavior, set the **Read-During-Write** option to either **New Data** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about this behavior, refer to “Read-During-Write Operations” on page 3–15.

Table 5–10. Loop Filter Control of High Frequency Capacitor

LFC[1]	LFC[0]	Setting (Decimal)
0	0	0
0	1	1
1	1	3

Bypassing a PLL Counter

Bypassing a PLL counter results in a divide (N, C0 to C4 counters) factor of one.

Table 5–11 lists the settings for bypassing the counters in PLLs of Cyclone IV devices.

Table 5–11. PLL Counter Settings

PLL Scan Chain Bits [0..8] Settings								Description
LSB							MSB	
X	X	X	X	X	X	X	1 ⁽¹⁾	PLL counter bypassed
X	X	X	X	X	X	X	0 ⁽¹⁾	PLL counter not bypassed

Note to Table 5–11:

(1) Bypass bit.

To bypass any of the PLL counters, set the bypass bit to 1. The values on the other bits are then ignored.

Dynamic Phase Shifting

The dynamic phase shifting feature allows the output phase of individual PLL outputs to be dynamically adjusted relative to each other and the reference clock without sending serial data through the scan chain of the corresponding PLL. This feature simplifies the interface and allows you to quickly adjust t_{CO} delays by changing output clock phase shift in real time. This is achieved by incrementing or decrementing the VCO phase-tap selection to a given C counter or to the M counter. The phase is shifted by 1/8 the VCO frequency at a time. The output clocks are active during this phase reconfiguration process.

Table 5–12 lists the control signals that are used for dynamic phase shifting.

Table 5–12. Dynamic Phase Shifting Control Signals (Part 1 of 2)

Signal Name	Description	Source	Destination
phasecounterselect[2..0]	Counter Select. Three bits decoded to select either the M or one of the C counters for phase adjustment. One address map to select all C counters. This signal is registered in the PLL on the rising edge of <code>scanclk</code> .	Logic array or I/O pins	PLL reconfiguration circuit
phaseupdown	Selects dynamic phase shift direction; 1 = UP, 0 = DOWN. Signal is registered in the PLL on the rising edge of <code>scanclk</code> .	Logic array or I/O pins	PLL reconfiguration circuit
phasestep	Logic high enables dynamic phase shifting.	Logic array or I/O pins	PLL reconfiguration circuit

6. I/O Features in Cyclone IV Devices

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This chapter describes the I/O and high speed I/O capabilities and features offered in Cyclone® IV devices.

The I/O capabilities of Cyclone IV devices are driven by the diversification of I/O standards in many low-cost applications, and the significant increase in required I/O performance. Altera's objective is to create a device that accommodates your key board design needs with ease and flexibility.

The I/O flexibility of Cyclone IV devices is increased from the previous generation low-cost FPGAs by allowing all I/O standards to be selected on all I/O banks. Improvements to on-chip termination (OCT) support and the addition of true differential buffers have eliminated the need for external resistors in many applications, such as display system interfaces.

High-speed differential I/O standards have become popular in high-speed interfaces because of their significant advantages over single-ended I/O standards. The Cyclone IV devices support LVDS, BLVDS, RSDS, mini-LVDS, and PPDS. The transceiver reference clocks and the existing general-purpose I/O (GPIO) clock input features also support the LVDS I/O standards.

The Quartus® II software completes the solution with powerful pin planning features that allow you to plan and optimize I/O system designs even before the design files are available.

This chapter includes the following sections:

- “Cyclone IV I/O Elements” on page 6–2
- “I/O Element Features” on page 6–3
- “OCT Support” on page 6–6
- “I/O Standards” on page 6–11
- “Termination Scheme for I/O Standards” on page 6–13
- “I/O Banks” on page 6–16

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Designing with LVDS

Cyclone IV I/O banks support the LVDS I/O standard. The Cyclone IV GX right I/O banks support true LVDS transmitters while the Cyclone IV E left and right I/O banks support true LVDS transmitters. On the top and bottom I/O banks, the emulated LVDS transmitters are supported using two single-ended output buffers with external resistors. One of the single-ended output buffers is programmed to have opposite polarity. The LVDS receiver requires an external 100- Ω termination resistor between the two signals at the input buffer.

Figure 6-12 shows a point-to-point LVDS interface using Cyclone IV devices true LVDS output and input buffers.

Figure 6-12. Cyclone IV Devices LVDS Interface with True Output Buffer on the Right I/O Banks

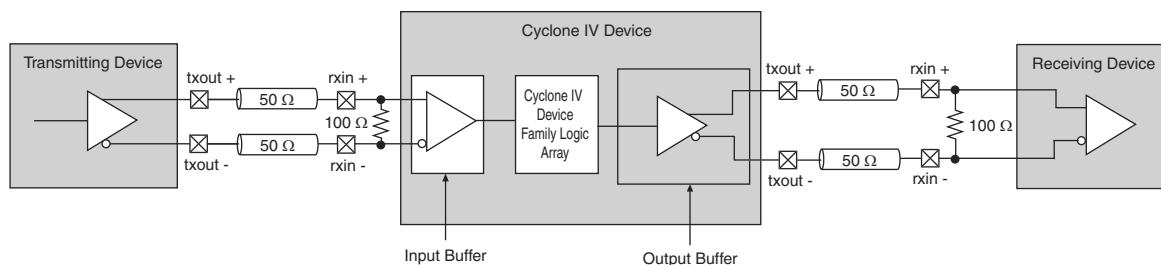
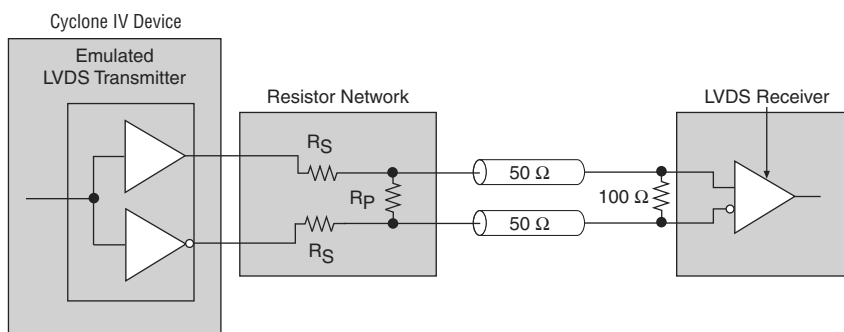


Figure 6-13 shows a point-to-point LVDS interface with Cyclone IV devices LVDS using two single-ended output buffers and external resistors.

Figure 6-13. LVDS Interface with External Resistor Network on the Top and Bottom I/O Banks ⁽¹⁾



Note to Figure 6-13:

(1) $R_S = 120\ \Omega$. $R_P = 170\ \Omega$.

BLVDS I/O Standard Support in Cyclone IV Devices

The BLVDS I/O standard is a high-speed differential data transmission technology that extends the benefits of standard point-to-point LVDS to multipoint configuration that supports bidirectional half-duplex communication. BLVDS differs from standard LVDS by providing a higher drive to achieve similar signal swings at the receiver while loaded with two terminations at both ends of the bus.

Table 7–1 lists the number of DQS or DQ groups supported on each side of the Cyclone IV GX device.

Table 7–1. Cyclone IV GX Device DQS and DQ Bus Mode Support for Each Side of the Device

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP4CGX15	169-pin FBGA	Right	1	0	0	0	—	—
		Top ⁽¹⁾	1	0	0	0	—	—
		Bottom ⁽²⁾	1	0	0	0	—	—
EP4CGX22 EP4CGX30	169-pin FBGA	Right	1	0	0	0	—	—
		Top ⁽¹⁾	1	0	0	0	—	—
		Bottom ⁽²⁾	1	0	0	0	—	—
	324-pin FBGA	Right	2	2	1	1	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	484-pin FBGA ⁽³⁾	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
EP4CGX50 EP4CGX75	484-pin FBGA	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	672-pin FBGA	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
EP4CGX110 EP4CGX150	484-pin FBGA	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	672-pin FBGA	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	896-pin FBGA	Right	6	3	2	2	1	1
		Top	6	3	3	3	1	1
		Bottom	6	3	3	3	1	1

Notes to Table 7–1:

- (1) Some of the DQ pins can be used as RUP and RDN pins. You cannot use these groups if you are using these pins as RUP and RDN pins for OCT calibration.
- (2) Some of the DQ pins can be used as RUP pins while the DM pins can be used as RDN pins. You cannot use these groups if you are using the RUP and RDN pins for OCT calibration.
- (3) Only available for EP4CGX30 device.

four devices. During the first configuration cycle, the master device reads its configuration data from the serial configuration device while holding `nCEO` high. After completing its configuration cycle, the master device drives `nCE` low and sends the second copy of the configuration data to all three slave devices, configuring them simultaneously.

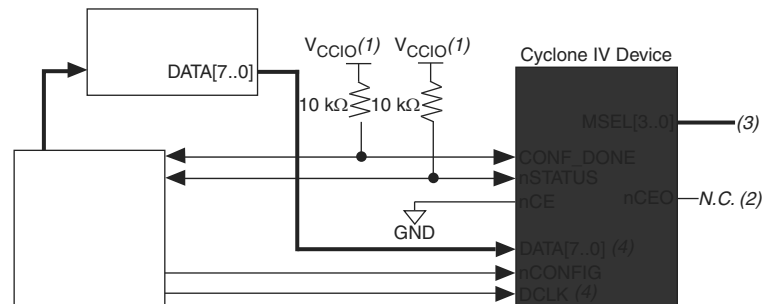
The advantage of the setup in Figure 8-4 is that you can have a different `.sof` for the master device. However, all the slave devices must be configured with the same `.sof`. You can either compress or uncompress the `.sof` in this configuration method.



You can still use this method if the master and slave devices use the same `.sof`.

the device, must be stored in the external host device. Figure 8-19 shows the configuration interface connections between the Cyclone IV devices and an external device for single-device configuration.

Figure 8-19. Single-Device FPP Configuration Using an External Host



Notes to Figure 8-19:

- (1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.
- (2) The nCE pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (3) The $MSEL$ pin settings vary for different configuration voltage standards and POR time. To connect the $MSEL$ pins, refer to Table 8-4 on page 8-8 and Table 8-5 on page 8-9. Connect the $MSEL$ pins directly to V_{CCA} or GND.
- (4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. $DATA[7..0]$ and $DCLK$ must fit the maximum overshoot outlined in Equation 8-1 on page 8-5.

After $nSTATUS$ is released, the device is ready to receive configuration data and the configuration stage begins. When $nSTATUS$ is pulled high, the external host device places the configuration data one byte at a time on the $DATA[7..0]$ pins.

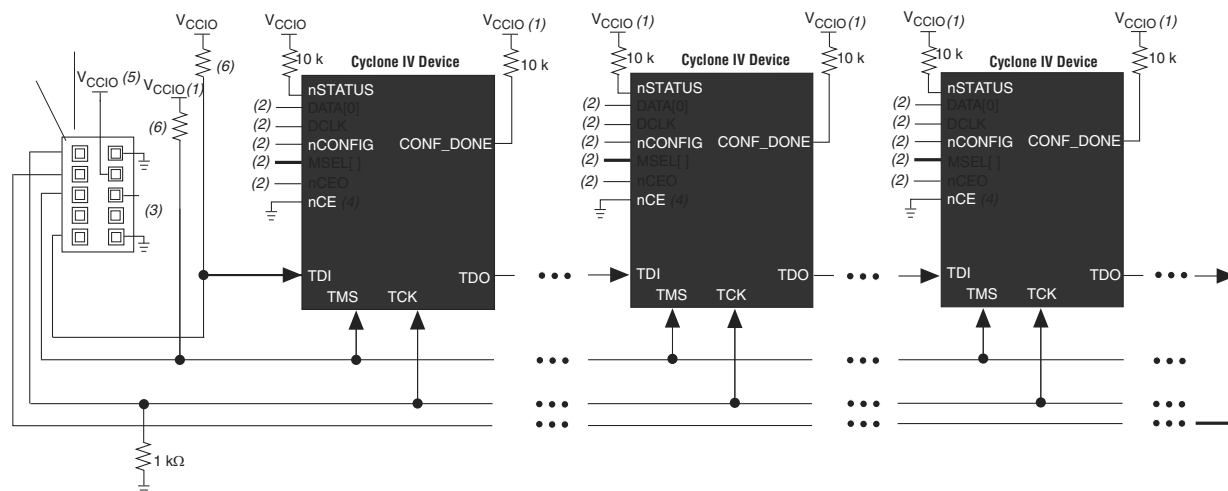
Cyclone IV devices receive configuration data on the $DATA[7..0]$ pins and the clock is received on the $DCLK$ pin. Data is latched into the device on the rising edge of $DCLK$. Data is continuously clocked into the target device until $CONF_DONE$ goes high. The $CONF_DONE$ pin goes high one byte early in FPP configuration mode. The last byte is required for serial configuration (AS and PS) modes.

 Two $DCLK$ falling edges are required after $CONF_DONE$ goes high to begin initialization of the device.

Supplying a clock on $CLKUSR$ does not affect the configuration process. After the $CONF_DONE$ pin goes high, $CLKUSR$ is enabled after the time specified as t_{CD2CU} . After this time period elapses, Cyclone IV devices require 3,192 clock cycles to initialize properly and enter user mode. For more information about the supported $CLKUSR f_{MAX}$ value for Cyclone IV devices, refer to Table 8-13 on page 8-44.

The $INIT_DONE$ pin is released and pulled high when initialization is complete. The external host device must be able to detect this low-to-high transition, which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

Figure 8-26. JTAG Configuration of Multiple Devices Using a Download Cable (1.2, 1.5, and 1.8-V V_{CCIO} Powering the JTAG Pins)



Notes to Figure 8-26:

- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Connect the $nCONFIG$ and $MSEL$ pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the $nCONFIG$ pin to logic-high and the $MSEL$ pins to GND. In addition, pull $DCLK$ and $DATA[0]$ to either high or low, whichever is convenient on your board.
- (3) In the USB-Blaster and ByteBlaster II cable, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) You must connect the nCE pin to GND or driven low for successful JTAG configuration.
- (5) Power up the V_{CC} of the ByteBlaster II or USB-Blaster cable with supply from V_{CCIO} . The ByteBlaster II and USB-Blaster cables do not support a target supply voltage of 1.2 V. For the target supply voltage value, refer to the *ByteBlaster II Download Cable User Guide* and the *USB-Blaster Download Cable User Guide*.
- (6) Resistor value can vary from 1 k Ω to 10 k Ω .



If a non-Cyclone IV device is cascaded in the JTAG-chain, TDO of the non-Cyclone IV device driving into TDI of the Cyclone IV device must fit the maximum overshoot outlined in Equation 8-1 on page 8-5.

The $CONF_DONE$ and $nSTATUS$ signals are shared in multi-device AS, AP, PS, and FPP configuration chains to ensure that the devices enter user mode at the same time after configuration is complete. When the $CONF_DONE$ and $nSTATUS$ signals are shared among all the devices, you must configure every device when JTAG configuration is performed.

If you only use JTAG configuration, Altera recommends that you connect the circuitry as shown in Figure 8-25 or Figure 8-26, in which each of the $CONF_DONE$ and $nSTATUS$ signals are isolated so that each device can enter user mode individually.

After the first device completes configuration in a multi-device configuration chain, its $nCEO$ pin drives low to activate the nCE pin of the second device, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, ensure that the nCE pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multi-device configuration chain, the $nCEO$ of the previous device drives the nCE pin of the next device low when it has successfully been JTAG configured. You can place other Altera devices that have JTAG support in the same JTAG chain for device programming and configuration.

Table 9–4 defines the registers shown in Figure 9–1.

Table 9–4. Error Detection Registers

Register	Function
32-bit signature register	This register contains the CRC signature. The signature register contains the result of the user mode calculated CRC value compared against the pre-calculated CRC value. If no errors are detected, the signature register is all zeros. A non-zero signature register indicates an error in the configuration CRAM contents. The CRC_ERROR signal is derived from the contents of this register.
32-bit storage register	This register is loaded with the 32-bit pre-computed CRC signature at the end of the configuration stage. The signature is then loaded into the 32-bit CRC circuit (called the Compute and Compare CRC block, as shown in Figure 9–1) during user mode to calculate the CRC error. This register forms a 32-bit scan chain during execution of the CHANGE_EDREG JTAG instruction. The CHANGE_EDREG JTAG instruction can change the content of the storage register. Therefore, the functionality of the error detection CRC circuitry is checked in-system by executing the instruction to inject an error during the operation. The operation of the device is not halted when issuing the CHANGE_EDREG instruction.

Error Detection Timing

When the error detection CRC feature is enabled through the Quartus II software, the device automatically activates the CRC process upon entering user mode after configuration and initialization is complete.

The CRC_ERROR pin is driven low until the error detection circuitry detects a corrupted bit in the previous CRC calculation. After the pin goes high, it remains high during the next CRC calculation. This pin does not log the previous CRC calculation. If the new CRC calculation does not contain any corrupted bits, the CRC_ERROR pin is driven low. The error detection runs until the device is reset.

The error detection circuitry runs off an internal configuration oscillator with a divisor that sets the maximum frequency.

Table 9–5 lists the minimum and maximum error detection frequencies.

Table 9–5. Minimum and Maximum Error Detection Frequencies for Cyclone IV Devices

Error Detection Frequency	Maximum Error Detection Frequency	Minimum Error Detection Frequency	Valid Divisors (2 ⁿ)
80 MHz/2 ⁿ	80 MHz	312.5 kHz	0, 1, 2, 3, 4, 5, 6, 7, 8

You can set a lower clock frequency by specifying a division factor in the Quartus II software (for more information, refer to “Software Support”). The divisor is a power of two (2), where *n* is between 0 and 8. The divisor ranges from one through 256. Refer to Equation 9–1.

Equation 9–1.

$$\text{Error detection frequency} = \frac{80 \text{ MHz}}{2^n}$$

CRC calculation time depends on the device and the error detection clock frequency.

Transmitter Channel Datapath

The following sections describe the Cyclone IV GX transmitter channel datapath architecture as shown in Figure 1–3:

- TX Phase Compensation FIFO
- Byte Serializer
- 8B/10B Encoder
- Serializer
- Transmitter Output Buffer

TX Phase Compensation FIFO

The TX phase compensation FIFO compensates for the phase difference between the low-speed parallel clock and the FPGA fabric interface clock, when interfacing the transmitter channel to the FPGA fabric (directly or through the PIPE and PCIe hard IP). The FIFO is four words deep, with latency between two to three parallel clock cycles. Figure 1–4 shows the TX phase compensation FIFO block diagram.

Figure 1–4. TX Phase Compensation FIFO Block Diagram



Note to Figure 1–4:

(1) The x refers to the supported 8-, 10-, 16-, or 20-bits transceiver channel width.

 The FIFO can operate in registered mode, contributing to only one parallel clock cycle of latency in Deterministic Latency functional mode. For more information, refer to “Deterministic Latency Mode” on page 1–73.

 For more information about FIFO clocking, refer to “FPGA Fabric-Transceiver Interface Clocking” on page 1–43.

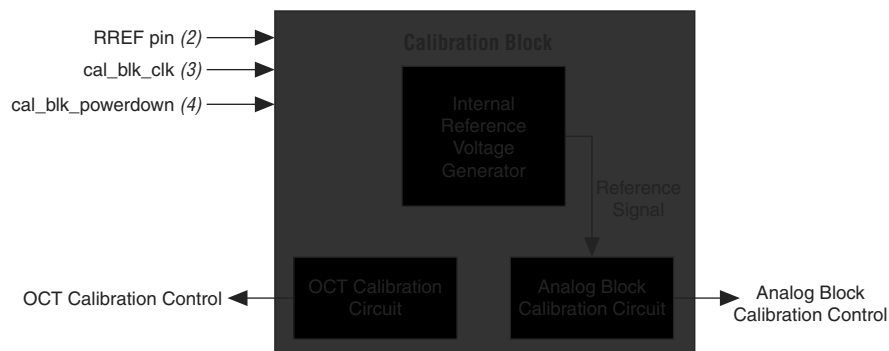
Byte Serializer

The byte serializer divides the input datapath width by two to allow transmitter channel operation at higher data rates while meeting the maximum FPGA fabric frequency limit. This module is required in configurations that exceed the maximum FPGA fabric-transceiver interface clock frequency limit and optional in configurations that do not.

 For the FPGA fabric-transceiver interface frequency specifications, refer to the *Cyclone IV Device Data Sheet*.

The calibration block internally generates a constant internal reference voltage, independent of PVT variations and uses this voltage and the external reference resistor on the RREF pin to generate constant reference currents. The OCT calibration circuit calibrates the OCT resistors present in the transceiver channels. Figure 1-41 shows the calibration block diagram.

Figure 1-41. Input Signals to the Calibration Blocks ⁽¹⁾



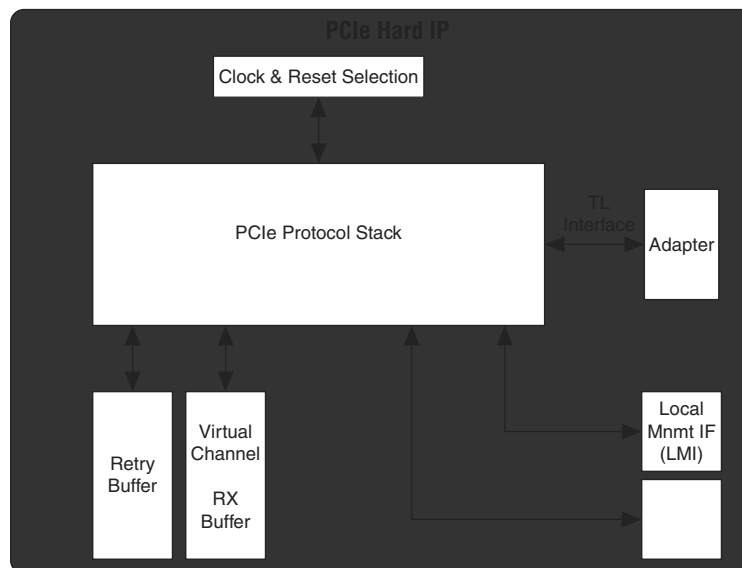
Notes to Figure 1-41:

- (1) All transceiver channels use the same calibration block clock and power down signals.
- (2) Connect a 2 k Ω (tolerance max $\pm$ 1%) external resistor to the RREF pin to ground. The RREF resistor connection in the board must be free from any external noise.
- (3) Supports up to 125 MHz clock frequency. Use either dedicated global clock or divide-down logic from the FPGA fabric to generate a slow clock on the local clock routing.
- (4) The calibration block restarts the calibration process following deassertion of the cal_blk_powerdown signal.

PCI-Express Hard IP Block

Figure 1-42 shows the block diagram of the PCIe hard IP block implementing the PHY MAC, Data Link Layer, and Transaction Layer for PCIe interfaces. The PIPE interface is used as the interface between the transceiver and the hard IP block.

Figure 1-42. PCI Express Hard IP High-Level Block Diagram



Fast Recovery from P0s State

The PCIe protocol defines fast training sequences for bit and byte synchronization to transition from L0s to L0 (PIPE P0s to P0) power states. The PHY must acquire bit and byte synchronization when transitioning from L0s to L0 state between 16 ns to 4 μ s. Each Cyclone IV GX receiver channel has built-in fast recovery circuit that allows the receiver to meet the requirement when enabled.

Electrical Idle Inference

In PIPE mode, the Cyclone IV GX transceiver supports inferring the electrical idle condition at each receiver instead of detecting the electrical idle condition using analog circuitry, as defined in the version 2.0 of PCIe Base Specification. The inference is supported using `rx_elecidleinferred[2..0]` port, with valid driven values as listed in Table 1-17 in each link training and status state machine substate.

Table 1-17. Electrical Idle Inference Conditions

rx_elecidleinferred [2..0]	Link Training and Status State Machine State	Description
3'b100	L0	Absence of <code>update_FC</code> or alternatively skip ordered set in 128 μ s window
3'b101	Recovery.RcvrCfg	Absence of TS1 or TS2 ordered set in 1280 UI interval
3'b101	Recovery.Speed when successful speed negotiation = 1'b1	Absence of TS1 or TS2 ordered set in 1280 UI interval
3'b110	Recovery.Speed when successful speed negotiation = 1'b0	Absence of an exit from electrical idle in 2000 UI interval
3'b111	Loopback.Active (as slave)	Absence of an exit from electrical idle in 128 μ s window

The electrical idle inference module drives the `pipelecidle` signal high in each receiver channel when an electrical idle condition is inferred. The electrical idle inference module cannot detect electrical idle exit condition based on the reception of the electrical idle exit ordered set, as specified in the PCI Express (PIPE) Base Specification.



When enabled, the electrical idle inference block uses electrical idle ordered set detection from the fast recovery circuitry to drive the `pipelecidle` signal.

Compliance Pattern Transmission

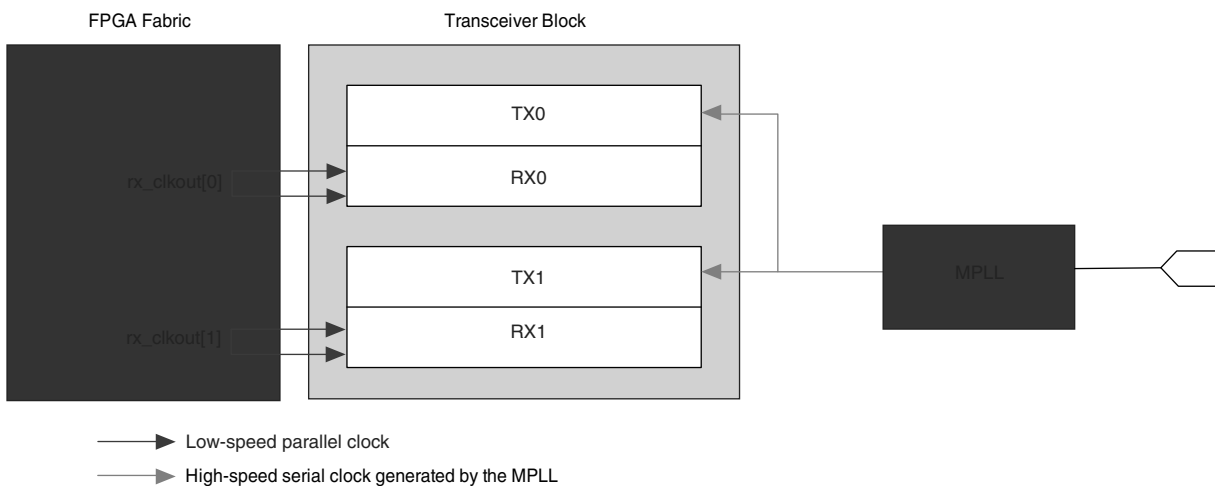
In PIPE mode, the Cyclone IV GX transceiver supports compliance pattern transmission which requires the first /K28.5/ code group of the compliance pattern to be encoded with negative current disparity. This requirement is supported using a `tx_forcedispc` port that when driven with logic high, the transmitter data on the `tx_datain` port is transmitted with negative current running disparity.

Option 3: Use the Respective Channel Receiver Core Clocks

- Enable this option if you want the individual channel's rx_clkout signal to provide the read clock to its respective Receive Phase Compensation FIFO.
- This option is typically enabled when the channel is reconfigured from a Basic or Protocol configuration with or without rate matching to another Basic or Protocol configuration with or without rate matching.

Figure 3-15 shows the respective rx_clkout of each channel clocking the respective receiver channels of a transceiver block.

Figure 3-15. Option 3 for Receiver Core Clocking (Channel Reconfiguration Mode)



PLL Reconfiguration Mode

Cyclone IV GX device support the PLL reconfiguration support through the ALTPLL_RECONFIG MegaWizard. You can use this mode to reconfigure the multipurpose PLL or general purpose PLL used to clock the transceiver channel without affecting the remaining blocks of the channel. When you reconfigure the multipurpose PLL or general purpose PLL of a transceiver block to run at a different data rate, all the transceiver channels listening to this multipurpose PLL or general purpose PLL also get reconfigured to the new data rate. Channel settings are not affected. When you reconfigure the multipurpose PLL or general purpose PLL to support a different data rate, you must ensure that the functional mode of the transceiver channel supports the reconfigured data rate.

The PLL reconfiguration mode can be enabled by selecting the **Enable PLL Reconfiguration** option in the ALTGX MegaWizard under **Reconfiguration Setting** tab. For multipurpose PLL or general purpose PLL reconfiguration, .mif files are required to dynamically reconfigure the PLL setting in order to change the output frequency of the transceiver PLL to support different data rates.

Chapter Revision Dates

The chapters in this document, Cyclone IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Cyclone IV Device Datasheet
Revised: *December 2016*
Part Number: *CYIV-53001-2.1*

Table 1-16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices ⁽¹⁾

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V) ⁽²⁾		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 x V _{CCIO} ⁽³⁾	0.5 x V _{CCIO} ⁽³⁾	0.52 x V _{CCIO} ⁽³⁾	—	0.5 x V _{CCIO}	—
				0.47 x V _{CCIO} ⁽⁴⁾	0.5 x V _{CCIO} ⁽⁴⁾	0.53 x V _{CCIO} ⁽⁴⁾			

Notes to Table 1-16:

- (1) For an explanation of terms used in Table 1-16, refer to “Glossary” on page 1-37.
- (2) V_{TT} of the transmitting device must track V_{REF} of the receiving device.
- (3) Value shown refers to DC input reference voltage, V_{REF(DC)}.
- (4) Value shown refers to AC input reference voltage, V_{REF(AC)}.

Table 1-17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices

I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)		V _{IH(AC)} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V _{REF} - 0.18	V _{REF} + 0.18	—	—	V _{REF} - 0.35	V _{REF} + 0.35	—	V _{TT} - 0.57	V _{TT} + 0.57	8.1	-8.1
SSTL-2 Class II	—	V _{REF} - 0.18	V _{REF} + 0.18	—	—	V _{REF} - 0.35	V _{REF} + 0.35	—	V _{TT} - 0.76	V _{TT} + 0.76	16.4	-16.4
SSTL-18 Class I	—	V _{REF} - 0.125	V _{REF} + 0.125	—	—	V _{REF} - 0.25	V _{REF} + 0.25	—	V _{TT} - 0.475	V _{TT} + 0.475	6.7	-6.7
SSTL-18 Class II	—	V _{REF} - 0.125	V _{REF} + 0.125	—	—	V _{REF} - 0.25	V _{REF} + 0.25	—	0.28	V _{CCIO} - 0.28	13.4	-13.4
HSTL-18 Class I	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	8	-8
HSTL-18 Class II	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	16	-16
HSTL-15 Class I	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	8	-8
HSTL-15 Class II	—	V _{REF} - 0.1	V _{REF} + 0.1	—	—	V _{REF} - 0.2	V _{REF} + 0.2	—	0.4	V _{CCIO} - 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 x V _{CCIO}	0.75 x V _{CCIO}	8	-8
HSTL-12 Class II	-0.15	V _{REF} - 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	-0.24	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.24	0.25 x V _{CCIO}	0.75 x V _{CCIO}	14	-14

IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.054	1.924	3.387	4.017	3.411	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.010	1.875	3.341	4.252	3.367	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.641	0.631	1.111	1.377	1.124	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.971	0.931	1.684	2.298	1.684	ns

Notes to Table 1–40:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.057	1.921	3.389	4.146	3.412	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.059	1.919	3.420	4.374	3.441	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.670	0.623	1.160	1.420	1.168	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.960	0.919	1.656	2.258	1.656	ns

Notes to Table 1–41:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1-46. Glossary (Part 5 of 5)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage.
	$V_{IL(DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} - V_{OL}$.
	V_{OH}	Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level.
	V_{OL}	Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX(AC)}$	AC differential output cross point voltage: the voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for the SSTL and HSTL I/O standards.
	$V_{REF(AC)}$	AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)} + \text{noise}$. The peak-to-peak AC noise on V_{REF} must not exceed 2% of $V_{REF(DC)}$.
	$V_{REF(DC)}$	DC input reference voltage for the SSTL and HSTL I/O standards.
	$V_{SWING(AC)}$	AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	$V_{SWING(DC)}$	DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	V_{TT}	Termination voltage for the SSTL and HSTL I/O standards.
	$V_X(AC)$	AC differential input cross point voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—