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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3491
Number of Logic Elements/Cells	55856
Total RAM Bits	2396160
Number of I/O	324
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce55f23c7n

Chapter 7. External Memory Interfaces in Cyclone IV Devices

Section III. System Integration

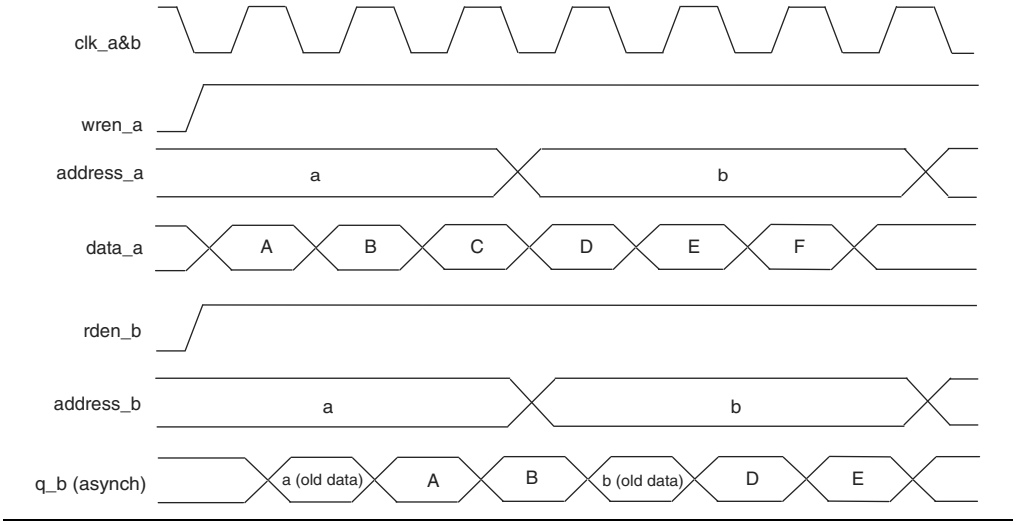
Chapter 8. Configuration and Remote System Upgrades in Cyclone IV Devices

In this mode, you also have two output choices: **Old Data** mode or **Don't Care** mode. In **Old Data** mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In **Don't Care** mode, the same operation results in a "Don't Care" or unknown value on the RAM outputs.

For more information about how to implement the desired behavior, refer to the *RAM Megafunction User Guide*.

Figure 3–16 shows a sample functional waveform of mixed port read-during-write behavior for **Old Data** mode. In **Don't Care** mode, the old data is replaced with "Don't Care".

Figure 3–16. Mixed Port Read-During-Write: Old Data Mode



For mixed-port read-during-write operation with dual clocks, the relationship between the clocks determines the output behavior of the memory. If you use the same clock for the two clocks, the output is the old data from the address location. However, if you use different clocks, the output is unknown during the mixed-port read-during-write operation. This unknown value may be the old or new data at the address location, depending on whether the read happens before or after the write.

Conflict Resolution

When you are using M9K memory blocks in true dual-port mode, it is possible to attempt two write operations to the same memory location (address). Because there is no conflict resolution circuitry built into M9K memory blocks, this results in unknown data being written to that location. Therefore, you must implement conflict-resolution logic external to the M9K memory block.

4. Embedded Multipliers in Cyclone IV Devices

CYIV-51004-1.1

Cyclone® IV devices include a combination of on-chip resources and external interfaces that help increase performance, reduce system cost, and lower the power consumption of digital signal processing (DSP) systems. Cyclone IV devices, either alone or as DSP device co-processors, are used to improve price-to-performance ratios of DSP systems. Particular focus is placed on optimizing Cyclone IV devices for applications that benefit from an abundance of parallel processing resources, which include video and image processing, intermediate frequency (IF) modems used in wireless communications systems, and multi-channel communications and video systems.

This chapter contains the following sections:

Embedded Multiplier Block Overview

Figure 4–1 shows one of the embedded multiplier columns with the surrounding logic array blocks (LABs). The embedded multiplier is configured as either one 18 × 18 multiplier or two 9 × 9 multipliers. For multiplications greater than 18 × 18, the Quartus® II software cascades multiple embedded multiplier blocks together. There are no restrictions on the data width of the multiplier, but the greater the data width, the slower the multiplication process.

Figure 4–1. Embedded Multipliers Arranged in Columns with Adjacent LABs

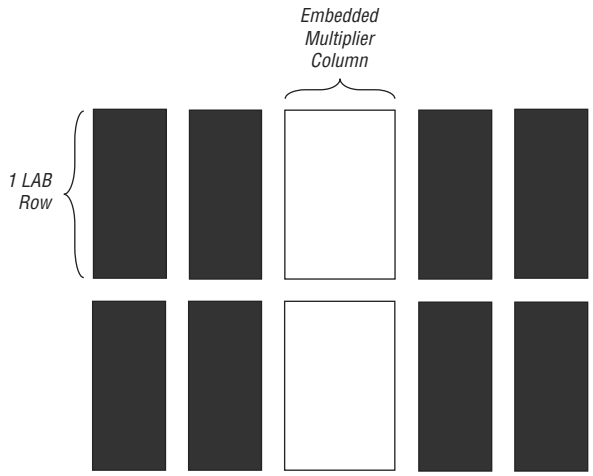


Table 4–2 lists the sign of the multiplication results for the various operand sign representations. The results of the multiplication are signed if any one of the operands is a signed value.

Table 4–2. Multiplier Sign Representation

Data A		Data B		Result
signa Value	Logic Level	signb Value	Logic Level	
Unsigned	Low	Unsigned	Low	Unsigned
Unsigned	Low	Signed	High	Signed
Signed	High	Unsigned	Low	Signed
Signed	High	Signed	High	Signed

Each embedded multiplier block has only one `signa` and one `signb` signal to control the sign representation of the input data to the block. If the embedded multiplier block has two 9 × 9 multipliers, the `Data A` input of both multipliers share the same `signa` signal, and the `Data B` input of both multipliers share the same `signb` signal. You can dynamically change the `signa` and `signb` signals to modify the sign representation of the input operands at run time. You can send the `signa` and `signb` signals through a dedicated input register. The multiplier offers full precision, regardless of the sign representation.

☞ When the `signa` and `signb` signals are unused, the Quartus II software sets the multiplier to perform unsigned multiplication by default.

Output Registers

You can register the embedded multiplier output with output registers in either 18- or 36-bit sections, depending on the operational mode of the multiplier. The following control signals are available for each output register in the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers in a single embedded multiplier are fed by the same clock, clock enable, and asynchronous clear signals.

Operational Modes

You can use an embedded multiplier block in one of two operational modes, depending on the application needs:

- One 18 × 18 multiplier
- Up to two 9 × 9 independent multipliers

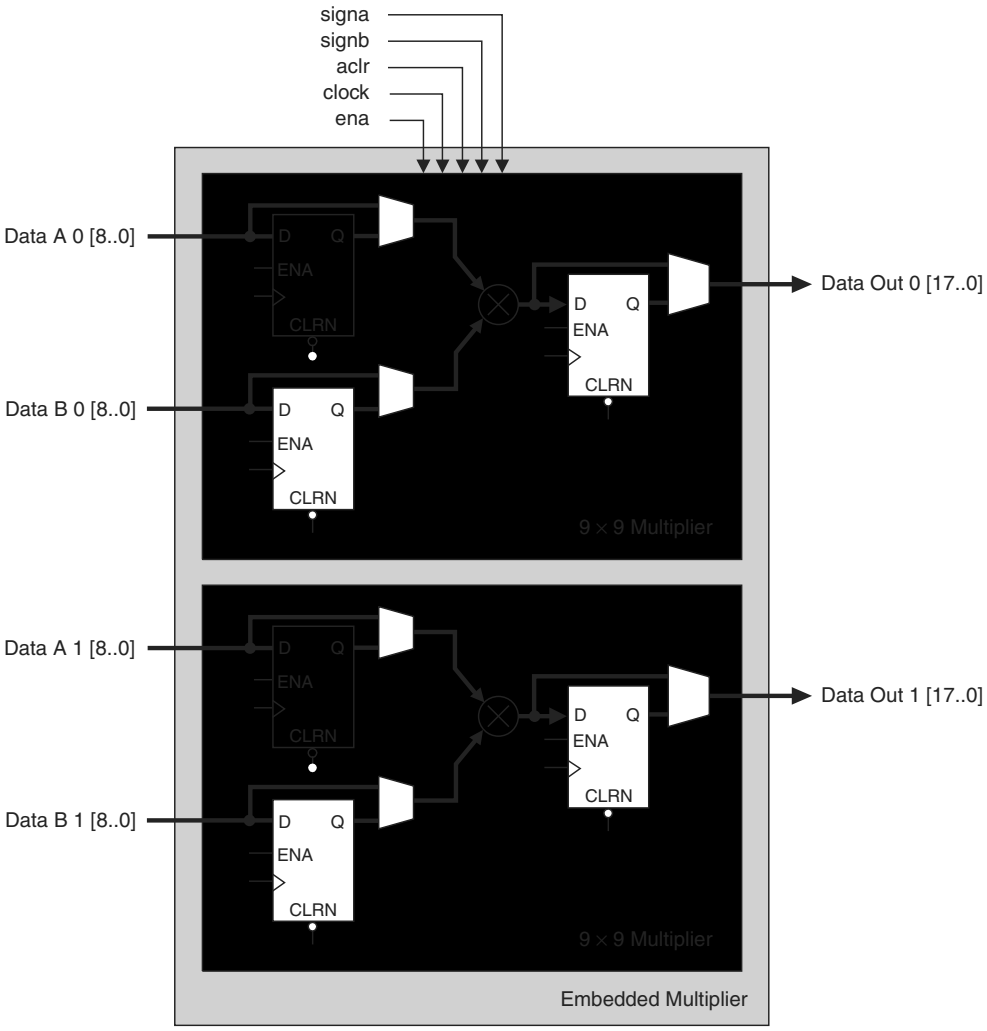
☞ You can also use embedded multipliers of Cyclone IV devices to implement multiplier adder and multiplier accumulator functions, in which the multiplier portion of the function is implemented with embedded multipliers, and the adder or accumulator function is implemented in logic elements (LEs).

9-Bit Multipliers

You can configure each embedded multiplier to support two 9 × 9 independent multipliers for input widths of up to 9 bits.

Figure 4–4 shows the embedded multiplier configured to support two 9-bit multipliers.

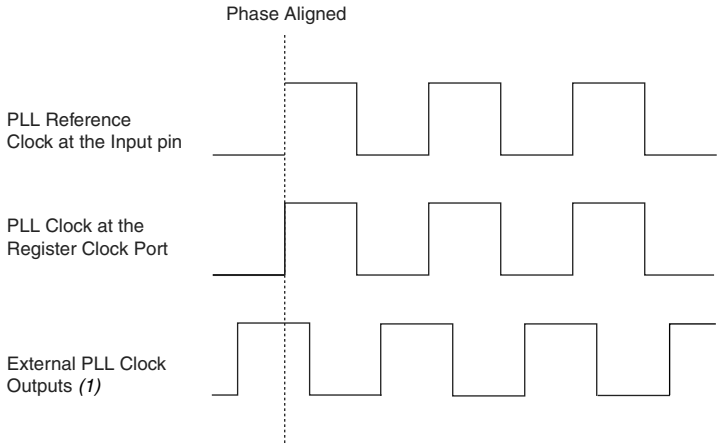
Figure 4–4. 9-Bit Multiplier Mode



All 9-bit multiplier inputs and results are independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Two 9 × 9 multipliers in the same embedded multiplier block share the same `signa` and `signb` signal. Therefore, all the `Data A` inputs feeding the same embedded multiplier must have the same sign representation. Similarly, all the `Data B` inputs feeding the same embedded multiplier must have the same sign representation.

Figure 5–14 shows a waveform example of the phase relationship of the PLL clocks in this mode.

Figure 5–14. Phase Relationship Between PLL Clocks in Normal Mode



Note to Figure 5–14:

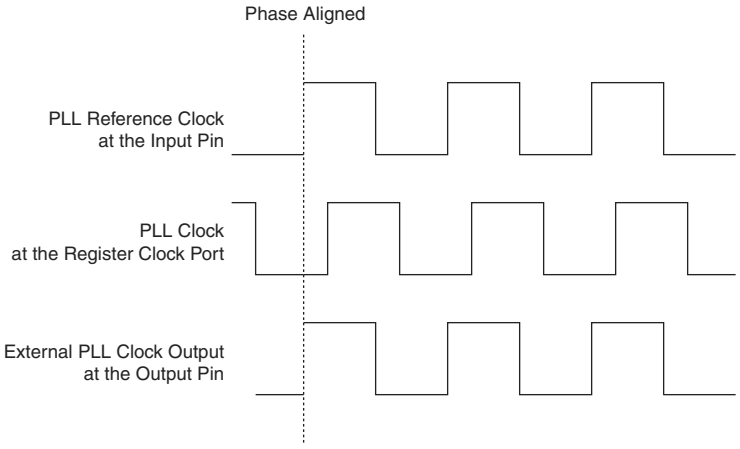
(1) The external clock output can lead or lag the PLL internal clock signals.

Zero Delay Buffer Mode

In zero delay buffer (ZDB) mode, the external clock output pin is phase-aligned with the clock input pin for zero delay through the device. When using this mode, use the same I/O standard on the input clock and output clocks to guarantee clock alignment at the input and output pins.

Figure 5–15 shows an example waveform of the phase relationship of the PLL clocks in ZDB mode.

Figure 5–15. Phase Relationship Between PLL Clocks in ZDB Mode



Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figure 6–5 and Figure 6–6.

Figure 6–5. Cyclone IV Devices HSTL I/O Standard Termination

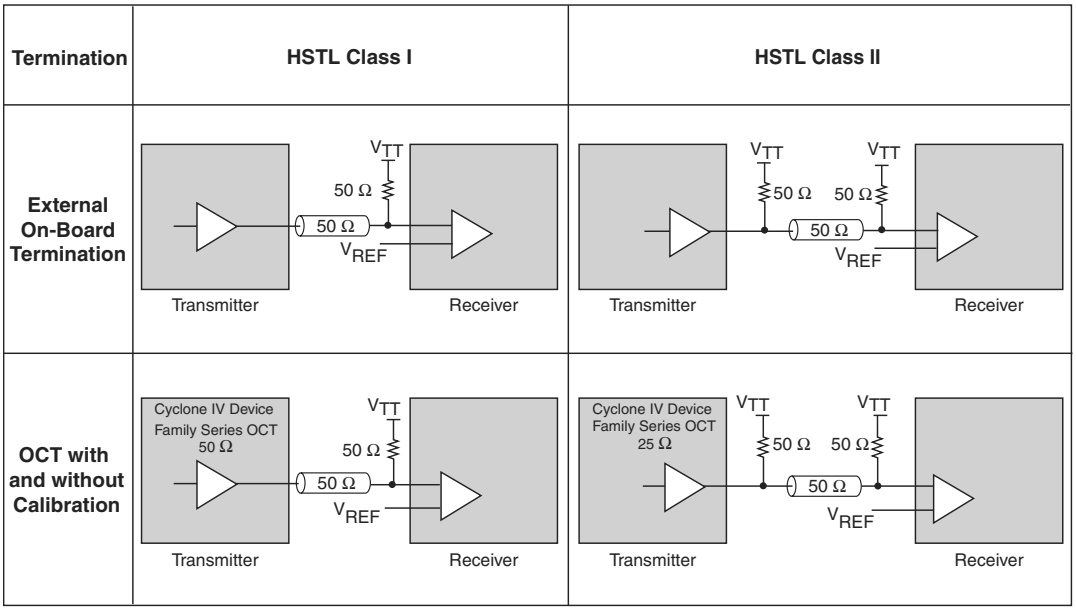
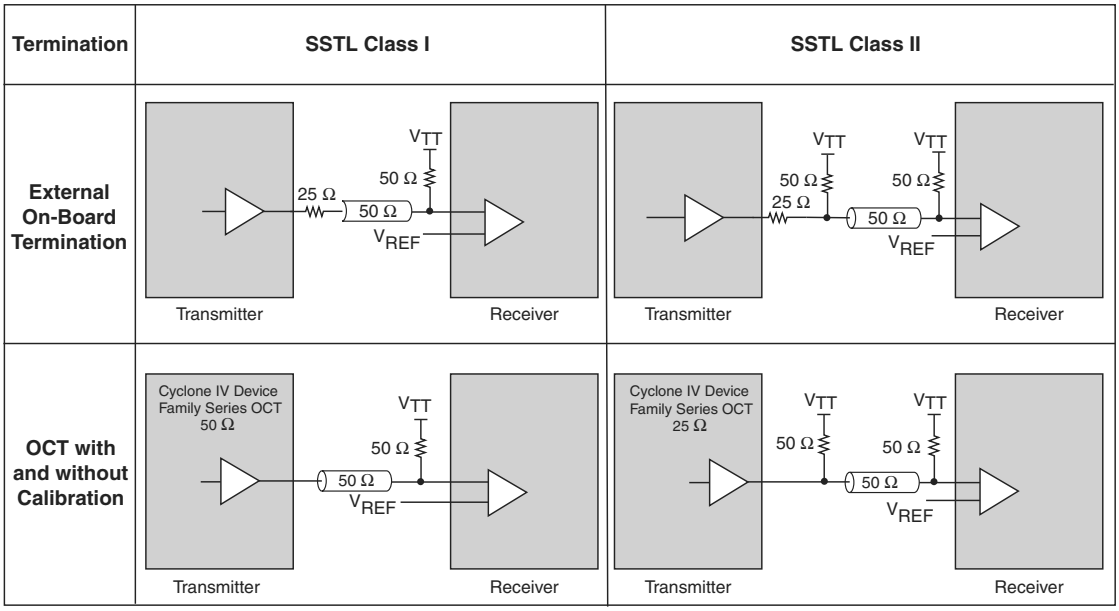


Figure 6–6. Cyclone IV Devices SSTL I/O Standard Termination



7. External Memory Interfaces in Cyclone IV Devices

CYIV-51007-2.6

This chapter describes the memory interface pin support and the external memory interface features of Cyclone® IV devices.

In addition to an abundant supply of on-chip memory, Cyclone IV devices can easily interface with a broad range of external memory devices, including DDR2 SDRAM, DDR SDRAM, and QDR II SRAM. External memory devices are an important system component of a wide range of image processing, storage, communications, and general embedded applications.

Altera recommends that you construct all DDR2 or DDR SDRAM external memory interfaces using the Altera® ALTMEMPHY megafunction. You can implement the controller function using the Altera DDR2 or DDR SDRAM memory controllers, third-party controllers, or a custom controller for unique application needs. Cyclone IV devices support QDR II interfaces electrically, but Altera does not supply controller or physical layer (PHY) megafunctions for QDR II interfaces.

This chapter includes the following sections:

For more information about supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to the *External Memory Interface Handbook*.

Figure 7–3 shows the location and numbering of the DQS, DQ, or CQ# pins in I/O banks of the Cyclone IV GX device in the 324-pin FBGA package only.

Figure 7–3. DQS, CQ, or CQ# Pins for Cyclone IV GX Devices in the 324-Pin FBGA Package

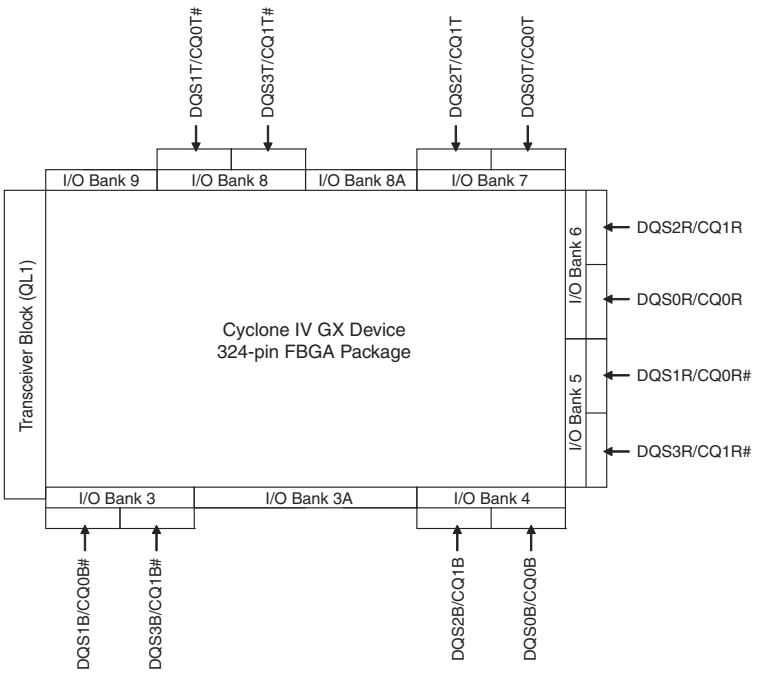


Figure 7–4 shows the location and numbering of the DQS, DQ, or CQ# pins in I/O banks of the Cyclone IV GX device in the 169-pin FBGA package.

Figure 7–4. DQS, CQ, or CQ# Pins for Cyclone IV GX Devices in the 169-Pin FBGA Package

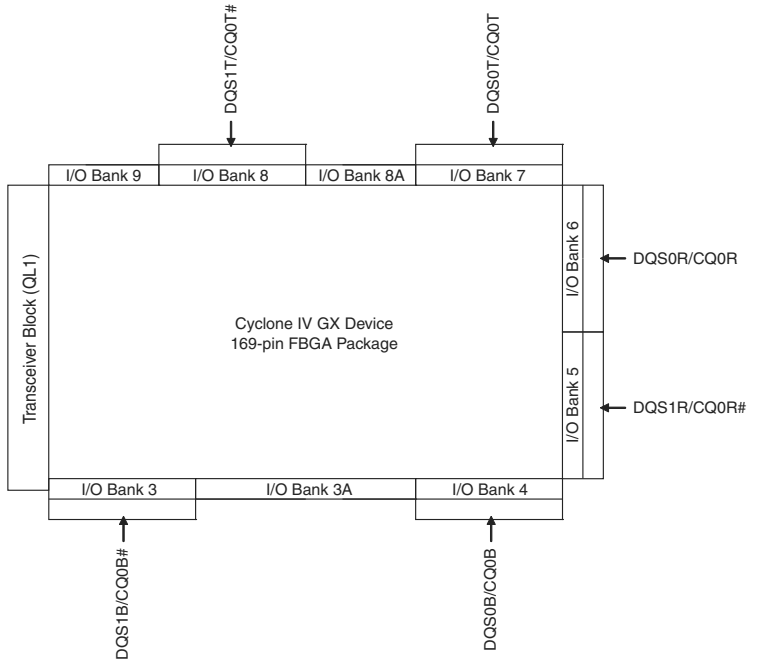
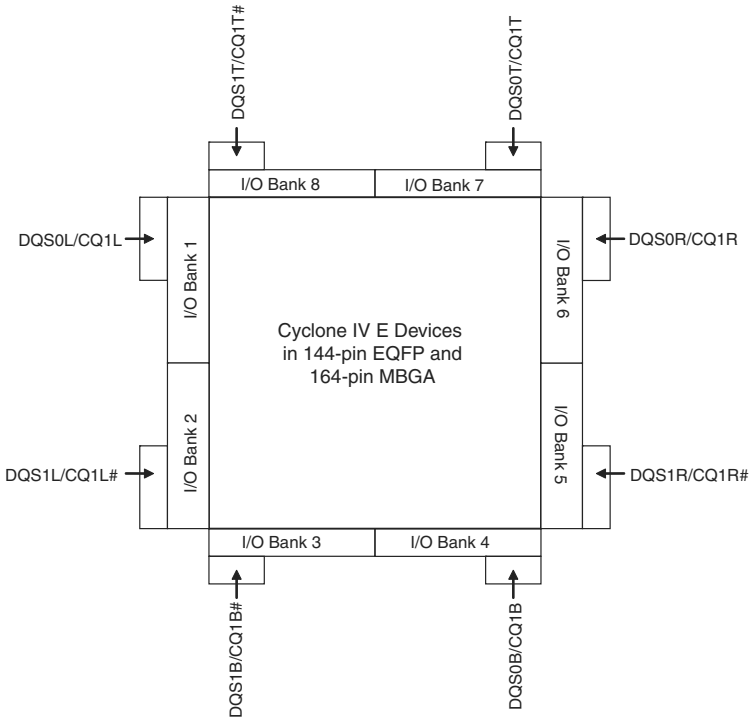


Figure 7–6 shows the location and numbering of the DQS, DQ, or CQ# pins in I/O banks of the Cyclone IV E device in the 144-pin EQFP and 164-pin MBGA packages.

Figure 7–6. DQS, CQ, or CQ# Pins for Cyclone IV E Devices in the 144-Pin EQFP and 164-pin MBGA Packages



In Cyclone IV devices, the ×9 mode uses the same DQ and DQS pins as the ×8 mode, and one additional DQ pin that serves as a regular I/O pin in the ×8 mode. The ×18 mode uses the same DQ and DQS pins as ×16 mode, with two additional DQ pins that serve as regular I/O pins in the ×16 mode. Similarly, the ×36 mode uses the same DQ and DQS pins as the ×32 mode, with four additional DQ pins that serve as regular I/O pins in the ×32 mode. When not used as DQ or DQS pins, the memory interface pins are available as regular I/O pins.

Optional Parity, DM, and Error Correction Coding Pins

Cyclone IV devices support parity in ×9, ×18, and ×36 modes. One parity bit is available per eight bits of data pins. You can use any of the DQ pins for parity in Cyclone IV devices because the parity pins are treated and configured similarly to DQ pins.

DM pins are only required when writing to DDR2 and DDR SDRAM devices. QDR II SRAM devices use the BWS# signal to select the byte to be written into memory. A low signal on the DM or BWS# pin indicates the write is valid. Driving the DM or BWS# pin high causes the memory to mask the DQ signals. Each group of DQS and DQ signals has one DM pin. Similar to the DQ output signals, the DM signals are clocked by the -90° shifted clock.

The nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors, as shown in Figure 8–8 on page 8–26 and Figure 8–9 on page 8–27. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they receive their configuration data. When all target devices in the chain receive their configuration data and release CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

Guidelines for Connecting Parallel Flash to Cyclone IV E Devices for an AP Interface

For single- and multi-device AP configuration, the board trace length and loading between the supported parallel flash and Cyclone IV E devices must follow the recommendations listed in Table 8–11. These recommendations also apply to an AP configuration with multiple bus masters.

Table 8–11. Maximum Trace Length and Loading for AP Configuration

Cyclone IV E AP Pins	Maximum Board Trace Length from Cyclone IV E Device to Flash Device (inches)	Maximum Board Load (pF)
DCLK	6	15
DATA[15..0]	6	30
PADD[23..0]	6	30
nRESET	6	30
Flash_nCE	6	30
nOE	6	30
nAVD	6	30
nWE	6	30
I/O (1)	6	30

Note to Table 8–11:

(1) The AP configuration ignores the WAIT signal from the flash during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.

Configuring With Multiple Bus Masters

Similar to the AS configuration scheme, the AP configuration scheme supports multiple bus masters for the parallel flash. For another master to take control of the AP configuration bus, the master must assert nCONFIG low for at least 500 ns to reset the master Cyclone IV E device and override the weak 10-kΩ pull-down resistor on the nCE pin. This resets the master Cyclone IV E device and causes it to tri-state its AP configuration bus. The other master device then takes control of the AP configuration bus. After the other master device is done, it releases the AP configuration bus, then releases the nCE pin, and finally pulses nCONFIG low to restart the configuration.

In the AP configuration scheme, multiple masters share the parallel flash. Similar to the AS configuration scheme, the bus control is negotiated by the nCE pin.

Remote System Upgrade Registers

The remote system upgrade block contains a series of registers that stores the configuration addresses, watchdog timer settings, and status information. Table 8–22 lists these registers.

Table 8–22. Remote System Upgrade Registers

Register	Description
Shift register	This register is accessible by the logic array and allows the update, status, and control registers to be written and sampled by user logic. Write access is enabled in remote update mode for factory configurations to allow writing to the update register. Write access is disabled for all application configurations in remote update mode.
Control register	This register contains the current configuration address, the user watchdog timer settings, one option bit for checking early CONF_DONE, and one option bit for selecting the internal oscillator as the startup state machine clock. During a read operation in an application configuration, this register is read into the shift register. When a reconfiguration cycle is started, the contents of the update register are written into the control register.
Update register	This register contains data similar to that in the control register. However, it can only be updated by the factory configuration by shifting data into the shift register and issuing an update operation. When a reconfiguration cycle is triggered by the factory configuration, the control register is updated with the contents of the update register. During a read in a factory configuration, this register is read into the shift register.
Status register	This register is written by the remote system upgrade circuitry on every reconfiguration to record the cause of the reconfiguration. This information is used by the factory configuration to determine the appropriate action following a reconfiguration. During a capture cycle, this register is read into the shift register.

The control and status registers of the remote system upgrade are clocked by the 10-MHz internal oscillator (the same oscillator that controls the user watchdog timer) or the CLKUSR. However, the shift and update registers of the remote system upgrade are clocked by the maximum frequency of 40-MHz user clock input (RU_CLK). There is no minimum frequency for RU_CLK.

Remote System Upgrade Control Register

The remote system upgrade control register stores the application configuration address, the user watchdog timer settings, and option bits for a application configuration. In remote update mode for the AS configuration scheme, the control register address bits are set to all zeros (24'b0) at power up to load the AS factory configuration. In remote update mode for the AP configuration scheme, the control register address bits are set to 24'h010000 (24'b1 0000 0000 0000 0000) at power up to load the AP default factory configuration. However, for the AP configuration scheme, you can change the default factory configuration address to any desired address using the APFC_BOOT_ADDR JTAG instruction. Additionally, a factory configuration in remote update mode has write access to this register.

Configuration error detection determines if the configuration data received through an external memory device is corrupted during configuration. To validate the configuration data, the Quartus® II software uses a function to calculate the CRC value for each configuration data frame and stores the frame-based CRC value in the configuration data as part of the configuration bit stream.

During configuration, Cyclone IV devices use the same methodology to calculate the CRC value based on the frame of data that is received and compares it against the frame CRC value in the data stream. Configuration continues until either the device detects an error or all the values are calculated.

In addition to the frame-based CRC value, the Quartus II software generates a 32-bit CRC value for the whole configuration bit stream. This 32-bit CRC value is stored in the 32-bit storage register at the end of the configuration and is used for user mode error detection that is discussed in "User Mode Error Detection".

User Mode Error Detection

☞ User mode error detection is available in Cyclone IV GX and Cyclone IV E devices with 1.2-V core voltage. Cyclone IV E devices with 1.0-V core voltage do not support user mode error detection.

Soft errors are changes in a configuration random-access memory (CRAM) bit state due to an ionizing particle. Cyclone IV devices have built-in error detection circuitry to detect data corruption by soft errors in the CRAM cells.

This error detection capability continuously computes the CRC of the configured CRAM bits based on the contents of the device and compares it with the pre-calculated CRC value obtained at the end of the configuration. If the CRCs match, there is no error in the current configuration CRAM bits. The process of error detection continues until the device is reset (by setting `nCONFIG` to low).

The Cyclone IV device error detection feature does not check memory blocks and I/O buffers. These device memory blocks support parity bits that are used to check the contents of memory blocks for any error. The I/O buffers are not verified during error detection because the configuration data uses flip-flops as storage elements that are more resistant to soft errors. Similar flip-flops are used to store the pre-calculated CRC and other error detection circuitry option bits.

The error detection circuitry in Cyclone IV devices uses a 32-bit CRC IEEE 802 standard and a 32-bit polynomial as the CRC generator. Therefore, a single 32-bit CRC calculation is performed by the device. If a soft error does not occur, the resulting 32-bit signature value is `0x00000000`, that results in a `0` on the `CRC_ERROR` output signal. If a soft error occurs in the device, the resulting signature value is non-zero and the `CRC_ERROR` output signal is `1`.

You can inject a soft error by changing the 32-bit CRC storage register in the CRC circuitry. After verifying the induced failure, you can restore the 32-bit CRC value to the correct CRC value with the same instruction and inserting the correct value.

☞ Before updating it with a known bad value, Altera recommends reading out the correct value.

Fast Recovery from P0s State

The PCIe protocol defines fast training sequences for bit and byte synchronization to transition from L0s to L0 (PIPE P0s to P0) power states. The PHY must acquire bit and byte synchronization when transitioning from L0s to L0 state between 16 ns to 4 µs. Each Cyclone IV GX receiver channel has built-in fast recovery circuit that allows the receiver to meet the requirement when enabled.

Electrical Idle Inference

In PIPE mode, the Cyclone IV GX transceiver supports inferring the electrical idle condition at each receiver instead of detecting the electrical idle condition using analog circuitry, as defined in the version 2.0 of PCIe Base Specification. The inference is supported using `rx_elecidleinfersel[2..0]` port, with valid driven values as listed in Table 1–17 in each link training and status state machine substate.

Table 1–17. Electrical Idle Inference Conditions

rx_elecidleinfersel [2..0]	Link Training and Status State Machine State	Description
3'b100	L0	Absence of `update_FC` or alternatively skip ordered set in 128 µs window
3'b101	Recovery.RcvrCfg	Absence of `TS1` or `TS2` ordered set in 1280 UI interval
3'b101	Recovery.Speed when successful speed negotiation = 1'b1	Absence of `TS1` or `TS2` ordered set in 1280 UI interval
3'b110	Recovery.Speed when successful speed negotiation = 1'b0	Absence of an exit from electrical idle in 2000 UI interval
3'b111	Loopback.Active (as slave)	Absence of an exit from electrical idle in 128 µs window

The electrical idle inference module drives the `pipeelecidle` signal high in each receiver channel when an electrical idle condition is inferred. The electrical idle inference module cannot detect electrical idle exit condition based on the reception of the electrical idle exit ordered set, as specified in the PCI Express (PIPE) Base Specification.

When enabled, the electrical idle inference block uses electrical idle ordered set detection from the fast recovery circuitry to drive the `pipeelecidle` signal.

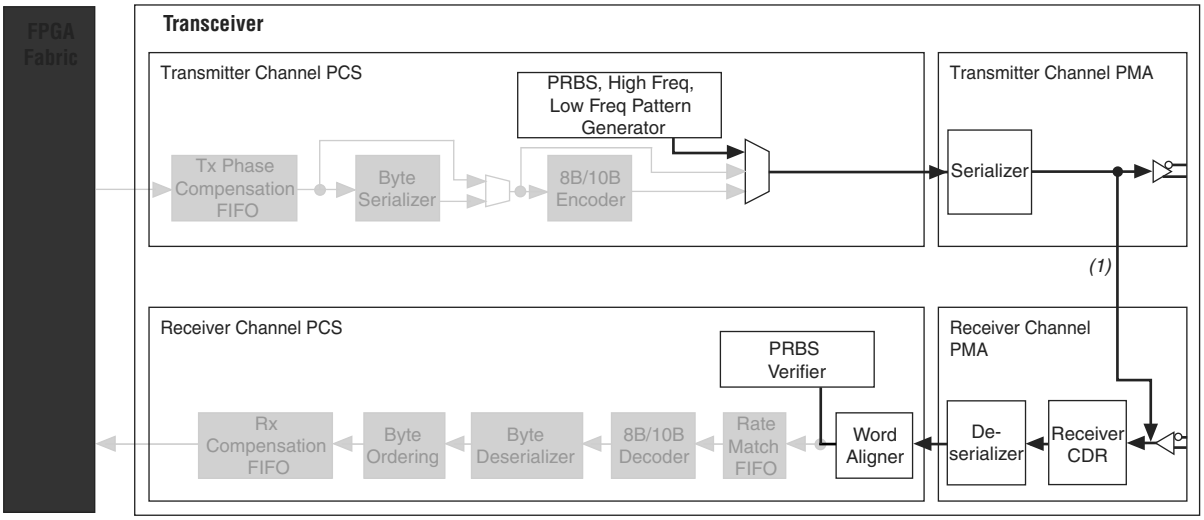
Compliance Pattern Transmission

In PIPE mode, the Cyclone IV GX transceiver supports compliance pattern transmission which requires the first /K28.5/ code group of the compliance pattern to be encoded with negative current disparity. This requirement is supported using a `tx_forcedispcompliance` port that when driven with logic high, the transmitter data on the `tx_datain` port is transmitted with negative current running disparity.

PRBS

Figure 1–74 shows the datapath for the PRBS, high and low frequency pattern test modes. The pattern generator is located in TX PCS before the serializer, and PRBS pattern verifier located in RX PCS after the word aligner.

Figure 1–74. PRBS Pattern Test Mode Datapath



Note to Figure 1–74:

(1) Serial loopback path is optional and can be enabled for the PRBS verifier to check the PRBS pattern

Table 1–25 lists the supported PRBS, high and low frequency patterns, and corresponding channel settings. The PRBS pattern repeats after completing an iteration. The number of bits a PRBS X pattern sends before repeating the pattern is $2^{(X-1)}$ bits.

Table 1–25. PRBS, High and Low Frequency Patterns, and Channel Settings (Part 1 of 2)

Patterns	Polynomial	8-bit Channel Width				10-bit Channel Width			
		Channel Width of 8 bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages	Channel Width of 10-bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages
PRBS 7	$X^7 + X^6 + 1$	Y	16'h3040	2.0	2.5	N	—	—	—
PRBS 8	$X^8 + X^7 + 1$	Y	16'hFF5A	2.0	2.5	N	—	—	—
PRBS 10	$X^{10} + X^7 + 1$	N	—	—	—	Y	10'h3FF	2.5	3.125
PRBS 23	$X^{23} + X^{18} + 1$	Y	16'hFFFF	2.0	2.5	N	—	—	—
High frequency (2)	1010101010	Y	—	2.0	2.5	Y	—	2.5	3.125

Document Revision History

Table 1–30 lists the revision history for this chapter.

Table 1–30. Document Revision History

Date	Version	Changes
February 2015	3.7	■ Updated the GiGE row in Table 1–14. ■ Updated the "GIGE Mode" section. ■ Updated the note in the "Clock Frequency Compensation" section.
October 2013	3.6	Updated Figure 1–15 and Table 1–4.
May 2013	3.5	Updated Table 1–27 by setting "rx_locktodata" and "rx_locktorefclk" to "Input"
October 2012	3.4	■ Updated the data rate for the V-by-one protocol and the F324 package support in HD-SDI in Table 1–1. ■ Updated note (1) to Figure 1–27. ■ Added latency information to Figure 1–67.
November 2011	3.3	■ Updated "Word Aligner" and "Basic Mode" sections. ■ Updated Figure 1–37.
December 2010	3.2	■ Updated for the Quartus II software version 10.1 release. ■ Updated Table 1–1, Table 1–5, Table 1–11, Table 1–14, Table 1–24, Table 1–25, Table 1–26, Table 1–27, Table 1–28, and Table 1–29. ■ Updated "8B/10B Encoder", "Transmitter Output Buffer", "Receiver Input Buffer", "Clock Data Recovery", "Miscellaneous Transmitter PCS Features", "Miscellaneous Receiver PCS Feature", "Input Reference Clocking", "PCI Express (PIPE) Mode", "Channel Deskewing", "Lane Synchronization", "Serial Loopback", and "Self Test Modes" sections. ■ Added Figure 1–9, Figure 1–10, Figure 1–19, Figure 1–20, and Figure 1–43. ■ Updated Figure 1–53, Figure 1–55, Figure 1–59, Figure 1–60, Figure 1–69, Figure 1–70, Figure 1–71, Figure 1–72, Figure 1–73, and Figure 1–74.
November 2010	3.1	Updated Introductory information.
July 2010	3.0	■ Updated information for the Quartus II software version 10.0 release. ■ Reset control, power down, and dynamic reconfiguration information moved to new *Cyclone IV Reset Control and Power Down* and *Cyclone IV Dynamic Reconfiguration* chapters.

4. Wait for at least $t_{LTR\_LTD\_Manual}$ (the time between markers 6 and 7), then deassert the `rx_locktorefclk` signal. At the same time, assert the `rx_locktodata` signal (marker 7). At this point, the receiver CDR enters lock-to-data mode and the receiver CDR starts locking to the received data.
5. Deassert `rx_digitalreset` at least t_{LTD_Manual} (the time between markers 7 and 8) after asserting the `rx_locktodata` signal. At this point, the transmitter and receiver are ready for data traffic.

Reset Sequence in Loss of Link Conditions

Loss of link can occur due to loss of local reference clock source or loss of the link due to an unplugged cable. Other adverse conditions like loss of power could also cause the loss of signal from the other device or link partner.

Loss of Local REFCLK or Other Reference Clock Condition

Should local reference clock input become disabled or unstable, take the following steps:

1. Monitor `pll_locked` signal. `Pll_locked` is de-asserted if local reference clock source becomes unavailable.
2. `Pll_locked` assertion indicates a stable reference clock because TX PLL locks to the incoming clock. You can follow appropriate reset sequence provided in the device handbook, starting from `pll_locked` assertion.

Loss of Link Due To Unplugged Cable or Far End Shut-off Condition

Use one or more of the following methods to identify whether link partner is alive:

- Signal detect is available in PCIe and Basic modes. You can monitor `rx_signaldetect` signal as loss of link indicator. `rx_signaldetect` is asserted when the link partner comes back up.
- You can implement a ppm detector in device core for modes that do not have signal detect to monitor the link. Ppm detector helps in identifying whether the link is alive.
- Data corruption or RX phase comp FIFO overflow or underflow condition in user logic may indicate a loss of link condition.

Apply the following reset sequences when loss of link is detected:

- For Automatic CDR lock mode:
  a. Monitor `rx_freqlocked` signal. Loss of link causes `rx_freqlocked` to be de-asserted when CDR moves back to lock-to-data (LTD) mode.
  b. Assert `rx_digitalreset`.
  c. `rx_freqlocked` toggles over time when CDR switches between lock-to-reference (LTR) and LTD modes.
  d. If `rx_freqlocked` goes low at any point, re-assert `rx_digitalreset`.
  e. If data corruption or RX phase comp FIFO overflow or underflow condition is observed in user logic, assert `rx_digitalreset` for 2 parallel clock cycles, then de-assert the signal.

Table 3–5. rx_dataoutfull[31..0] FPGA Fabric-Transceiver Channel Interface Signal Descriptions (Part 2 of 3)

FPGA Fabric-Transceiver Channel Interface Description	Receive Signal Description (Based on Cyclone IV GX Supported FPGA Fabric-Transceiver Channel Interface Widths)
16-bit FPGA fabric-Transceiver Channel Interface with PCS-PMA set to 8/10 bits	Two 8-bit unencoded Data (rx_dataout) rx_dataoutfull[7:0] - rx_dataout (LSByte) and rx_dataoutfull[23:16]- rx_dataout (MSByte)
	The following signals are used in 16-bit 8B/10B modes:
	Two Control Bits rx_dataoutfull[8] - rx_ctrldetect (LSB) and rx_dataoutfull[24]- rx_ctrldetect (MSB)
	Two Receiver Error Detect Bits rx_dataoutfull[9] - rx_errdetect (LSB) and rx_dataoutfull[25]- rx_errdetect (MSB)
	Two Receiver Sync Status Bits rx_dataoutfull [10] - rx_syncstatus (LSB) and rx_dataoutfull[26] - rx_syncstatus (MSB)
	Two Receiver Disparity Error Bits rx_dataoutfull [11] - rx_disperr (LSB) and rx_dataoutfull[27] - rx_disperr (MSB)
	Two Receiver Pattern Detect Bits rx_dataoutfull[12] - rx_patterndetect (LSB) and rx_dataoutfull[28]- rx_patterndetect (MSB)
	rx_dataoutfull[13] and rx_dataoutfull[29]: Rate Match FIFO deletion status indicator (rx_rmfifodatadeleted) in non-PCI Express (PIPE) functional modes
	rx_dataoutfull[14] and rx_dataoutfull[30]: Rate Match FIFO insertion status indicator (rx_rmfifodatainserted) in non-PCI Express (PIPE) functional modes
	Two 2-bit PCI Express (PIPE) Functional Mode Status Bits rx_dataoutfull[14:13] - rx_pipestatus (LSB) and rx_dataoutfull[30:29] - rx_pipestatus (MSB)
	rx_dataoutfull[15] and rx_dataoutfull[31]: 8B/10B running disparity indicator (rx_runningdisp)

Figure 1–2 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.

Figure 1–2. Lock Time Parameters for Manual Mode

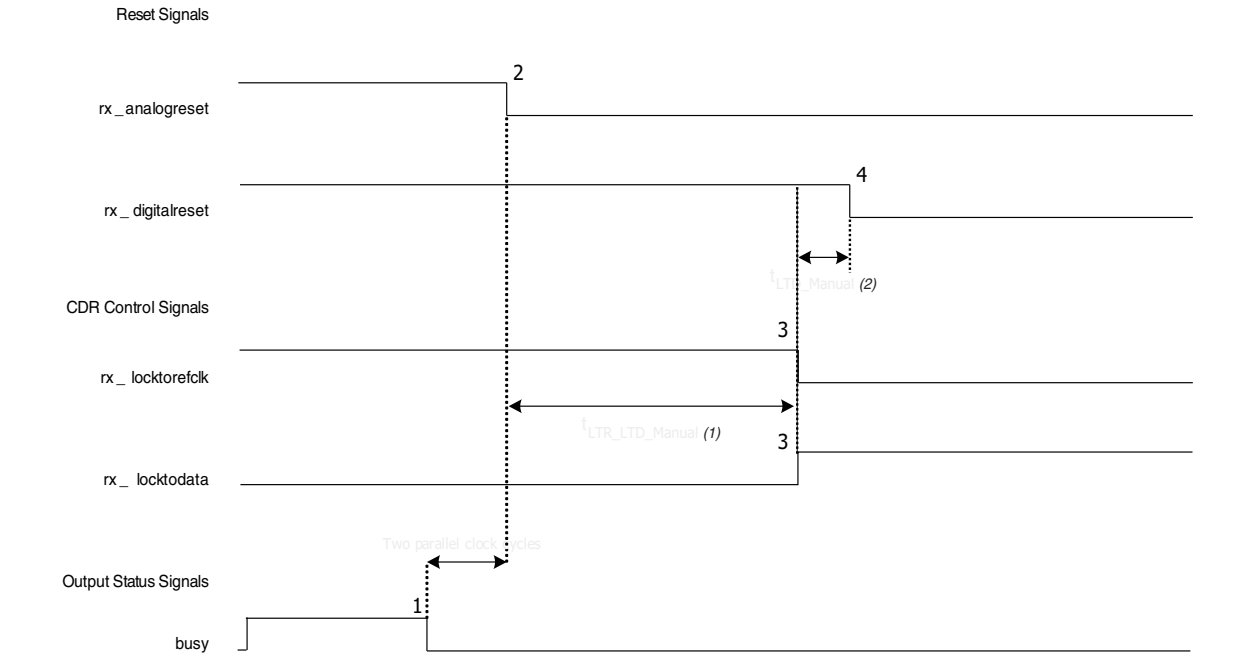


Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode