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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3491
Number of Logic Elements/Cells	55856
Total RAM Bits	2396160
Number of I/O	324
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce55f23c9l

3. Memory Blocks in Cyclone IV Devices

CYIV-51003-1.1

Cyclone® IV devices feature embedded memory structures to address the on-chip memory needs of Altera® Cyclone IV device designs. The embedded memory structure consists of columns of M9K memory blocks that you can configure to provide various memory functions, such as RAM, shift registers, ROM, and FIFO buffers.

This chapter contains the following sections:

- “Memory Modes” on page 3–7
- “Clocking Modes” on page 3–14
- “Design Considerations” on page 3–15

Overview

M9K blocks support the following features:

- 8,192 memory bits per block (9,216 bits per block including parity)
- Independent read-enable (*rden*) and write-enable (*wren*) signals for each port
- Packed mode in which the M9K memory block is split into two 4.5 K single-port RAMs
- Variable port configurations
- Single-port and simple dual-port modes support for all port widths
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Two clock-enable control signals for each port (port A and port B)
- Initialization file to pre-load memory content in RAM and ROM modes

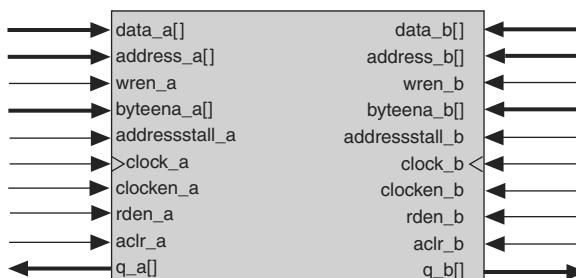
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True Dual-Port Mode

True dual-port mode supports any combination of two-port operations: two reads, two writes, or one read and one write, at two different clock frequencies. Figure 3–10 shows Cyclone IV devices true dual-port memory configuration.

Figure 3–10. Cyclone IV Devices True Dual-Port Memory ⁽¹⁾



Note to Figure 3–10:

(1) True dual-port memory supports input or output clock mode in addition to the independent clock mode shown.

 The widest bit configuration of the M9K blocks in true dual-port mode is 512 × 16-bit (18-bit with parity).

Table 3–4 lists the possible M9K block mixed-port width configurations.

Table 3–4. Cyclone IV Devices M9K Block Mixed-Width Configurations (True Dual-Port Mode)

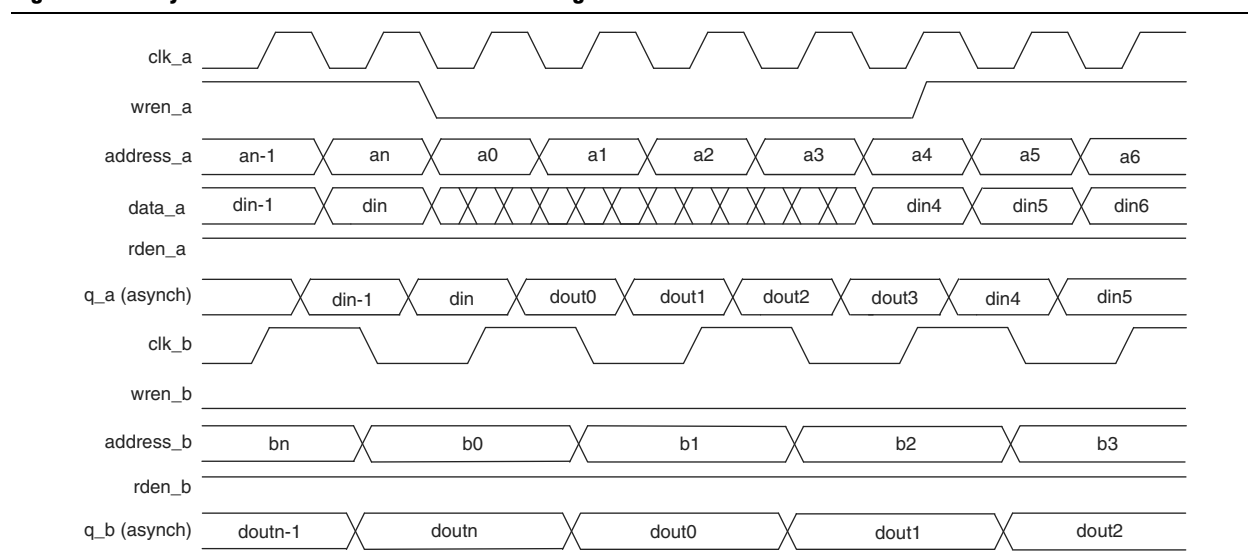
Read Port	Write Port						
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	1024 × 9	512 × 18
8192 × 1	✓	✓	✓	✓	✓	—	—
4096 × 2	✓	✓	✓	✓	✓	—	—
2048 × 4	✓	✓	✓	✓	✓	—	—
1024 × 8	✓	✓	✓	✓	✓	—	—
512 × 16	✓	✓	✓	✓	✓	—	—
1024 × 9	—	—	—	—	—	✓	✓
512 × 18	—	—	—	—	—	✓	✓

In true dual-port mode, M9K memory blocks support separate wren and rden signals. You can save power by keeping the rden signal low (inactive) when not reading. Read-during-write operations to the same address can either output “New Data” at that location or “Old Data”. To choose the desired behavior, set the **Read-During-Write** option to either **New Data** or **Old Data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information about this behavior, refer to “Read-During-Write Operations” on page 3–15.

In true dual-port mode, you can access any memory location at any time from either port A or port B. However, when accessing the same memory location from both ports, you must avoid possible write conflicts. When you attempt to write to the same address location from both ports at the same time, a write conflict happens. This results in unknown data being stored to that address location. There is no conflict resolution circuitry built into the Cyclone IV devices M9K memory blocks. You must handle address conflicts external to the RAM block.

Figure 3-11 shows true dual-port timing waveforms for the write operation at port A and read operation at port B. Registering the outputs of the RAM simply delays the q outputs by one clock cycle.

Figure 3-11. Cyclone IV Devices True Dual-Port Timing Waveform



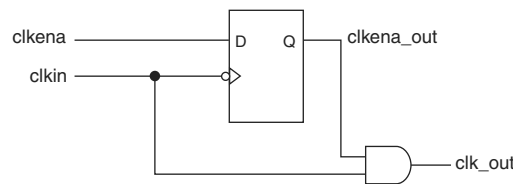
Shift Register Mode

Cyclone IV devices M9K memory blocks can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto-correlation and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flipflops that quickly exhaust many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources.

The size of a ($w \times m \times n$) shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n), and must be less than or equal to the maximum number of memory bits, which is 9,216 bits. In addition, the size of ($w \times n$) must be less than or equal to the maximum width of the block, which is 36 bits. If you need a larger shift register, you can cascade the M9K memory blocks.

Figure 5-7 shows how to implement the `clkena` signal with a single register.

Figure 5-7. `clkena` Implementation

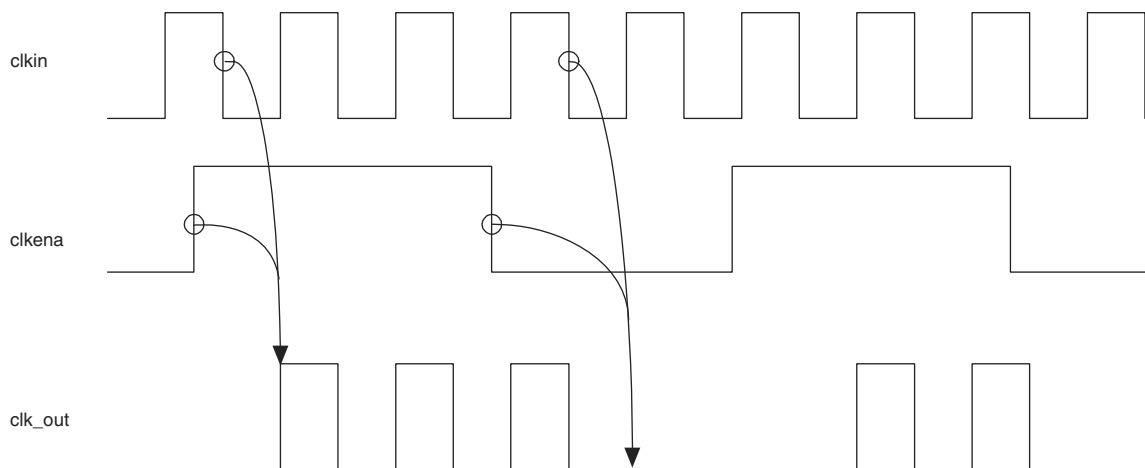


 The `clkena` circuitry controlling the output C0 of the PLL to an output pin is implemented with two registers instead of a single register, as shown in Figure 5-7.

Figure 5-8 shows the waveform example for a clock output enable. The `clkena` signal is sampled on the falling edge of the clock (`clk_in`).

 This feature is useful for applications that require low power or sleep mode.

Figure 5-8. `clkena` Implementation: Output Enable



The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during PLL resynchronization.

Altera recommends using the `clkena` signals when switching the clock source to the PLLs or the GCLK. The recommended sequence is:

1. Disable the primary output clock by de-asserting the `clkena` signal.
2. Switch to the secondary clock using the dynamic select signals of the clock control block.
3. Allow some clock cycles of the secondary clock to pass before reasserting the `clkena` signal. The exact number of clock cycles you must wait before enabling the secondary clock is design-dependent. You can build custom logic to ensure glitch-free transition when switching between different clock sources.

PLLs in Cyclone IV Devices

Cyclone IV GX devices offer two variations of PLLs: general purpose PLLs and multipurpose PLLs. Cyclone IV E devices only have the general purpose PLLs.

The general purpose PLLs are used for general-purpose applications in the FPGA fabric and periphery such as external memory interfaces. The multipurpose PLLs are used for clocking the transceiver blocks. When the multipurpose PLLs are not used for transceiver clocking, they can be used for general-purpose clocking.



For more details about the multipurpose PLLs used for transceiver clocking, refer to the *Cyclone IV Transceivers* chapter.

Cyclone IV GX devices contain up to eight general purpose PLLs and multipurpose PLLs while Cyclone IV E devices have up to four general purpose PLLs that provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces.



For more information about the number of general purpose PLLs and multipurpose PLLs in each device density, refer to the *Cyclone IV Device Family Overview* chapter.



The general I/O pins cannot drive the PLL clock input pins.

Table 5-5 lists the features available in Cyclone IV GX PLLs.

Table 5-5. Cyclone IV GX PLL Features (Part 1 of 2)

Features	Availability									
	General Purpose PLLs				Multipurpose PLLs					
	PLL_1 (1), (10)	PLL_2 (1), (10)	PLL_3 (2)	PLL_4 (3)	PLL_1 (4)	PLL_2 (4)	PLL_5 (1), (10)	PLL_6 (1), (10)	PLL_7 (1)	PLL_8 (1)
C (output counters)	5									
M, N, C counter sizes	1 to 512 ⁽⁵⁾									
Dedicated clock outputs	1 single-ended or 1 differential pair									
Clock input pins	12 single-ended or 6 differential pairs ⁽⁶⁾ and 4 differential pairs ⁽⁷⁾									
Spread-spectrum input clock tracking	✓ ⁽⁸⁾									
PLL cascading	Through GCLK									
Source-Synchronous Mode	✓	✓	✓	✓	✓	✓	✓	—	—	✓
No Compensation Mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Normal Mode	✓	✓	✓	✓	✓	✓	✓	—	—	✓
Zero Delay Buffer Mode	✓	✓	✓	✓	✓	✓	✓	—	—	✓
Deterministic Latency Compensation Mode	✓	✓	—	—	✓	✓	✓	✓	✓	✓
Phase shift resolution ⁽⁹⁾	Down to 96 ps increments									
Programmable duty cycle	✓									
Output counter cascading	✓									

Clock Feedback Modes

Cyclone IV PLLs support up to five different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. For the supported feedback modes, refer to Table 5-5 on page 5-18 for Cyclone IV GX PLLs and Table 5-6 on page 5-19 for Cyclone IV E PLLs.



Input and output delays are fully compensated by the PLL only if you are using the dedicated clock input pins associated with a given PLL as the clock sources.

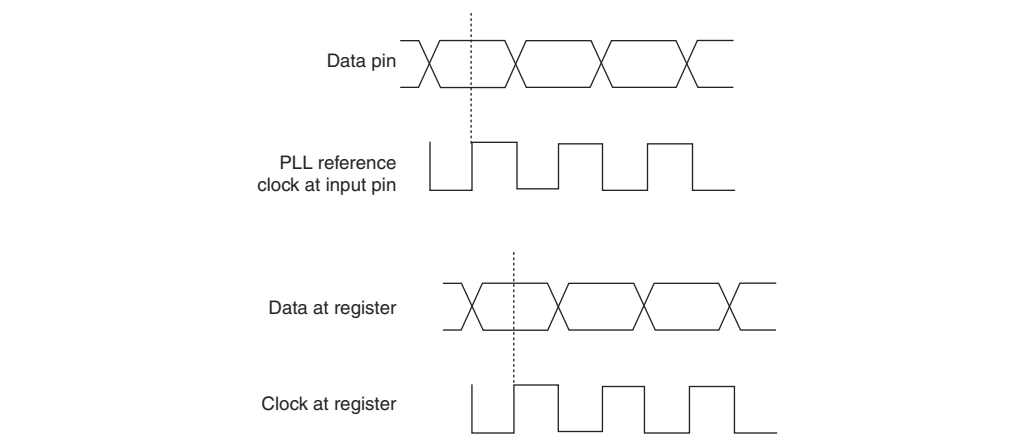
When driving the PLL using the GCLK network, the input and output delays may not be fully compensated in the Quartus II software.

Source-Synchronous Mode

If the data and clock arrive at the same time at the input pins, the phase relationship between the data and clock remains the same at the data and clock ports of any I/O element input register.

Figure 5-12 shows an example waveform of the data and clock in this mode. Use this mode for source-synchronous data transfers. Data and clock signals at the I/O element experience similar buffer delays as long as the same I/O standard is used.

Figure 5-12. Phase Relationship Between Data and Clock in Source-Synchronous Mode



Source-synchronous mode compensates for delay of the clock network used, including any difference in the delay between the following two paths:

- Data pin to I/O element register input
- Clock input pin to the PLL phase frequency detector (PFD) input



Set the input pin to the register delay chain in the I/O element to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL. Also, all data pins must use the **PLL COMPENSATED logic** option in the Quartus II software.

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figure 6-5 and Figure 6-6.

Figure 6-5. Cyclone IV Devices HSTL I/O Standard Termination

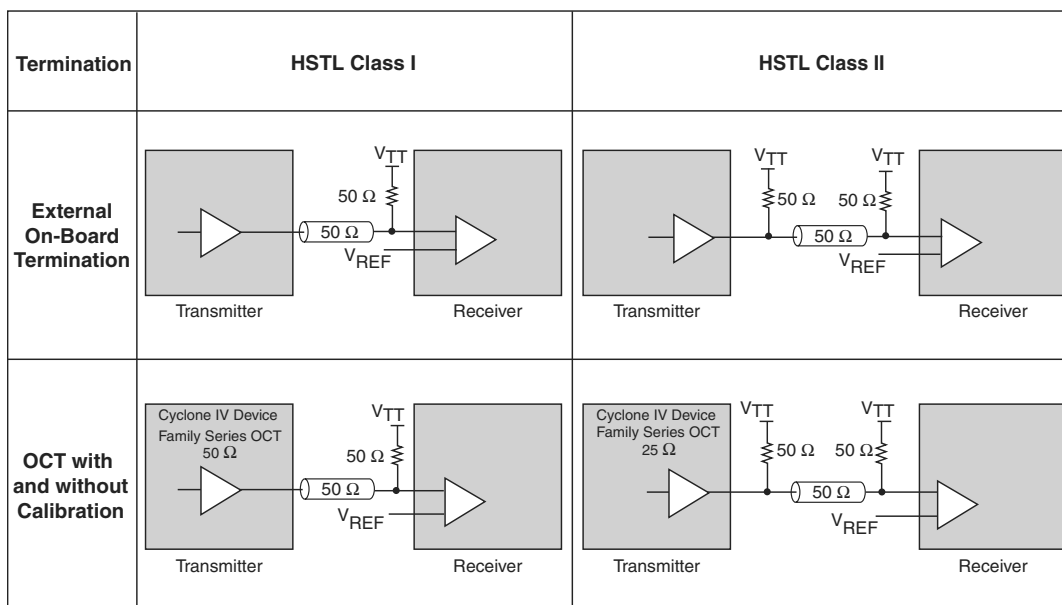


Figure 6-6. Cyclone IV Devices SSTL I/O Standard Termination

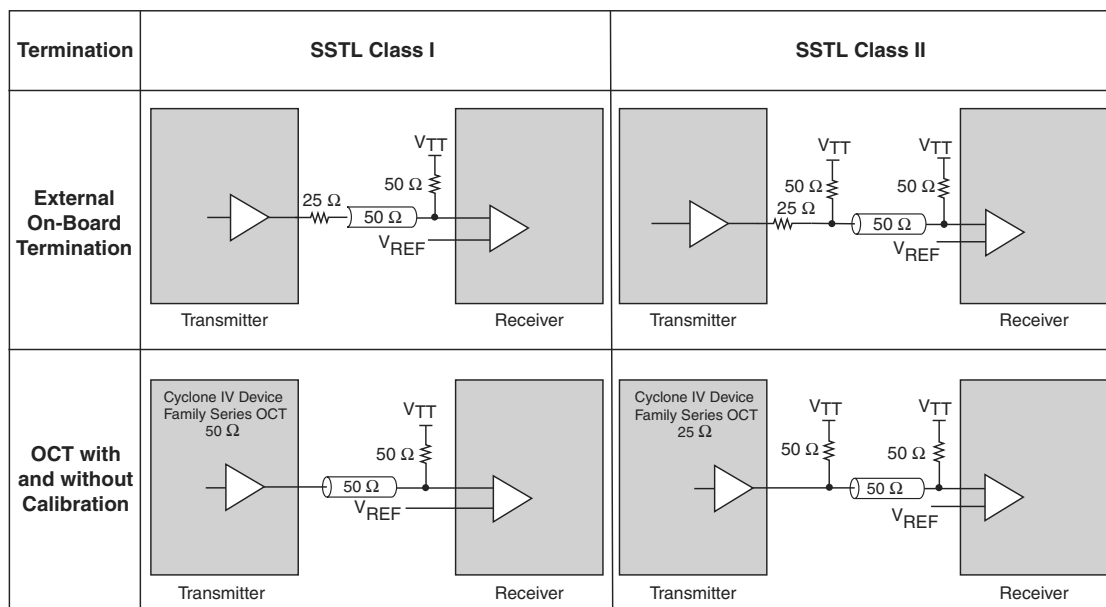
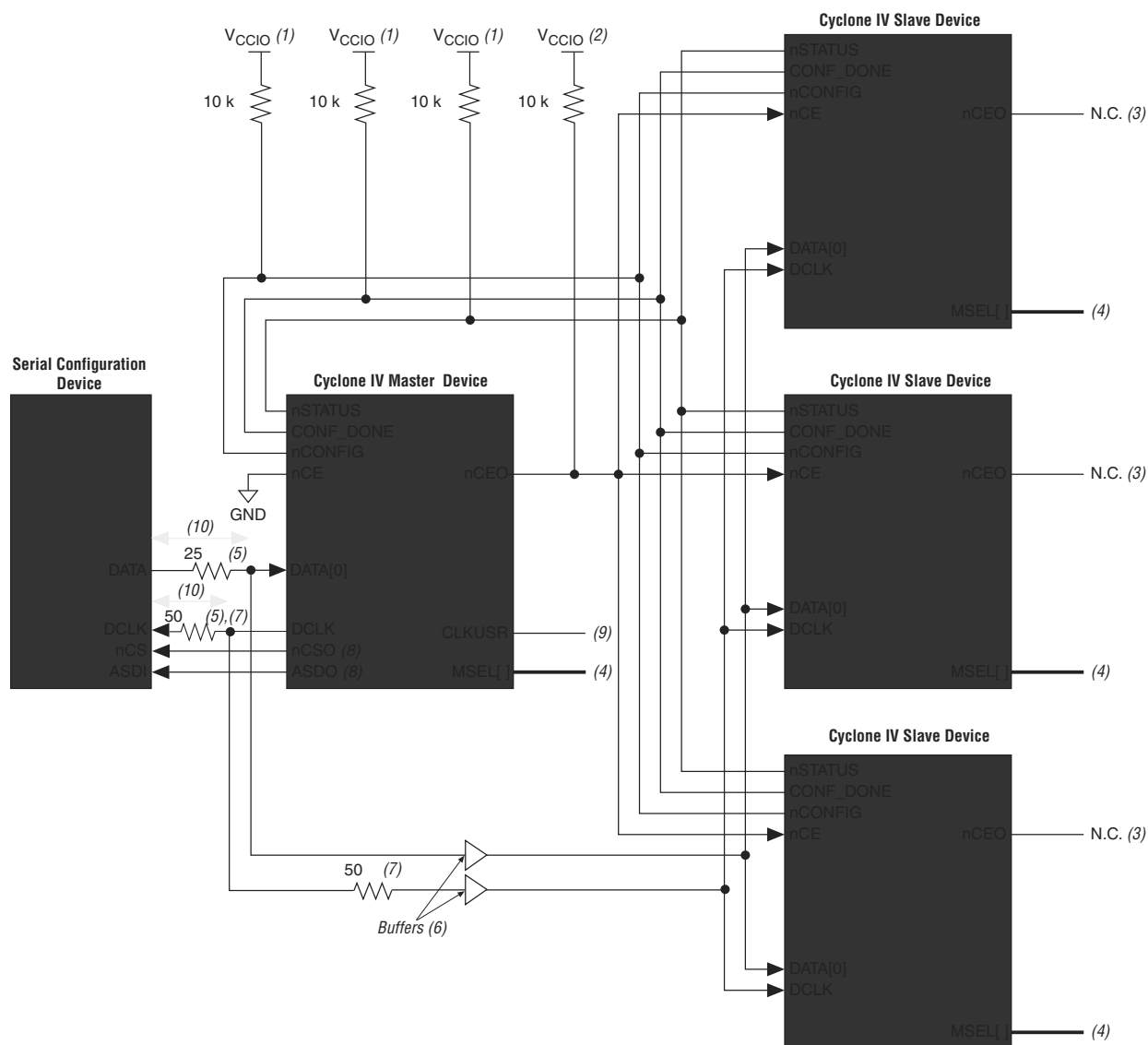


Figure 8-4. Multi-Device AS Configuration in Which Devices Receive the Same Data with Multiple .sof**Notes to Figure 8-4:**

- (1) Connect the pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the **nCE** pin resides.
- (3) The **nCEO** pin is left unconnected or used as a user I/O pin when it does not feed the **nCE** pin of another device.
- (4) The **MSEL** pin settings vary for different configuration voltage standards and POR time. You must set the master device in AS mode and the slave devices in PS mode. To connect the **MSEL** pins for the master device in AS mode and the slave devices in PS mode, refer to Table 8-3 on page 8-8, Table 8-4 on page 8-8, and Table 8-5 on page 8-9. Connect the **MSEL** pins directly to V_{CCA} or **GND**.
- (5) Connect the series resistor at the near end of the serial configuration device.
- (6) Connect the repeater buffers between the master and slave devices for **DATA[0]** and **DCLK**. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8-5.
- (7) The 50- Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50- Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.
- (8) These pins are dual-purpose I/O pins. The **nCSO** pin functions as **FLASH_nCE** pin in AP mode. The **ASDO** pin functions as **DATA[1]** pin in AP and FPP modes.
- (9) Only Cyclone IV GX devices have an option to select **CLKUSR** (40 MHz maximum) as the external clock source for **DCLK**.
- (10) For multi-devices AS configuration using Cyclone IV E with 1.0 V core voltage, the maximum board trace-length from the serial configuration device to the junction-split on both **DCLK** and **Data0** line is 3.5 inches.

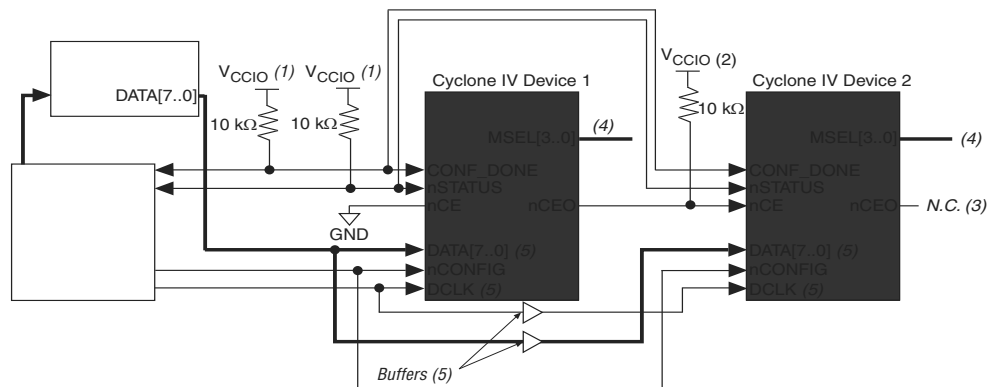
To ensure that DCLK and DATA[0] are not left floating at the end of the configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[0] pin is available as a user I/O pin after configuration. When you choose the FPP scheme in the Quartus II software, the DATA[0] pin is tri-stated by default in user mode and must be driven by the external host device. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box.

The DCLK speed must be below the specified system frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

The external host device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the external device to detect errors and to determine when programming is complete. If all configuration data is sent, but CONF_DONE or INIT_DONE has not gone high, the external device must reconfigure the target device.

Figure 8-20 shows how to configure multiple devices with a MAX II device. This circuit is similar to the FPP configuration circuit for a single device, except the Cyclone IV devices are cascaded for multi-device configuration.

Figure 8-20. Multi-Device FPP Configuration Using an External Host



Notes to Figure 8-20:

- (1) The pull-up resistor must be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.
- (2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.
- (3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8-4 on page 8-8 and Table 8-5 on page 8-9. Connect the MSEL pins directly to V_{CCA} or GND.
- (5) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[7..0] and DCLK must fit the maximum overshoot outlined in Equation 8-1 on page 8-5.

After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the nCE pin of the second device, which prompts the second device to begin configuration. The second device in the chain begins configuration in one clock cycle; therefore, the transfer of data destinations is transparent to the MAX II device. All other configuration pins (nCONFIG, nSTATUS,

Table 8–21 lists the optional configuration pins. If you do not enable these optional configuration pins in the Quartus II software, they are available as general-purpose user I/O pins. Therefore, during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Table 8–21. Optional Configuration Pins

Pin Name	User Mode	Pin Type	Description
CLKUSR	N/A if option is on. I/O if option is off.	Input	Optional user-supplied clock input synchronizes the initialization of one or more devices. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software. In AS configuration for Cyclone IV GX devices, you can use this pin as an external clock source to generate the <code>DCLK</code> by changing the clock source option in the Quartus II software in the Configuration tab of the Device and Pin Options dialog box.
INIT_DONE	N/A if option is on. I/O if option is off.	Output open-drain	Status pin is used to indicate when the device has initialized and is in user-mode. When <code>nCONFIG</code> is low, the <code>INIT_DONE</code> pin is tri-stated and pulled high due to an external 10-k Ω pull-up resistor during the beginning of configuration. After the option bit to enable <code>INIT_DONE</code> is programmed into the device (during the first frame of configuration data), the <code>INIT_DONE</code> pin goes low. When initialization is complete, the <code>INIT_DONE</code> pin is released and pulled high and the device enters user mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software. The functionality of this pin changes if the Enable OCT_DONE option is enabled in the Quartus II software. This option controls whether the <code>INIT_DONE</code> signal is gated by the <code>OCT_DONE</code> signal, which indicates the power-up on-chip termination (OCT) calibration is complete. If this option is turned off, the <code>INIT_DONE</code> signal is not gated by the <code>OCT_DONE</code> signal.
DEV_OE	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as programmed. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
DEV_CLRn	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. You can enable this pin by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.

Table 9–7 lists the input and output ports that you must include in the atom.

Table 9–7. CRC Block Input and Output Ports

Port	Input/Output	Definition
<i><crcblock_name></i>	Input	Unique identifier for the CRC block, and represents any identifier name that is legal for the given description language (for example, Verilog HDL, VHDL, and AHDL). This field is required.
.clk (<i><clock source></i>)	Input	This signal designates the clock input of this cell. All operations of this cell are with respect to the rising edge of the clock. Whether it is the loading of the data into the cell or data out of the cell, it always occurs on the rising edge. This port is required.
.shiftnld (<i><shiftnld source></i>)	Input	This signal is an input into the error detection block. If shiftnld =1, the data is shifted from the internal shift register to the regout at each rising edge of clk . If shiftnld =0, the shift register parallel loads either the pre-calculated CRC value or the update register contents, depending on the ldsrc port input. To do this, the shiftnld must be driven low for at least two clock cycles. This port is required.
.ldsrc (<i><ldsrc source></i>)	Input	This signal is an input into the error detection block. If ldsrc =0, the pre-computed CRC register is selected for loading into the 32-bit shift register at the rising edge of clk when shiftnld =0. If ldsrc =1, the signature register (result of the CRC calculation) is selected for loading into the shift register at the rising edge of clk when shiftnld =0. This port is ignored when shiftnld =1. This port is required.
.crcerror (<i><crcerror indicator output></i>)	Output	This signal is the output of the cell that is synchronized to the internal oscillator of the device (80-MHz internal oscillator) and not to the clk port. It asserts high if the error block detects that a SRAM bit has flipped and the internal CRC computation has shown a difference with respect to the pre-computed value. You must connect this signal either to an output pin or a bidirectional pin. If it is connected to an output pin, you can only monitor the CRC_ERROR pin (the core cannot access this output). If the CRC_ERROR signal is used by core logic to read error detection logic, you must connect this signal to a BIDIR pin. The signal is fed to the core indirectly by feeding a BIDIR pin that has its output enable port connected to V_{CC} (see Figure 9–3 on page 9–8).
.regout (<i><registered output></i>)	Output	This signal is the output of the error detection shift register synchronized to the clk port to be read by core logic. It shifts one bit at each cycle, so you should clock the clk signal 31 cycles to read out the 32 bits of the shift register.

Recovering from CRC Errors

The system that the Altera FPGA resides in must control device reconfiguration. After detecting an error on the **CRC_ERROR** pin, strobing the **nCONFIG** low directs the system to perform the reconfiguration at a time when it is safe for the system to reconfigure the FPGA.

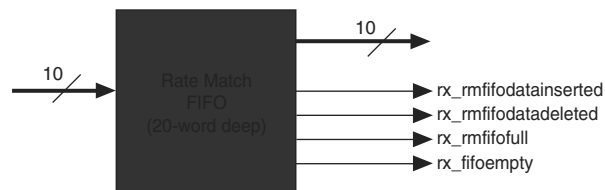
When the data bit is rewritten with the correct value by reconfiguring the device, the device functions correctly.

While soft errors are uncommon in Altera devices, certain high-reliability applications might require a design to account for these errors.

Rate Match FIFO

In asynchronous systems, the upstream transmitter and local receiver can be clocked with independent reference clocks. Frequency differences in the order of a few hundred ppm can corrupt the data when latching from the recovered clock domain (the same clock domain as the upstream transmitter reference clock) to the local receiver reference clock domain. Figure 1–21 shows the rate match FIFO block diagram.

Figure 1–21. Rate Match FIFO Block Diagram



The rate match FIFO compensates for small clock frequency differences of up to ± 300 ppm (600 ppm total) between the upstream transmitter and the local receiver clocks by performing the following functions:

- Insert skip symbols when the local receiver reference clock frequency is greater than the upstream transmitter reference clock frequency
- Delete skip symbols when the local receiver reference clock frequency is less than the upstream transmitter reference clock frequency

The 20-word deep rate match FIFO and logics control insertion and deletion of skip symbols, depending on the ppm difference. The operation begins after the word aligner synchronization status (`rx_syncstatus`) is asserted.



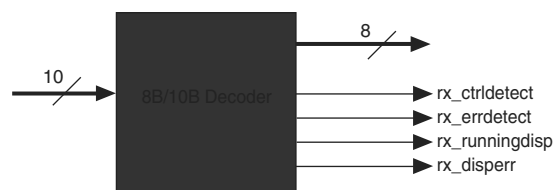
Rate match FIFO is only supported with 8B/10B encoded data and the word aligner in automatic synchronization state machine mode.

8B/10B Decoder

The 8B/10B decoder receives 10-bit data and decodes it into an 8-bit data and a 1-bit control identifier. The decoder is compliant with Clause 36 of the IEEE 802.3 specification.

Figure 1–22 shows the 8B/10B decoder block diagram.

Figure 1–22. 8B/10B Decoder Block Diagram



Bonded Channel Configuration

In bonded channel configuration, the low-speed clock for the bonded channels share a common bonded clock path that reduces clock skew between the bonded channels. The phase compensation FIFOs in bonded channels share a set of pointers and control logic that results in equal FIFO latency between the bonded channels. These features collectively result in lower channel-to-channel skew when implementing multi-channel serial interface in bonded channel configuration.

In a transceiver block, the high-speed clock for each bonded channels is distributed independently from one of the two multipurpose PLLs directly adjacent to the block. The low-speed clock for bonded channels is distributed from a common bonded clock path that selects from one of the two multipurpose PLLs directly adjacent to the block. Transceiver channels for devices in F484 and larger packages support additional clocking flexibility for $\times 2$ bonded channels. In these packages, the $\times 2$ bonded channels support high-speed and low-speed bonded clock distribution from PLLs beyond the two multipurpose PLLs directly adjacent to the block. Table 1–10 lists the high- and low-speed clock sources for the bonded channels.

Table 1–10. High- and Low-Speed Clock Sources for Bonded Channels in Bonded Channel Configuration

Package	Transceiver Block	Bonded Channels	High- and Low-Speed Clocks Source	
			Option 1	Option 2
F324 and smaller	GXBL0	$\times 2$ in channels 0, 1 $\times 4$ in all channels	MPLL_1	MPLL_2
F484 and larger	GXBL0	$\times 2$ in channels 0, 1	MPLL_5/ GPLL_1	MPLL_6
		$\times 4$ in all channels	MPLL_5	MPLL_6
	GXBL1 (1)	$\times 2$ in channels 0, 1	MPLL_7/ MPLL_6	MPLL_8
		$\times 4$ in all channels	MPLL_7	MPLL_8

Note to Table 1–10:

(1) GXBL1 is not available for transceivers in F484 package.



When implementing $\times 2$ bonded channel configuration in a transceiver block, remaining channels 2 and 3 are available to implement other non-bonded channel configuration.

Figure 1-45 and Figure 1-46 show the supported transceiver configurations in Basic mode with the 8-bit and 10-bit PMA-PCS interface width respectively.

Figure 1-45. Supported Transceiver Configurations in Basic Mode with the 8-bit PMA-PCS Interface Width

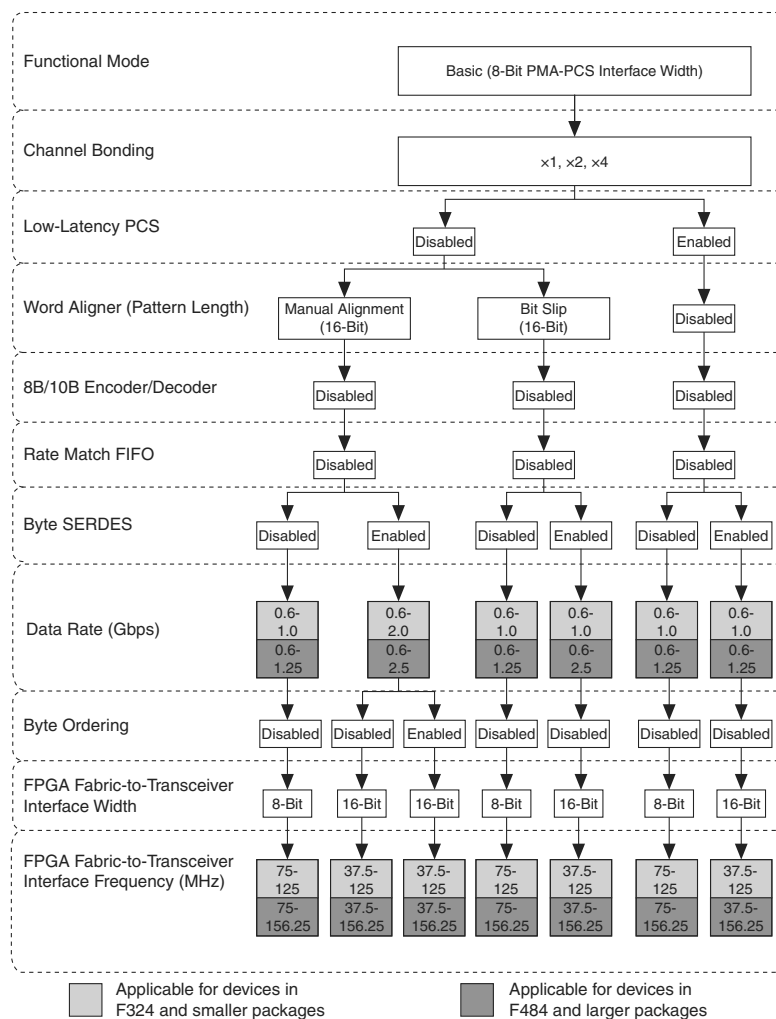


Figure 1–50 and Figure 1–51 show the detection mechanism example for a successful and unsuccessful receiver detection scenarios respectively. The tx_forcelecidle port must be asserted at least 10 parallel clock cycles prior to assertion of tx_detectrxloopback port to ensure the transmitter buffer is properly tri-stated. Detection completion is indicated by pipephydonestatus assertion, with detection successful indicated by 3'b011 on pipestatus[2..0] port, or detection unsuccessful by 3'b000 on pipestatus[2..0] port.

Figure 1–50. Example of Successful Receiver Detect Operation

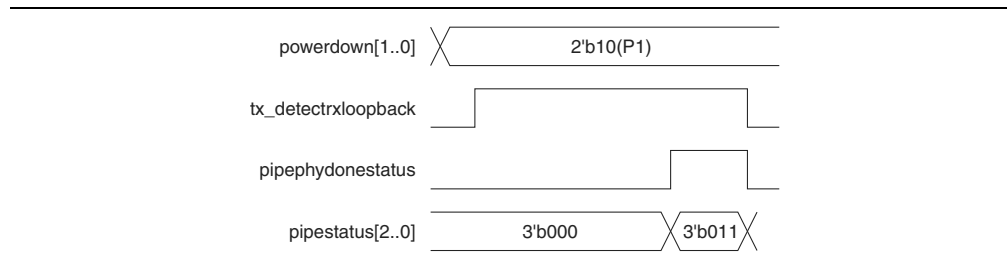
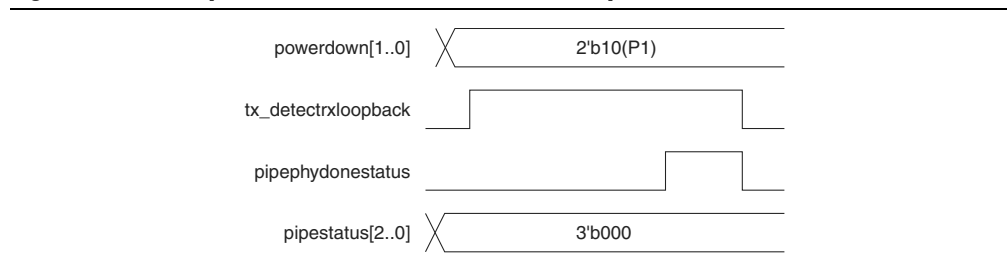


Figure 1–51. Example of Unsuccessful Receiver Detect Operation

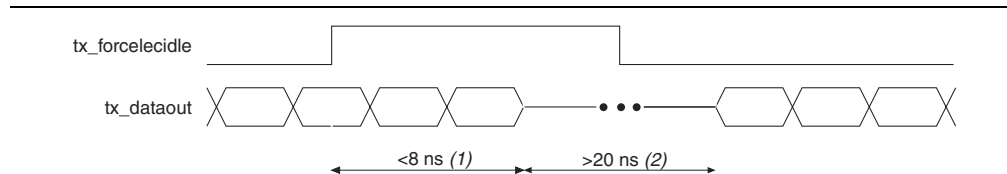


Electrical Idle Control

The Cyclone IV GX transceivers support transmitter buffer in electrical idle state using the tx_forcelecidle port. During electrical idle, the transmitter buffer differential and common mode output voltage levels are compliant to the PCIe Base Specification 2.0 for Gen1 signaling rate.

Figure 1–52 shows the relationship between assertion of the tx_forcelecidle port and the transmitter buffer output on the tx_dataout port.

Figure 1–52. Transmitter Buffer Electrical Idle State



Notes to Figure 1–52:

- (1) The protocol requires the transmitter buffer to transition to a valid electrical idle after sending an electrical idle ordered set within 8 ns.
- (2) The protocol requires transmitter buffer to stay in electrical idle for a minimum of 20 ns for Gen1 signaling rate.

Clock Rate Compensation

In XAUI mode, the rate match FIFO compensates up to ± 100 ppm (200 ppm total) difference between the upstream transmitter and the local receiver reference clock. The XAUI protocol requires the transmitter to send /R/ (/K28.0/) code groups simultaneously on all four lanes (denoted as ||R|| column) during inter-packet gaps, adhering to rules listed in the IEEE P802.3ae specification.

The rate match operation begins after rx_syncstatus and rx_channelaligned are asserted. The rx_syncstatus signal is from the word aligner, indicating that synchronization is acquired on all four channels, while rx_channelaligned signal is from the deskew FIFO, indicating channel alignment.

The rate match FIFO looks for the ||R|| column (simultaneous /R/ code groups on all four channels) and deletes or inserts ||R|| columns to prevent the rate match FIFO from overflowing or under running. The rate match FIFO can insert or delete as many ||R|| columns as necessary to perform the rate match operation.

The rx_rmfiodeleted and rx_rmfiodeinserted flags that indicate rate match FIFO deletion and insertion events, respectively, are forwarded to the FPGA fabric. If an ||R|| column is deleted, the rx_rmfiodeleted flag from each of the four channels goes high for one clock cycle per deleted ||R|| column. If an ||R|| column is inserted, the rx_rmfiodeinserted flag from each of the four channels goes high for one clock cycle per inserted ||R|| column.



The rate match FIFO does not insert or delete code groups automatically to overcome FIFO empty or full conditions. In this case, the rate match FIFO asserts the rx_rmfiodefull and rx_rmfiodeempty flags for at least three recovered clock cycles to indicate rate match FIFO full and empty conditions, respectively. You must then assert the rx_digitalreset signal to reset the receiver PCS blocks.

Deterministic Latency Mode

Deterministic Latency mode provides the transceiver configuration that allows no latency uncertainty in the datapath and features to strictly control latency variation. This mode supports non-bonded ($\times 1$) and bonded ($\times 4$) channel configurations, and is typically used to support CPRI and OBSAI protocols that require accurate delay measurements along the datapath. The Cyclone IV GX transceivers configured in Deterministic Latency mode provides the following features:

- registered mode phase compensation FIFO
- receive bit-slip indication
- transmit bit-slip control
- PLL PFD feedback

Table 3–4 describes the tx_datainfull[21..0] FPGA fabric-transceiver channel interface signals.

Table 3–4. tx_datainfull[21..0] FPGA Fabric-Transceiver Channel Interface Signal Descriptions ⁽¹⁾

FPGA Fabric-Transceiver Channel Interface Description	Transmit Signal Description (Based on Cyclone IV GX Supported FPGA Fabric-Transceiver Channel Interface Widths)
8-bit FPGA fabric-Transceiver Channel Interface	tx_datainfull[7:0]: 8-bit data (tx_datain)
	The following signals are used only in 8B/10B modes:
	tx_datainfull[8]: Control bit (tx_ctrlenable)
	tx_datainfull[9] Transmitter force disparity Compliance (PCI Express [PIPE]) (tx_forcedisp) in all modes except PCI Express (PIPE) functional mode. For PCI Express (PIPE) functional mode, (tx_forcedispcompliance) is used.
	- For non-PIPE: tx_datainfull[10]: Forced disparity value (tx_dispval) - For PCIe: tx_datainfull[10]: Forced electrical idle (tx_forceelectedle)
10-bit FPGA fabric-Transceiver Channel Interface	tx_datainfull[9:0]: 10-bit data (tx_datain)
16-bit FPGA fabric-Transceiver Channel Interface with PCS-PMA set to 8/10 bits	Two 8-bit Data (tx_datain) tx_datainfull[7:0] - tx_datain (LSByte) and tx_datainfull[18:11] - tx_datain (MSByte)
	The following signals are used only in 8B/10B modes:
	tx_datainfull[8] - tx_ctrlenable (LSB) and tx_datainfull[19] - tx_ctrlenable (MSB)
	Force Disparity Enable - For non-PIPE: tx_datainfull[9] - tx_forcedisp (LSB) and tx_datainfull[20] - tx_forcedisp (MSB) - For PCIe: tx_datainfull[9] - tx_forcedispcompliance and tx_datainfull[20] - 0
	Force Disparity Value - For non-PIPE: tx_datainfull[10] - tx_dispval (LSB) and tx_datainfull[21] - tx_dispval (MSB) - For PCIe: tx_datainfull[10] - tx_forceelectedle and tx_datainfull[21] - tx_forceelectedle
20-bit FPGA fabric-Transceiver Channel Interface with PCS-PMA set to 10 bits	Two 10-bit Data (tx_datain) tx_datainfull[9:0] - tx_datain (LSByte) and tx_datainfull[20:11] - tx_datain (MSByte)

Note to Table 3–4:

(1) For all transceiver-related ports, refer to the “Transceiver Port Lists” section in the *Cyclone IV GX Transceiver Architecture* chapter.

Table 1-4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA_GXB}	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
V_I	DC input voltage	—	-0.5	—	3.6	V
V_O	DC output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	-40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) ⁽⁷⁾	50 μ s	—	50 ms	—
		Fast POR ⁽⁸⁾	50 μ s	—	3 ms	—
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1-4:

- (1) All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.
- (2) You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.
- (3) Power supplies must rise monotonically.
- (4) V_{CCIO} for all I/O banks must be powered up during device operation. Configurations pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.
- (5) You must set V_{CC_CLKIN} to 2.5 V if you use $CLKIN$ as a high-speed serial interface (HSSI) $refclk$ or as a $DIFFCLK$ input.
- (6) The $CLKIN$ pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.
- (7) The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.
- (8) The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT} , V_{CCA} , and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1-5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1-5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V_{ESDHBM}	ESD voltage using the HBM (GPIOs) ⁽¹⁾	± 2000	V
	ESD using the HBM (HSSI I/Os) ⁽²⁾	± 1000	V
V_{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) ⁽²⁾	± 250	V

Notes to Table 1-5:

- (1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ± 1000 V.
- (2) This value is applicable only to Cyclone IV GX devices.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Parallel (AP) ⁽¹⁾	20 to 40	33	MHz
Active Serial (AS)	20 to 40	33	MHz

Note to Table 1–29:

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

Table 1–30. JTAG Timing Parameters for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	19	—	ns
t_{JCL}	TCK clock low time	19	—	ns
t_{JPSU_TDI}	JTAG port setup time for TDI	1	—	ns
t_{JPSU_TMS}	JTAG port setup time for TMS	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output ^{(2), (3)}	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output ^{(2), (3)}	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance ^{(2), (3)}	—	15	ns
t_{JSSU}	Capture register setup time	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 1–30:

- (1) For more information about JTAG waveforms, refer to “JTAG Waveform” in “Glossary” on page 1–37.
- (2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.
- (3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.