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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 3491 |
| Number of Logic Elements/Cells | 55856 |
| Total RAM Bits | 2396160 |
| Number of I/O | 324 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep4ce55f23i7 |

# Cyclone IV Device Family Speed Grades

Table 1–5 lists the Cyclone IV GX devices speed grades.

**Table 1–5. Speed Grades for the Cyclone IV GX Device Family**

| Device | F169 | F324 | F484 | F672 | F896 |
|---|---|---|---|---|---|
| EP4CGX15 | C6, C7, C8, I7 | — | — | — | — |
| EP4CGX22 | C6, C7, C8, I7 | C6, C7, C8, I7 | — | — | — |
| EP4CGX30 | C6, C7, C8, I7 | C6, C7, C8, I7 | C6, C7, C8, I7 | — | — |
| EP4CGX50 | — | — | C6, C7, C8, I7 | C6, C7, C8, I7 | — |
| EP4CGX75 | — | — | C6, C7, C8, I7 | C6, C7, C8, I7 | — |
| EP4CGX110 | — | — | C7, C8, I7 | C7, C8, I7 | C7, C8, I7 |
| EP4CGX150 | — | — | C7, C8, I7 | C7, C8, I7 | C7, C8, I7 |

Table 1–6 lists the Cyclone IV E devices speed grades.

**Table 1–6. Speed Grades for the Cyclone IV E Device Family** *(1), (2)*

| Device | E144 | M164 | M256 | U256 | F256 | F324 | U484 | F484 | F780 |
|---|---|---|---|---|---|---|---|---|---|
| EP4CE6 | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | — | — |
| EP4CE10 | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | — | — |
| EP4CE15 | C8L, C9L, I8L C6, C7, C8, I7 | I7N | C7N, I7N | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | C8L, C9L, I8L C6, C7, C8, I7, A7 | — |
| EP4CE22 | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | — | — | — | — |
| EP4CE30 | — | — | — | — | — | A7N | — | C8L, C9L, I8L C6, C7, C8, I7, A7 | C8L, C9L, I8L C6, C7, C8, I7 |
| EP4CE40 | — | — | — | — | — | A7N | I7N | C8L, C9L, I8L C6, C7, C8, I7, A7 | C8L, C9L, I8L C6, C7, C8, I7 |
| EP4CE55 | — | — | — | — | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7 | C8L, C9L, I8L C6, C7, C8, I7 |
| EP4CE75 | — | — | — | — | — | — | I7N | C8L, C9L, I8L C6, C7, C8, I7 | C8L, C9L, I8L C6, C7, C8, I7 |
| EP4CE115 | — | — | — | — | — | — | — | C8L, C9L, I8L C7, C8, I7 | C8L, C9L, I8L C7, C8, I7 |

**Notes to Table 1–6:**

(1) C8L, C9L, and I8L speed grades are applicable for the 1.0-V core voltage.

(2) C6, C7, C8, I7, and A7 speed grades are applicable for the 1.2-V core voltage.

For more information, refer to the *External Memory Interfaces in Cyclone IV Devices* chapter.

## Configuration

Cyclone IV devices use SRAM cells to store configuration data. Configuration data is downloaded to the Cyclone IV device each time the device powers up. Low-cost configuration options include the Altera EPCS family serial flash devices and commodity parallel flash configuration options. These options provide the flexibility for general-purpose applications and the ability to meet specific configuration and wake-up time requirements of the applications.

Table 1–9 lists which configuration schemes are supported by Cyclone IV devices.

**Table 1–9. Configuration Schemes for Cyclone IV Device Family**

| Devices | Supported Configuration Scheme |
|---|---|
| Cyclone IV GX | AS, PS, JTAG, and FPP *(1)* |
| Cyclone IV E | AS, AP, PS, FPP, and JTAG |

**Note to Table 1–9:**

(1) The FPP configuration scheme is only supported by the EP4CGX30F484 and EP4CGX50/75/110/150 devices.

IEEE 1149.6 (AC JTAG) is supported on all transceiver I/O pins. All other pins support IEEE 1149.1 (JTAG) for boundary scan testing.

For more information, refer to the *JTAG Boundary-Scan Testing for Cyclone IV Devices* chapter.

For Cyclone IV GX devices to meet the PCIe 100 ms wake-up time requirement, you must use passive serial (PS) configuration mode for the EP4CGX15/22/30 devices and use fast passive parallel (FPP) configuration mode for the EP4CGX30F484 and EP4CGX50/75/110/150 devices.

For more information, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.

The cyclical redundancy check (CRC) error detection feature during user mode is supported in all Cyclone IV GX devices. For Cyclone IV E devices, this feature is only supported for the devices with the core voltage of 1.2 V.

For more information about CRC error detection, refer to the *SEU Mitigation in Cyclone IV Devices* chapter.

## High-Speed Transceivers (Cyclone IV GX Devices Only)

Cyclone IV GX devices contain up to eight full duplex high-speed transceivers that can operate independently. These blocks support multiple industry-standard communication protocols, as well as Basic mode, which you can use to implement your own proprietary protocols. Each transceiver channel has its own pre-emphasis and equalization circuitry, which you can set at compile time to optimize signal integrity and reduce bit error rates. Transceiver blocks also support dynamic reconfiguration, allowing you to change data rates and protocols on-the-fly.

**Table 5–2. GCLK Network Connections for EP4CGX30, EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 Devices (1), (2) (Part 1 of 4)**

| GCLK Network Clock Sources | GCLK Networks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 |
| CLKIO4/DIFFCLK_2n | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | — | ✓ | — | — | — | — | — | — | — | — | — | — | — | — | — |
| CLKIO5/DIFFCLK_2p | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | ✓ | — | — | ✓ | — | — | — | — | — | — | — | — | — | — | — | — |
| CLKIO6/DIFFCLK_3n | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | ✓ | — | — | — | — | — | — | — | — | — | — | — | — | — |
| CLKIO7/DIFFCLK_3p | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | — | ✓ | — | ✓ | — | — | — | — | — | — | — | — | — | — | — | — |
| CLKIO8/DIFFCLK_5n | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | — | ✓ | — | — | — | — | — | — | — |
| CLKIO9/DIFFCLK_5p | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | ✓ | — | — | ✓ | — | — | — | — | — | — |
| CLKIO10/DIFFCLK_4n/REFCLK3n | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | ✓ | | — | — | — | — | — | — |
| CLKIO11/DIFFCLK_4p/REFCLK3p | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | — | ✓ | — | ✓ | — | — | — | — | — | — |
| CLKIO12/DIFFCLK_7p/REFCLK2p | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | — | ✓ | — |
| CLKIO13/DIFFCLK_7n/REFCLK2n | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | ✓ | — | — | ✓ |
| CLKIO14/DIFFCLK_6p | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | ✓ | — |
| CLKIO15/DIFFCLK_6n | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | — | ✓ | — | ✓ |
| PLL_1_C0 | ✓ | — | — | ✓ | — | ✓ | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | — | ✓ | — | ✓ |
| PLL_1_C1 | — | ✓ | — | — | ✓ | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | — | ✓ | — |
| PLL_1_C2 | ✓ | — | ✓ | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | — | — | — |
| PLL_1_C3 | — | ✓ | — | ✓ | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | — | — |
| PLL_1_C4 | — | — | ✓ | — | ✓ | ✓ | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | ✓ |
| PLL_2_C0 | — | — | — | — | — | — | ✓ | — | — | ✓ | — | ✓ | — | — | — | — | — | — | ✓ | — | — | ✓ | — | ✓ | — | — | — | — | — | — |
| PLL_2_C1 | — | — | — | — | — | — | — | ✓ | — | — | ✓ | — | — | — | — | — | — | — | — | ✓ | — | — | ✓ | — | — | — | — | — | — | — |
| PLL_2_C2 | — | — | — | — | — | — | ✓ | — | ✓ | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | — | — | — | — | — | — | — | — | — |
| PLL_2_C3 | — | — | — | — | — | — | — | ✓ | — | ✓ | — | — | — | — | — | — | — | — | — | ✓ | — | ✓ | — | — | — | — | — | — | — | — |
| PLL_2_C4 | — | — | — | — | — | — | — | — | ✓ | — | ✓ | ✓ | — | — | — | — | — | — | — | — | ✓ | — | ✓ | ✓ | — | — | — | — | — | — |

Table 6–2 on page 6–7 shows the possible settings for I/O standards with current strength control. These programmable current strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for IOH and IOL of the corresponding I/O standard.

☞ When you use programmable current strength, on-chip series termination ($R_S$ OCT) is not available.

## Slew Rate Control

The output buffer for each Cyclone IV I/O pin provides optional programmable output slew-rate control. Table 6–2 on page 6–7 shows the possible slew rate option and the Quartus II default slew rate setting. However, these fast transitions may introduce noise transients in the system. A slower slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Because each I/O pin has an individual slew-rate control, you can specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges. Slew rate control is available for single-ended I/O standards with current strength of 8 mA or higher.

☞ You cannot use the programmable slew rate feature when using OCT with calibration.

☞ You cannot use the programmable slew rate feature when using the 3.0-V PCI, 3.0-V PCI-X, 3.3-V LVTTL, or 3.3-V LVCMOS I/O standards. Only the fast slew rate (default) setting is available.

## Open-Drain Output

Cyclone IV devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that are asserted by multiple devices in your system.

## Bus Hold

Each Cyclone IV device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry holds the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage in which noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than $V_{CCIO}$ to prevent overdriving signals.

☞ If you enable the bus-hold feature, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus-hold circuitry is not available on dedicated clock pins.

Bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

# I/O Banks

I/O pins on Cyclone IV devices are grouped together into I/O banks. Each bank has a separate power bus.

Cyclone IV E devices have eight I/O banks, as shown in Figure 6–9. Each device I/O pin is associated with one I/O bank. All single-ended I/O standards are supported in all banks except HSTL-12 Class II, which is only supported in column I/O banks. All differential I/O standards are supported in all banks. The only exception is HSTL-12 Class II, which is only supported in column I/O banks.

Cyclone IV GX devices have up to ten I/O banks and two configuration banks, as shown in Figure 6–10 on page 6–18 and Figure 6–11 on page 6–19. The Cyclone IV GX configuration I/O bank contains three user I/O pins that can be used as normal user I/O pins if they are not used in configuration modes. Each device I/O pin is associated with one I/O bank. All single-ended I/O standards are supported except HSTL-12 Class II, which is only supported in column I/O banks. All differential I/O standards are supported in top, bottom, and right I/O banks. The only exception is HSTL-12 Class II, which is only supported in column I/O banks.

The entire left side of the Cyclone IV GX devices contain dedicated high-speed transceiver blocks for high speed serial interface applications. There are a total of 2, 4, and 8 transceiver channels for Cyclone IV GX devices, depending on the density and package of the device. For more information about the transceiver channels supported, refer to Figure 6–10 on page 6–18 and Figure 6–11 on page 6–19.

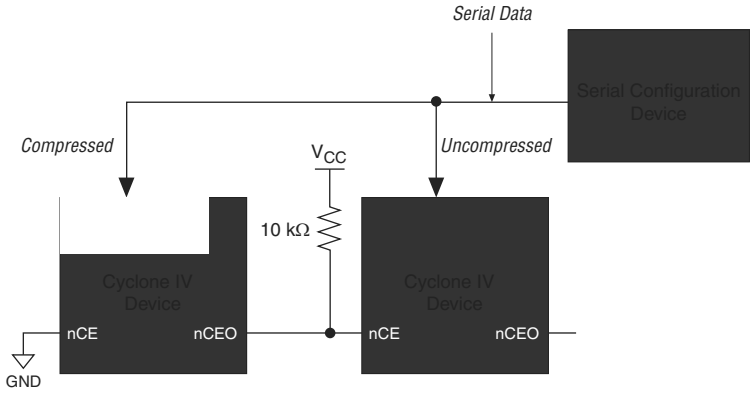
3. Click the **Configuration** tab.
4. Turn on **Generate compressed bitstreams**.
5. Click **OK**.
6. In the **Settings** dialog box, click **OK**.

You can enable compression when creating programming files from the **Convert Programming Files** dialog box. To enable compression, perform the following steps:

1. On the File menu, click **Convert Programming Files**.
2. Under **Output programming file**, select your desired file type from the **Programming file type** list.
3. If you select **Programmer Object File (.pof)**, you must specify the configuration device in the **Configuration device** list.
4. Under **Input files to convert**, select **SOF Data**.
5. Click **Add File** to browse to the Cyclone IV device SRAM object files (**.sof)**.
6. In the **Convert Programming Files** dialog box, select the **.pof** you added to **SOF Data** and click **Properties**.
7. In the **SOF File Properties** dialog box, turn on the **Compression** option.

When multiple Cyclone IV devices are cascaded, you can selectively enable the compression feature for each device in the chain. Figure 8–1 shows a chain of two Cyclone IV devices. The first device has compression enabled and receives compressed bitstream from the configuration device. The second device has the compression feature disabled and receives uncompressed data. You can generate programming files for this setup in the **Convert Programming Files** dialog box.

**Figure 8–1. Compressed and Uncompressed Configuration Data in the Same Configuration File**




## Configuration Requirement

This section describes Cyclone IV device configuration requirement and includes the following topics:

- "Power-On Reset (POR) Circuit" on page 8–4
- "Configuration File Size" on page 8–4
- "Power Up" on page 8–6

**Table 8–2. Uncompressed Raw Binary File (.rbf) Sizes for Cyclone IV Devices (Part 2 of 2)**

| Device | | Data Size (bits) |
|---|---|---|
| Cyclone IV GX | EP4CGX15 | 3,805,568 |
| | EP4CGX22 | 7,600,040 |
| | EP4CGX30 | 7,600,040 |
| | | 22,010,888 (1) |
| | EP4CGX50 | 22,010,888 |
| | EP4CGX75 | 22,010,888 |
| | EP4CGX110 | 39,425,016 |
| | EP4CGX150 | 39,425,016 |

**Note to Table 8–2:**

(1) Only for the F484 package.

Use the data in Table 8–2 to estimate the file size before design compilation. Different configuration file formats, such as Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) formats, have different file sizes. However, for any specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you use compression, the file size varies after each compilation, because the compression ratio depends on the design.

For more information about setting device configuration options or creating configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook*.

## Configuration and JTAG Pin I/O Requirements

Cyclone IV devices are manufactured using the TSMC 60-nm low-k dielectric process. Although Cyclone IV devices use TSMC 2.5-V transistor technology in the I/O buffers, the devices are compatible and able to interface with 2.5, 3.0, and 3.3-V configuration voltage standards by following specific requirements.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. When using a serial configuration device in an AS configuration scheme, you must connect a 25-Ω series resistor for the DATA[0] pin. When cascading the Cyclone IV device family in a multi-device configuration for AS, AP, FPP, and PS configuration schemes, you must connect the repeater buffers between the master and slave devices for the DATA and DCLK pins. When using the JTAG configuration scheme in a multi-device configuration, connect 25-Ω resistors on both ends of the TDO-TDI path if the TDO output driver is a non-Cyclone IV device.

The output resistance of the repeater buffers and the TDO path for all cases must fit the maximum overshoot equation shown in Equation 8–1.

**Equation 8–1. (1)**

$$0.8Z_O \leq R_E \leq 1.8Z_O$$

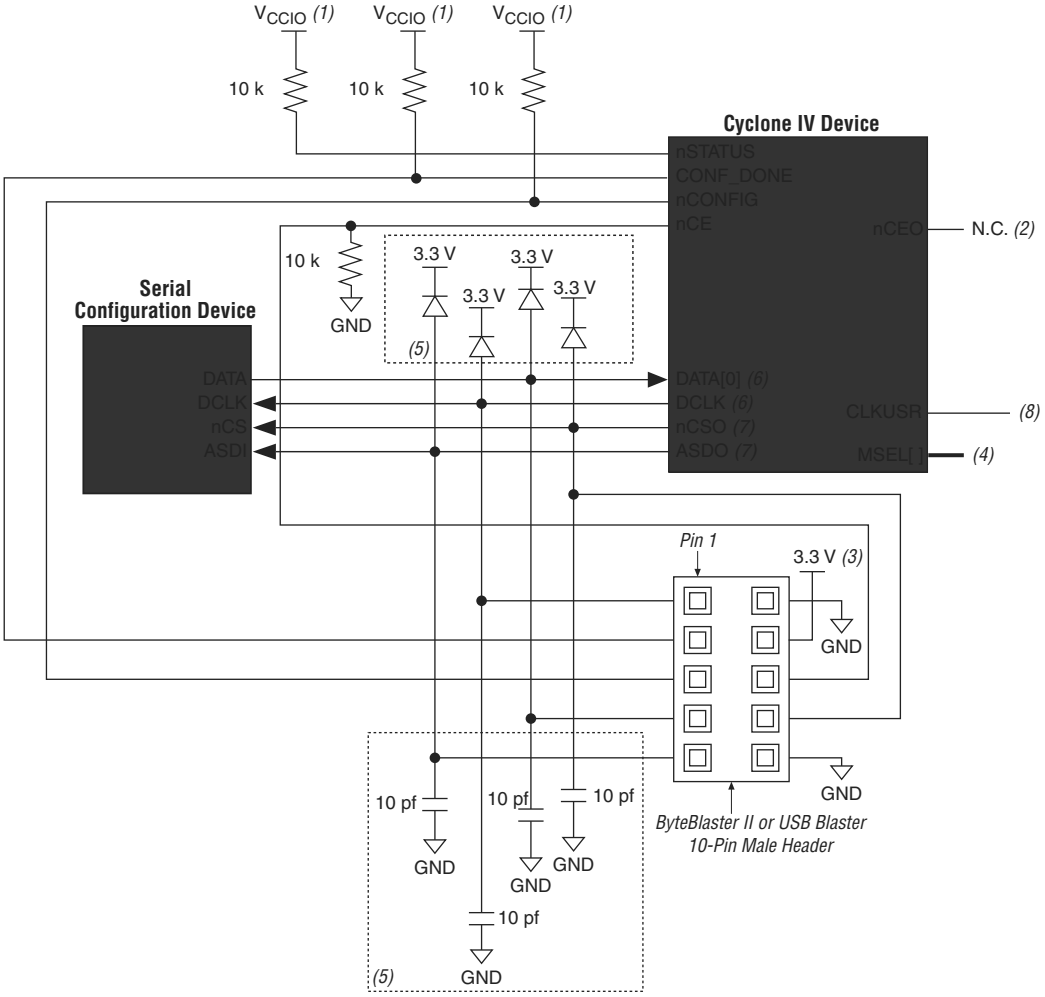
**Note to Equation 8–1:**

(1) $Z_O$ is the transmission line impedance and $R_E$ is the equivalent resistance of the output buffer.

For more information about the USB-Blaster download cable, refer to the *USB-Blaster Download Cable User Guide*. For more information about the ByteBlaster II download cable, refer to the *ByteBlaster II Download Cable User Guide*.

Figure 8–6 shows the download cable connections to the serial configuration device.

**Figure 8–6. In-System Programming of Serial Configuration Devices**




**Notes to Figure 8–6:**

(1) Connect these pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(3) Power up the $V_{CC}$ of the ByteBlaster II or USB-Blaster download cable with the 3.3-V supply.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(5) The diodes and capacitors must be placed as close as possible to the Cyclone IV device. You must ensure that the diodes and capacitors maintain a maximum AC voltage of 4.1 V. The external diodes and capacitors are required to prevent damage to the Cyclone IV device AS configuration input pins due to possible overshoot when programming the serial configuration device with a download cable. Altera recommends using the Schottky diode, which has a relatively lower forward diode voltage (VF) than the switching and Zener diodes, for effective voltage clamping.

(6) When cascading Cyclone IV devices in a multi-device AS configuration, connect the repeater buffers between the master and slave devices for DATA[0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8–5.

(7) These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as DATA[1] pin in AP and FPP modes.

(8) Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK.

# Cyclone IV Device Handbook,

# Volume 2

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CYIV-5V2-1.9

# Section I. Transceivers

This section provides a complete overview of all features relating to the Cyclone® IV device transceivers. This section includes the following chapters:

- Chapter 1, Cyclone IV Transceivers Architecture
- Chapter 2, Cyclone IV Reset Control and Power Down
- Chapter 3, Cyclone IV Dynamic Reconfiguration

## Revision History

Refer to the chapter for its own specific revision history. For information about when the chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

- Programmable equalization—boosts the high-frequency gain of the incoming signal up to 7 dB. This compensates for the low-pass filter effects of the transmission media. The amount of high-frequency gain required depends on the loss characteristics of the physical medium.
- Programmable DC gain—provides equal boost to incoming signal across the frequency spectrum with DC gain settings up to 6 dB.
- Programmable differential OCT—provides calibrated OCT at 100 Ω or 150 Ω with on-chip receiver common mode voltage at 0.82 V. The common mode voltage is tri-stated when you disable the OCT to use external termination.
- Offset cancellation—corrects the analog offset voltages that might exist from process variations between the positive and negative differential signals in the equalizer stage and CDR circuit.
- Signal detection—detects if the signal level present at the receiver input buffer is higher than the threshold with a built-in signal threshold detection circuitry. The circuitry has a hysteresis response that filters out any high-frequency ringing caused by ISI effects or high-frequency losses in the transmission medium. Detection is indicated by the assertion of the `rx_signaldetect` signal. Signal detection is only supported when 8B/10B encoder/decoder block is enabled. When not supported, the `rx_signaldetect` signal is forced high, bypassing the signal detection function.

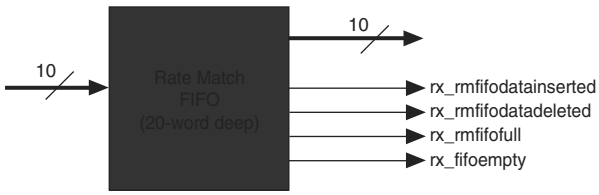
Disable OCT to use external termination if the link requires a 85 Ω termination, such as when you are interfacing with certain PCIe Gen1 or Gen2 capable devices.

For specifications on programmable equalization and DC gain settings, refer to the *Cyclone IV Device Data Sheet*.

## Rate Match FIFO

In asynchronous systems, the upstream transmitter and local receiver can be clocked with independent reference clocks. Frequency differences in the order of a few hundred ppm can corrupt the data when latching from the recovered clock domain (the same clock domain as the upstream transmitter reference clock) to the local receiver reference clock domain. Figure 1–21 shows the rate match FIFO block diagram.

**Figure 1–21. Rate Match FIFO Block Diagram**




The rate match FIFO compensates for small clock frequency differences of up to ±300 ppm (600 ppm total) between the upstream transmitter and the local receiver clocks by performing the following functions:

- Insert skip symbols when the local receiver reference clock frequency is greater than the upstream transmitter reference clock frequency
- Delete skip symbols when the local receiver reference clock frequency is less than the upstream transmitter reference clock frequency

The 20-word deep rate match FIFO and logics control insertion and deletion of skip symbols, depending on the ppm difference. The operation begins after the word aligner synchronization status (`rx_syncstatus`) is asserted.

Rate match FIFO is only supported with 8B/10B encoded data and the word aligner in automatic synchronization state machine mode.

## 8B/10B Decoder

The 8B/10B decoder receives 10-bit data and decodes it into an 8-bit data and a 1-bit control identifier. The decoder is compliant with Clause 36 of the IEEE 802.3 specification.

Figure 1–22 shows the 8B/10B decoder block diagram.

**Figure 1–22. 8B/10B Decoder Block Diagram**

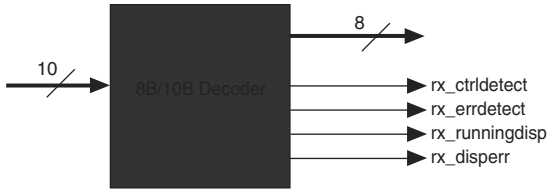
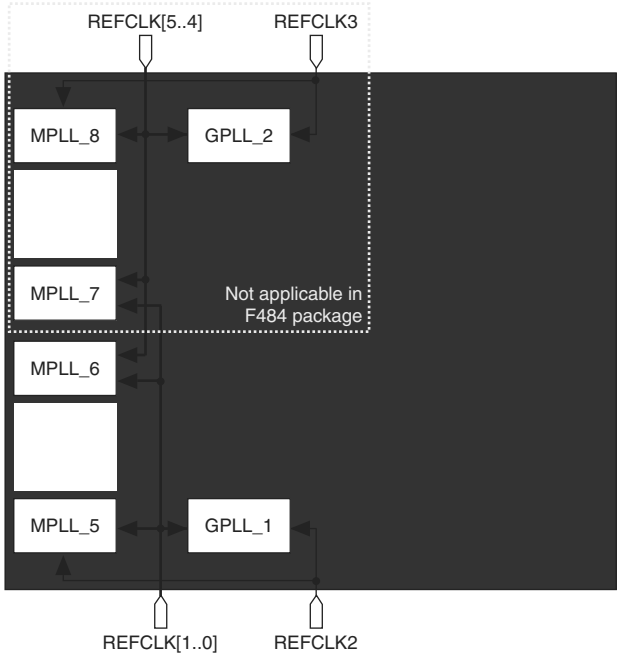


**Figure 1–26. PLL Input Reference Clocks in Transceiver Operation for F484 and Larger Packages (1), (2), (3)**




**Notes to Figure 1–26:**

(1) The REFCLK2 and REFCLK3 pins are dual-purpose CLKIO, REFCLK, or DIFFCLK pins that reside in banks 3A and 8A respectively.

(2) The REFCLK[1..0] and REFCLK[5..4] pins are dual-purpose differential REFCLK or DIFFCLK pins that reside in banks 3B and 8B respectively. These clock input pins do not have access to the clock control blocks and GCLK networks. For more details, refer to the *Clock Networks and PLLs in Cyclone IV Devices* chapter.

(3) Using any clock input pins other than the designated REFCLK pins as shown here to drive the MPLLs and GPLLs may have reduced jitter performance.

The input reference clocks reside in banks 3A, 3B, 8A, and 8B have dedicated $V_{CC\_CLKIN3A}$, $V_{CC\_CLKIN3B}$, $V_{CC\_CLKIN8A}$, and $V_{CC\_CLKIN8B}$ power supplies separately in their respective I/O banks to avoid the different power level requirements in the same bank for general purpose I/Os (GPIOs). Table 1–6 lists the supported I/O standard for the REFCLK pins.

**Table 1–6. REFCLK I/O Standard Support**

| I/O Standard | HSSI Protocol | Coupling | Termination | VCC_CLKIN Level | | I/O Pin Type | | |
|---|---|---|---|---|---|---|---|---|
| | | | | Input | Output | Column I/O | Row I/O | Supported Banks |
| **LVDS** | ALL | Differential AC (Needs off-chip resistor to restore $V_{CM}$) | Off-chip | 2.5 V | Not Supported | Yes | No | 3A, 3B, 8A, 8B |
| **LVPECL** | ALL | | Off-chip | 2.5 V | Not Supported | Yes | No | 3A, 3B, 8A, 8B |
| **1.2 V, 1.5 V, 3.3 V PCML** | ALL | | Off-chip | 2.5 V | Not Supported | Yes | No | 3A, 3B, 8A, 8B |
| | ALL | | Off-chip | 2.5 V | Not Supported | Yes | No | 3A, 3B, 8A, 8B |
| | ALL | | Off-chip | 2.5 V | Not Supported | Yes | No | 3A, 3B, 8A, 8B |
| **HCSL** | PCIe | Differential DC | Off-chip | 2.5 V | Not Supported | Yes | No | 3A, 3B, 8A, 8B |

Figure 1–35 shows the datapath clocking in the transmitter and receiver operation mode with the rate match FIFO. The receiver datapath clocking in configuration without the rate match FIFO is identical to Figure 1–34.

In configuration with the rate match FIFO, the CDR unit in the receiver channel recovers the clock from received serial data and generates the high-speed recovered clock for the deserializer, and low-speed recovered clock for forwarding to the receiver PCS. The low-speed recovered clock feeds to the following blocks in the receiver PCS:

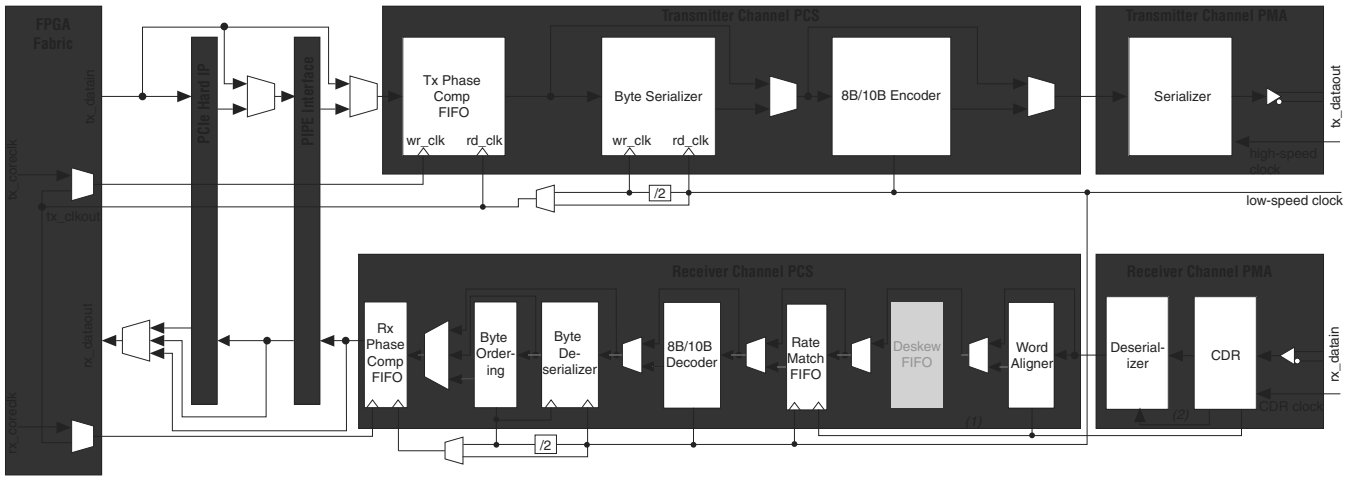
- word aligner
- write clock of rate match FIFO

The low-speed clock that is used in the transmitter PCS datapath feeds the following blocks in the receiver PCS:

- read clock of rate match FIFO
- 8B/10B decoder
- write clock of byte deserializer
- byte ordering
- write clock of RX phase compensation FIFO

When the byte deserializer is enabled, the low-speed clock frequency is halved before feeding into the write clock of RX phase compensation FIFO. The low-speed clock is available in the FPGA fabric as `tx_clkout` port, which can be used in the FPGA fabric to send transmitter data and control signals, and capture receiver data and status signals.

**Figure 1–35. Transmitter and Receiver Datapath Clocking with Rate Match FIFO in Non-Bonded Channel Configuration**




**Notes to Figure 1–35:**

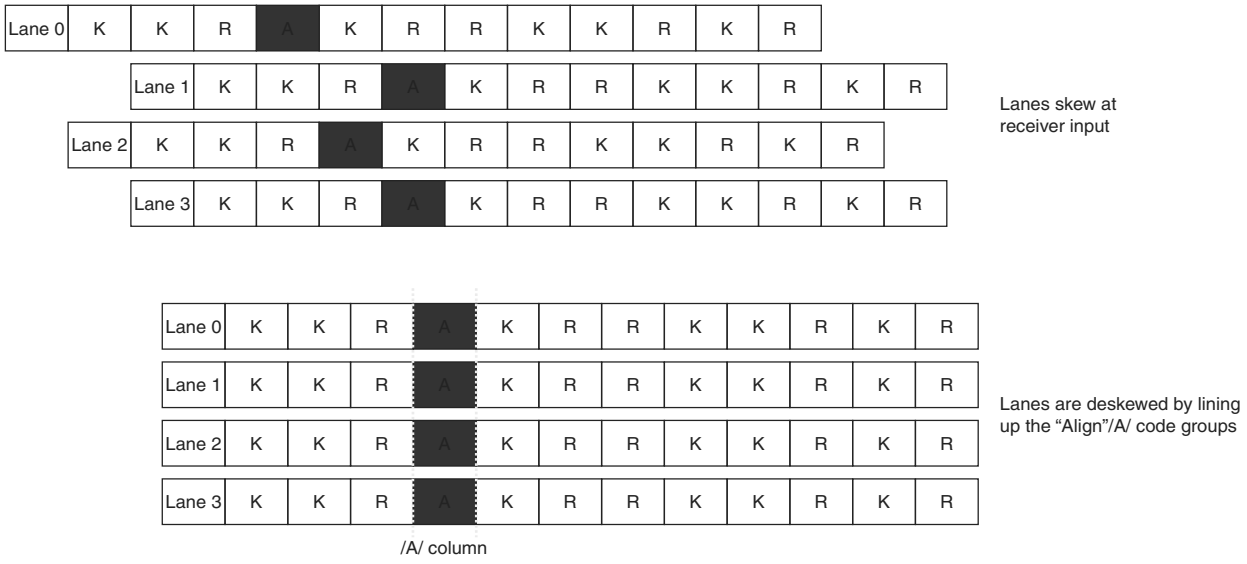
(1) Low-speed recovered clock.

(2) High-speed recovered clock.

- Channel alignment is acquired if three additional aligned ||A|| columns are observed at the output of the deskew FIFOs of the four channels after alignment of the first ||A|| column.
- Channel alignment is indicated by the assertion of `rx_channelaligned` signal.
- After acquiring channel alignment, if four misaligned ||A|| columns are seen at the output of the deskew FIFOs in all four channels with no aligned ||A|| columns in between, the `rx_channelaligned` signal is deasserted, indicating loss of channel alignment.

Figure 1–65 shows lane skew at the receiver input and how the deskew FIFO uses the /A/ code group to align the channels.

**Figure 1–65. Deskew FIFO–Lane Skew at the Receiver Input**




## Lane Synchronization

In XAUI mode, the word aligner is configured in automatic synchronization state machine mode that is compliant to the PCS synchronization state diagram specified in clause 48 of the IEEE P802.3ae specification. Table 1–23 lists the synchronization state machine parameters that implements the lane synchronization in XAUI mode.

**Table 1–23. Synchronization State Machine Parameters (1)**

| Parameter | Value |
|---|---|
| Number of valid synchronization (/K28.5/) code groups received to achieve synchronization | 4 |
| Number of erroneous code groups received to lose synchronization | 4 |
| Number of continuous good code groups received to reduce the error count by one | 4 |

**Note to Table 1–23:**

(1) The word aligner supports 7-bit and 10-bit pattern lengths in XAUI mode.

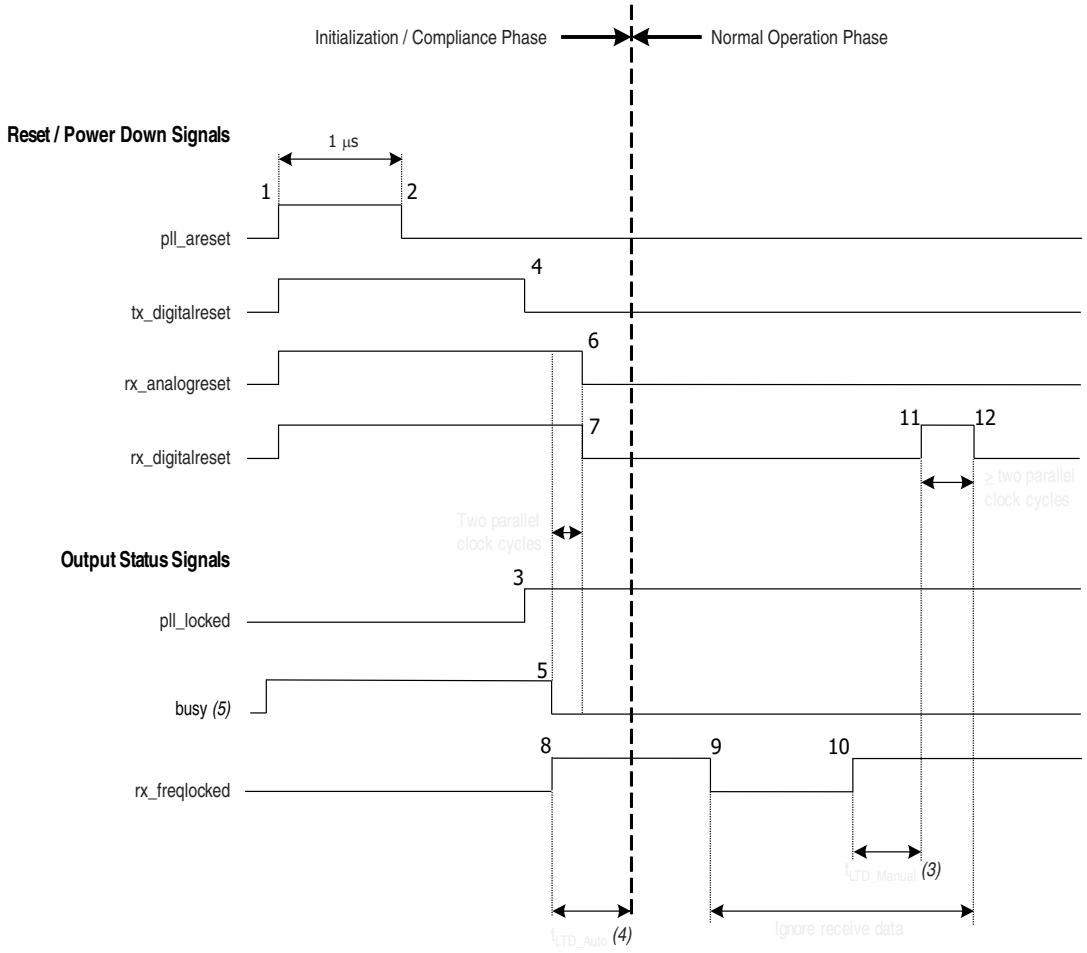
# PCIe Functional Mode

You can configure PCIe functional mode with or without the receiver clock rate compensation FIFO in the Cyclone IV GX device. The reset sequence remains the same whether or not you use the receiver clock rate compensation FIFO.

## PCIe Reset Sequence

The PCIe protocol consists of an initialization/compliance phase and a normal operation phase. The reset sequences for these two phases are described based on the timing diagram in Figure 2–10.

**Figure 2–10. Reset Sequence of PCIe Functional Mode (1), (2)**




**Notes to Figure 2–10:**

(1) This timing diagram is drawn based on the PCIe Gen 1 ×1 mode.

(2) For bonded PCIe Gen 1 ×2 and ×4 modes, there will be additional `rx_freqlocked[n]` signal. n=number of channels.

(3) For $t_{LTD\_Manual}$ duration, refer to the *Cyclone IV Device Datasheet* chapter.

(4) For $t_{LTD\_Auto}$ duration, refer to the *Cyclone IV Device Datasheet* chapter.

(5) The `busy` signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the `busy` signal is asserted and deasserted only if there is a read or write operation to the ALTGX_RECONFIG megafunction.

The **Offset cancellation for Receiver channels** option is automatically enabled in both the ALTGX and ALTGX_RECONFIG MegaWizard Plug-In Managers for **Receiver and Transmitter** and **Receiver only** configurations. It is not available for **Transmitter only** configurations. For **Receiver and Transmitter** and **Receiver only** configurations, you must connect the necessary interface signals between the ALTGX_RECONFIG and ALTGX (with receiver channels) instances.

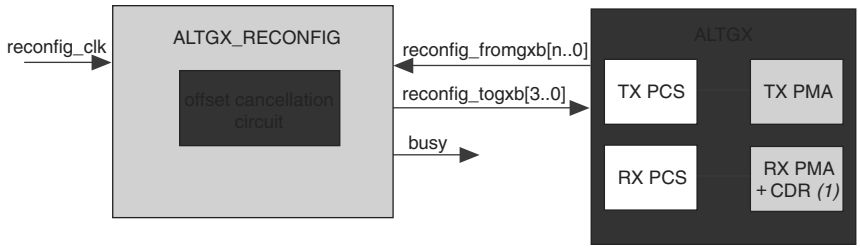
Offset cancellation is automatically executed once every time the device is powered on. The control logic for offset cancellation is integrated into the dynamic reconfiguration controller. You must connect the ALTGX_RECONFIG instance to the ALTGX instances (with receiver channels) in your design. You must connect the `reconfig_fromgxb`, `reconfig_togxb`, and necessary clock signals to both the ALTGX_RECONFIG and ALTGX (with receiver channels) instances.

When the device powers up, the dynamic reconfiguration controller initiates offset cancellation on the receiver channel by disconnecting the receiver input pins from the receiver data path. Subsequently, the offset cancellation process goes through different states and culminates in the offset cancellation of the receiver buffer.

☞ Offset cancellation process only occurs one time after power up and does not occur when subsequent `reconfig_reset` is asserted. If you assert `reconfig_reset` after the offset cancellation process is completed, the offset cancellation process will not run again.
If you assert `reconfig_reset` upon power up; offset cancellation will not begin until `reconfig_reset` is deasserted. If you assert `reconfig_reset` after power up but before offset cancellation process is completed; offset cancellation will not complete and restart only when `reconfig_reset` is deasserted.

Figure 3–2 shows the connection for offset cancellation mode.

**Figure 3–2. ALTGX and ALTGX_RECONFIG Connection for the Offset Cancellation Process**




**Note to Figure 3–2:**

(1) This block is active during the offset cancellation process.

☞ The dynamic reconfiguration controller sends and receives data to the transceiver channel through the `reconfig_togxb` and `reconfig_fromgxb` signals.

☞ The `gxb_powerdown` signal must not be asserted during the offset cancellation sequence.

The following are the channel reconfiguration mode options:

- Channel interface reconfiguration
- Data rate division at receiver channel

## Channel Interface Reconfiguration Mode

Enable this option if the reconfiguration of the transceiver channel involves the following changes:

- The reconfigured channel has a changed FPGA fabric-Transceiver channel interface data width
- The reconfigured channel has changed input control signals and output status signals
- The reconfigured channel has enabled and disabled the static PCS blocks of the transceiver channel

The following are the new input signals available when you enable this option:

- `tx_datainfull`—the width of this input signal depends on the number of channels you set up in the ALTGX MegaWizard Plug-In Manager. It is 22 bits wide per channel. This signal is available only for **Transmitter only** and **Receiver and Transmitter** configurations. This port replaces the existing `tx_datain` port.
- `rx_dataoutfull`—the width of this output signal depends on the number of channels you set up in the ALTGX MegaWizard Plug-In Manager. It is 32 bits wide per channel. This signal is available only for **Receiver only** and **Receiver and Transmitter** configurations. This port replaces the existing `rx_dataout` port.

  The Quartus II software has legality checks for the connectivity of `tx_datainfull` and `rx_dataoutfull` and the various control and status signals you enable in the **Clocking/Interface** screen. For example, the Quartus II software allows you to select and connect the `pipestatus` and `powerdn` signals. It assumes that you are planning to switch to and from PCI Express (PIPE) functional mode.

# Cyclone IV Device Handbook,

# Volume 3

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CYIV-5V3-2.1

**Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 3 of 4)**

| Symbol/ Description | Conditions | C6 | | | C7, I7 | | | C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Signal detect/loss threshold | PIPE mode | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | mV |
| $t_{LTR}$ *(10)* | — | — | — | 75 | — | — | 75 | — | — | 75 | µs |
| $t_{LTR-LTD\_Manual}$ *(11)* | — | 15 | — | — | 15 | — | — | 15 | — | — | µs |
| $t_{LTD}$ *(12)* | — | 0 | 100 | 4000 | 0 | 100 | 4000 | 0 | 100 | 4000 | ns |
| $t_{LTD\_Manual}$ *(13)* | — | — | — | 4000 | — | — | 4000 | — | — | 4000 | ns |
| $t_{LTD\_Auto}$ *(14)* | — | — | — | 4000 | — | — | 4000 | — | — | 4000 | ns |
| Receiver buffer and CDR offset cancellation time (per channel) | — | — | — | 17000 | — | — | 17000 | — | — | 17000 | reconfig_clk cycles |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 3 | — | — | 3 | — | — | 3 | — | dB |
| | DC Gain Setting = 2 | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| **Transmitter** | | | | | | | | | | | |
| Supported I/O Standards | 1.5 V PCML | | | | | | | | | | |
| Data rate (F324 and smaller package) | — | 600 | — | 2500 | 600 | — | 2500 | 600 | — | 2500 | Mbps |
| Data rate (F484 and larger package) | — | 600 | — | 3125 | 600 | — | 3125 | 600 | — | 2500 | Mbps |
| $V_{OCM}$ | 0.65 V setting | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Differential on-chip termination resistors | 100–Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| | 150–Ω setting | — | 150 | — | — | 150 | — | — | 150 | — | Ω |
| Differential and common mode return loss | PIPE, CPRI LV, Serial Rapid I/O SR, SDI, XAUI, SATA | Compliant | | | | | | | | | — |
| Rise time | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | ps |
| Fall time | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | ps |
| Intra-differential pair skew | — | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block skew | — | — | — | 120 | — | — | 120 | — | — | 120 | ps |