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Details

Product Status	Active
Number of LABs/CLBs	3491
Number of Logic Elements/Cells	55856
Total RAM Bits	2396160
Number of I/O	374
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce55f29c6n

3. Memory Blocks in Cyclone IV Devices

CYIV-51003-1.1

Cyclone® IV devices feature embedded memory structures to address the on-chip memory needs of Altera® Cyclone IV device designs. The embedded memory structure consists of columns of M9K memory blocks that you can configure to provide various memory functions, such as RAM, shift registers, ROM, and FIFO buffers.

This chapter contains the following sections:

- “Memory Modes” on page 3–7
- “Clocking Modes” on page 3–14
- “Design Considerations” on page 3–15

Overview

M9K blocks support the following features:

- 8,192 memory bits per block (9,216 bits per block including parity)
- Independent read-enable (*rden*) and write-enable (*wren*) signals for each port
- Packed mode in which the M9K memory block is split into two 4.5 K single-port RAMs
- Variable port configurations
- Single-port and simple dual-port modes support for all port widths
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Two clock-enable control signals for each port (port A and port B)
- Initialization file to pre-load memory content in RAM and ROM modes

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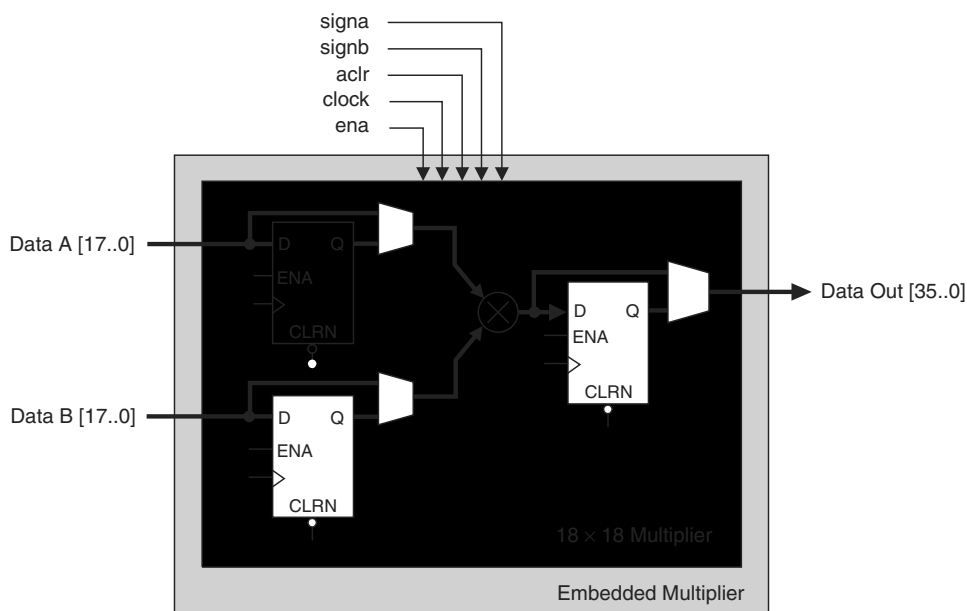


18-Bit Multipliers

You can configure each embedded multiplier to support a single 18×18 multiplier for input widths of 10 to 18 bits.

Figure 4-3 shows the embedded multiplier configured to support an 18-bit multiplier.

Figure 4-3. 18-Bit Multiplier Mode



All 18-bit multiplier inputs and results are independently sent through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Also, you can dynamically change the *signa* and *signb* signals and send these signals through dedicated input registers.

Document Revision History

Table 5-14 lists the revision history for this chapter.

Table 5-14. Document Revision History

Date	Version	Changes
October 2012	2.4	<ul style="list-style-type: none"> ■ Updated “Manual Override” and “PLL Cascading” sections. ■ Updated Figure 5-9.
November 2011	2.3	<ul style="list-style-type: none"> ■ Updated the “Dynamic Phase Shifting” section. ■ Updated Figure 5-26.
December 2010	2.2	<ul style="list-style-type: none"> ■ Updated for the Quartus II software version 10.1 release. ■ Updated Figure 5-3 and Figure 5-10. ■ Updated “GCLK Network Clock Source Generation”, “PLLs in Cyclone IV Devices”, and “Manual Override” sections. ■ Minor text edits.
July 2010	2.1	<ul style="list-style-type: none"> ■ Updated Figure 5-2, Figure 5-3, Figure 5-4, and Figure 5-10. ■ Updated Table 5-1, Table 5-2, and Table 5-5. ■ Updated “Clock Feedback Modes” section.
February 2010	2.0	<ul style="list-style-type: none"> ■ Added Cyclone IV E devices information for the Quartus II software version 9.1 SP1 release. ■ Updated “Clock Networks” section. ■ Updated Table 5-1 and Table 5-2. ■ Added Table 5-3. ■ Updated Figure 5-2, Figure 5-3, and Figure 5-9. ■ Added Figure 5-4 and Figure 5-10.
November 2009	1.0	Initial release.

Table 8-4. Configuration Schemes for Cyclone IV GX Devices (EP4CGX30 [only for F484 package], EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150) (Part 2 of 2)

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0	POR Delay	Configuration Voltage Standard (V) ⁽¹⁾
JTAG-based configuration (2)	(3)	(3)	(3)	(3)	—	—

Notes to Table 8-4:

- (1) Configuration voltage standard applied to the V_{CCIO} supply of the bank in which the configuration pins reside.
- (2) JTAG-based configuration takes precedence over other configuration schemes, which means the MSEL pin settings are ignored.
- (3) Do not leave the MSEL pins floating. Connect them to V_{CCA} or GND. These pins support the non-JTAG configuration scheme used in production. Altera recommends connecting the MSEL pins to GND if your device is only using JTAG configuration.


 Smaller Cyclone IV E devices or package options (E144 and F256 packages) do not have the MSEL[3] pin. The AS Fast POR configuration scheme at 3.0- or 2.5-V configuration voltage standard and the AP configuration scheme are not supported in Cyclone IV E devices without the MSEL[3] pin. To configure these devices with other supported configuration schemes, select MSEL[2..0] pins according to the MSEL settings in Table 8-5.

Table 8-5. Configuration Schemes for Cyclone IV E Devices

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0	POR Delay	Configuration Voltage Standard (V) ⁽¹⁾
AS	1	1	0	1	Fast	3.3
	0	1	0	0	Fast	3.0, 2.5
	0	0	1	0	Standard	3.3
	0	0	1	1	Standard	3.0, 2.5
AP	0	1	0	1	Fast	3.3
	0	1	1	0	Fast	1.8
	0	1	1	1	Standard	3.3
	1	0	1	1	Standard	3.0, 2.5
	1	0	0	0	Standard	1.8
PS	1	1	0	0	Fast	3.3, 3.0, 2.5
	0	0	0	0	Standard	3.3, 3.0, 2.5
FPP	1	1	1	0	Fast	3.3, 3.0, 2.5
	1	1	1	1	Fast	1.8, 1.5
JTAG-based configuration (2)	(3)	(3)	(3)	(3)	—	—

Notes to Table 8-5:

- (1) Configuration voltage standard applied to the V_{CCIO} supply of the bank in which the configuration pins reside.
- (2) JTAG-based configuration takes precedence over other configuration schemes, which means the MSEL pin settings are ignored.
- (3) Do not leave the MSEL pins floating. Connect them to V_{CCA} or GND. These pins support the non-JTAG configuration scheme used in production. Altera recommends connecting the MSEL pins to GND if your device is only using JTAG configuration.

four devices. During the first configuration cycle, the master device reads its configuration data from the serial configuration device while holding `nCEO` high. After completing its configuration cycle, the master device drives `nCE` low and sends the second copy of the configuration data to all three slave devices, configuring them simultaneously.

The advantage of the setup in Figure 8-4 is that you can have a different `.sof` for the master device. However, all the slave devices must be configured with the same `.sof`. You can either compress or uncompress the `.sof` in this configuration method.



You can still use this method if the master and slave devices use the same `.sof`.

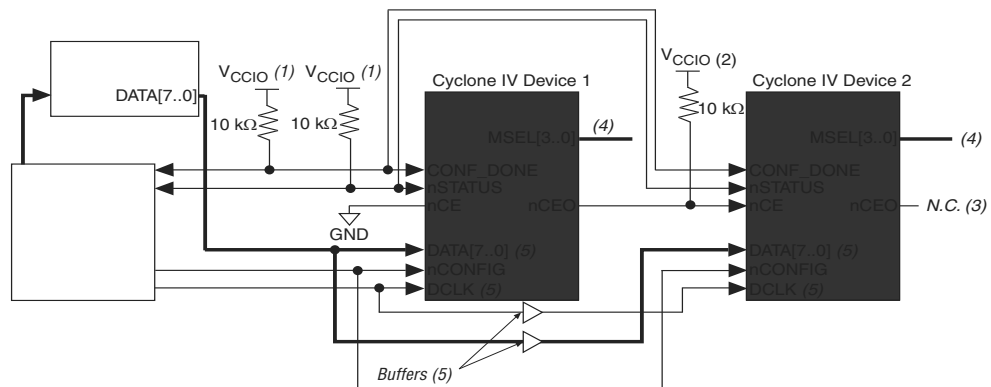
To ensure that DCLK and DATA[0] are not left floating at the end of the configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[0] pin is available as a user I/O pin after configuration. When you choose the FPP scheme in the Quartus II software, the DATA[0] pin is tri-stated by default in user mode and must be driven by the external host device. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box.

The DCLK speed must be below the specified system frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

The external host device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the external device to detect errors and to determine when programming is complete. If all configuration data is sent, but CONF_DONE or INIT_DONE has not gone high, the external device must reconfigure the target device.

Figure 8-20 shows how to configure multiple devices with a MAX II device. This circuit is similar to the FPP configuration circuit for a single device, except the Cyclone IV devices are cascaded for multi-device configuration.

Figure 8-20. Multi-Device FPP Configuration Using an External Host



Notes to Figure 8-20:

- (1) The pull-up resistor must be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.
- (2) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.
- (3) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8-4 on page 8-8 and Table 8-5 on page 8-9. Connect the MSEL pins directly to V_{CCA} or GND.
- (5) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[7..0] and DCLK must fit the maximum overshoot outlined in Equation 8-1 on page 8-5.

After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the nCE pin of the second device, which prompts the second device to begin configuration. The second device in the chain begins configuration in one clock cycle; therefore, the transfer of data destinations is transparent to the MAX II device. All other configuration pins (nCONFIG, nSTATUS,

Table 8-19. Configuration Pin Summary for Cyclone IV E Devices (Part 3 of 3)

Bank	Description	Input/Output	Dedicated	Powered By	Configuration Mode
5	DEV_CLRn	Input	—	V _{CCIO}	Optional, AP

Notes to Table 8-19:

- (1) To tri-state AS configuration pins in the AS configuration scheme, turn-on the **Enable input tri-state on active configuration pins in user mode** option from the **Device and Pin Options** dialog box. This tri-states DCLK, nCS0, Data[0], and Data[1]/ASDO pins. Dual-purpose pins settings for these pins are ignored. To set these pins to different settings, turn off the **Enable input tri-state on active configuration pins in user mode** option and set the desired setting from the Dual-purpose Pins Setting menu.
- (2) To tri-state AP configuration pins in the AP configuration scheme, turn-on the **Enable input tri-state on active configuration pins in user mode** option from the **Device and Pin Options** dialog box. This tri-states DCLK, Data[0..15], FLASH_nCE, and other AP pins. Dual-purpose pins settings for these pins are ignored. To set these pins to different settings, turn off the **Enable input tri-state on active configuration pins in user mode** option and set the desired setting from the Dual-purpose Pins Setting menu.
- (3) The CRC_ERROR pin is not available in Cyclone IV E devices with 1.0-V core voltage.
- (4) The CRC_ERROR pin is a dedicated open-drain output or an optional user I/O pin. Active high signal indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled in the Quartus II software from the **Error Detection CRC** tab of the **Device and Pin Options** dialog box. When using this pin, connect it to an external 10-k Ω pull-up resistor to an acceptable voltage that satisfies the input voltage of the receiving device.

Table 8-20 describes the dedicated configuration pins. You must properly connect these pins on your board for successful configuration. You may not need some of these pins for your configuration schemes.

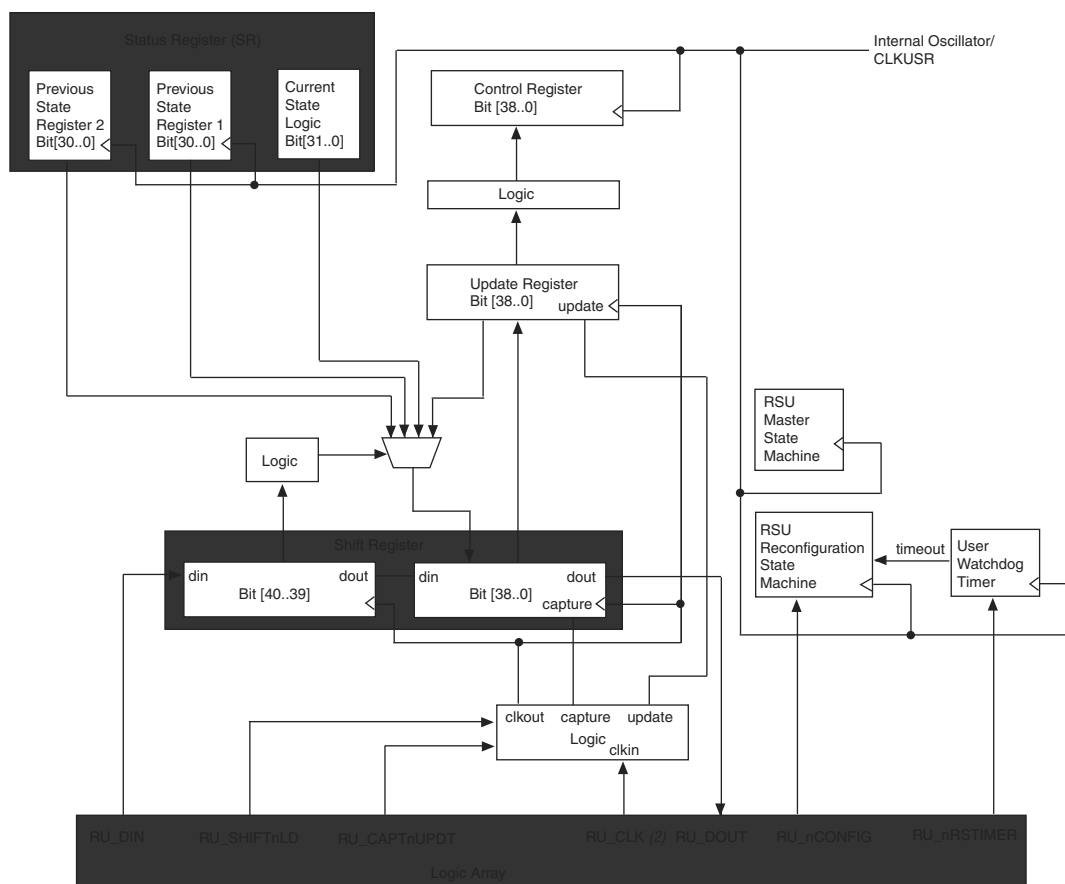
Table 8-20. Dedicated Configuration Pins on the Cyclone IV Device (Part 1 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
MSEL	N/A	All	Input	Configuration input that sets the Cyclone IV device configuration scheme. You must hardwire these pins to V _{CCA} or GND. The MSEL pins have internal 9-k Ω pull-down resistors that are always active.
nCONFIG	N/A	All	Input	Configuration control input. Pulling this pin low with external circuitry during user mode causes the Cyclone IV device to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic-high level starts a reconfiguration.
nSTATUS	N/A	All	Bidirectional open-drain	<p>The Cyclone IV device drives nSTATUS low immediately after power-up and releases it after the POR time.</p> <ul style="list-style-type: none"> ■ Status output—if an error occurs during configuration, nSTATUS is pulled low by the target device. ■ Status input—if an external source (for example, another Cyclone IV device) drives the nSTATUS pin low during configuration or initialization, the target device enters an error state. <p>Driving nSTATUS low after configuration and initialization does not affect the configured device. If you use a configuration device, driving nSTATUS low causes the configuration device to attempt to configure the device, but because the device ignores transitions on nSTATUS in user mode, the device does not reconfigure. To start a reconfiguration, you must pull nCONFIG low.</p>

Dedicated Remote System Upgrade Circuitry

This section describes the implementation of the Cyclone IV device remote system upgrade dedicated circuitry. The remote system upgrade circuitry is implemented in hard logic. This dedicated circuitry interfaces with the user-defined factory application configurations implemented in the Cyclone IV device logic array to provide the complete remote configuration solution. The remote system upgrade circuitry contains the remote system upgrade registers, a watchdog timer, and state machines that control those components. Figure 8-33 shows the data path of the remote system upgrade block.

Figure 8-33. Remote System Upgrade Circuit Data Path ⁽¹⁾



Notes to Figure 8-33:

- (1) The RU_DOUT, RU_SHIFTnLD, RU_CAPTnUPDT, RU_CLK, RU_DIN, RU_nCONFIG, and RU_nRSTIMER signals are internally controlled by the ALTREMOTE_UPDATE megafunction.
- (2) The RU_CLK refers to the ALTREMOTE_UPDATE megafunction block "clock" input. For more information, refer to the *Remote Update Circuitry (ALTREMOTE_UPDATE) Megafunction User Guide*.

11. Power Requirements for Cyclone IV Devices

CYIV-51011-1.3

This chapter describes information about external power supply requirements, hot-socketing specifications, power-on reset (POR) requirements, and their implementation in Cyclone IV devices.

This chapter includes the following sections:

- “External Power Supply Requirements” on page 11–1
- “Hot-Socketing Specifications” on page 11–2
- “Hot-socketing Feature Implementation” on page 11–3
- “Power-On Reset Circuitry” on page 11–3

External Power Supply Requirements

This section describes the different external power supplies required to power Cyclone IV devices. Table 11–1 and Table 11–2 list the descriptions of external power supply pins for Cyclone IV GX and Cyclone IV E devices, respectively.

- For each Altera recommended power supply’s operating conditions, refer to the *Cyclone IV Device Datasheet* chapter.
- For power supply pin connection guidelines and power regulator sharing, refer to the *Cyclone IV Device Family Pin Connection Guidelines*.

Table 11–1. Power Supply Descriptions for the Cyclone IV GX Devices (Part 1 of 2)

Power Supply Pin	Nominal Voltage Level (V)	Description
VCCINT	1.2	Core voltage, PCI Express (PCIe) hard IP block, and transceiver physical coding sublayer (PCS) power supply
VCCA ⁽¹⁾	2.5	PLL analog power supply
VCCD_PLL	1.2	PLL digital power supply
VCCIO ⁽²⁾	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	I/O banks power supply
VCC_CLKIN ^{(3), (4)}	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	Differential clock input pins power supply
VCCH_GXB	2.5	Transceiver output (TX) buffer power supply
VCCA_GXB	2.5	Transceiver physical medium attachment (PMA) and auxiliary power supply

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Word Aligner

Figure 1-16 shows the word aligner block diagram. The word aligner receives parallel data from the deserializer and restores the word boundary based on a pre-defined alignment pattern that must be received during link synchronization. The word aligner supports three operational modes as listed in Table 1-3.

Figure 1-16. Word Aligner Block Diagram

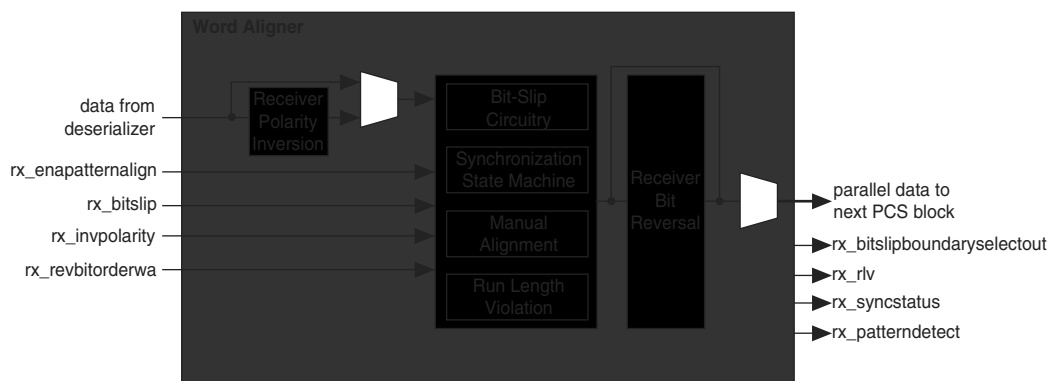


Table 1-3. Word Aligner Modes

Modes	PMA-PCS Interface Widths	Allowed Word Alignment Pattern Lengths
Manual Alignment	8-bit	16 bits
	10-bit	7 or 10 bits
Bit-Slip	8-bit	16 bits
	10-bit	7 or 10 bits
Automatic Synchronization State Machine	10-bit	7 or 10 bits

Manual Alignment Mode

In manual alignment mode, the `rx_enapatternalign` port controls the word aligner with either an 8- or 10-bit data width setting.

The 8-bit word aligner is edge-sensitive to the `rx_enapatternalign` signal. A rising edge on `rx_enapatternalign` signal after deassertion of the `rx_digitalreset` signal triggers the word aligner to look for the word alignment pattern in the received data stream. It updates the word boundary if it finds the word alignment pattern in a new word boundary. Any word alignment pattern received thereafter in a different word boundary causes the word aligner to re-align to the new word boundary only if there is a rising edge in the `rx_enapatternalign` signal.

The 10-bit word aligner is level-sensitive to the `rx_enapatternalign` signal. The word aligner looks for the programmed 7-bit or 10-bit word alignment pattern or its complement in the received data stream, if the `rx_enapatternalign` signal is held high. It updates the word boundary if it finds the word alignment pattern in a new word boundary. If the `rx_enapatternalign` signal is deasserted, the word aligner maintains the current word boundary even when it receives the word alignment pattern in a new word boundary.

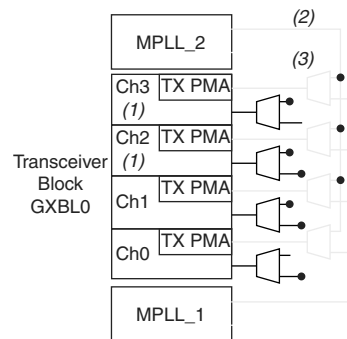
Transceiver Clocking Architecture

The multipurpose PLLs and general-purpose PLLs located on the left side of the device generate the clocks required for the transceiver operation. The following sections describe the Cyclone IV GX transceiver clocking architecture:

- “Input Reference Clocking” on page 1-27
- “Transceiver Channel Datapath Clocking” on page 1-29
- “FPGA Fabric-Transceiver Interface Clocking” on page 1-43

Figure 1–31 and Figure 1–32 show the high- and low-speed clock distribution for transceivers in F324 and smaller packages, and in F484 and larger packages in non-bonded channel configuration.

Figure 1–31. Clock Distribution in Non-Bonded Channel Configuration for Transceivers in F324 and Smaller Packages



Notes to Figure 1–31:

- (1) Transceiver channels 2 and 3 are not available for devices in F169 and smaller packages.
- (2) High-speed clock.
- (3) Low-speed clock.

When the byte serializer is enabled, the low-speed clock frequency is halved before feeding into the read clock of TX phase compensation FIFO. The low-speed clock is available in the FPGA fabric as `tx_clkout` port, which can be used in the FPGA fabric to send transmitter data and control signals.

Figure 1-33. Transmitter Only Datapath Clocking in Non-Bonded Channel Configuration

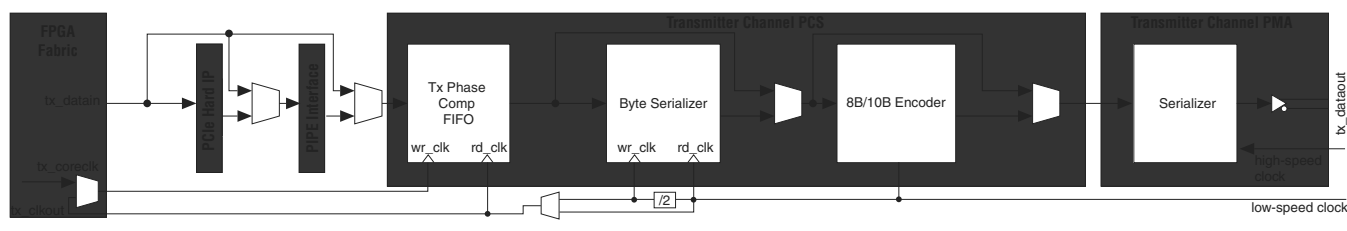
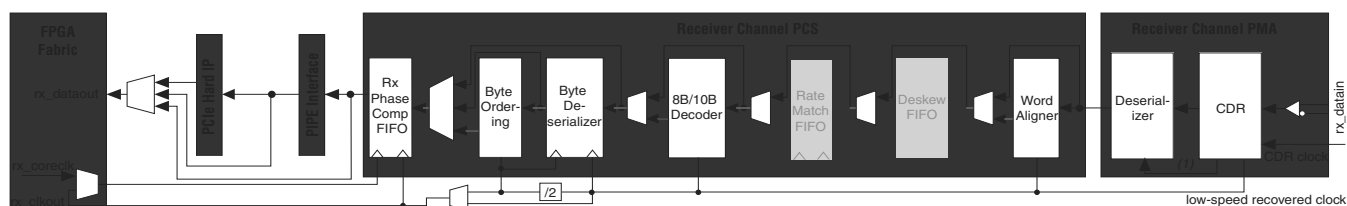


Figure 1-34 shows the datapath clocking in receiver only operation. In this mode, the receiver PCS supports configuration without the rate match FIFO. The CDR unit in the channel recovers the clock from the received serial data and generates the high-speed recovered clock for the deserializer, and low-speed recovered clock for forwarding to the receiver PCS. The low-speed recovered clock feeds to the following blocks in the receiver PCS:

- word aligner
- 8B/10B decoder
- write clock of byte deserializer
- byte ordering
- write clock of RX phase compensation FIFO

When the byte deserializer is enabled, the low-speed recovered clock frequency is halved before feeding into the write clock of the RX phase compensation FIFO. The low-speed recovered clock is available in the FPGA fabric as `rx_clkout` port, which can be used in the FPGA fabric to capture receiver data and status signals.

Figure 1-34. Receiver Only Datapath Clocking without Rate Match FIFO in Non-Bonded Channel Configuration



Note to Figure 1-34:

- (1) High-speed recovered clock.

When the transceiver is configured for transmitter and receiver operation in non-bonded channel configuration, the receiver PCS supports configuration with and without the rate match FIFO. The difference is only at the receiver datapath clocking. The transmitter datapath clocking is identical to transmitter only operation mode as shown in Figure 1-33.

Configuring the hard IP module requires using the PCI Express Compiler. When configuring the transceiver for PCIe implementation with hard IP module, the byte serializer and deserializer are not enabled, providing an 8-bit transceiver-PIPE-hard IP data interface width running at 250 MHz clock frequency.


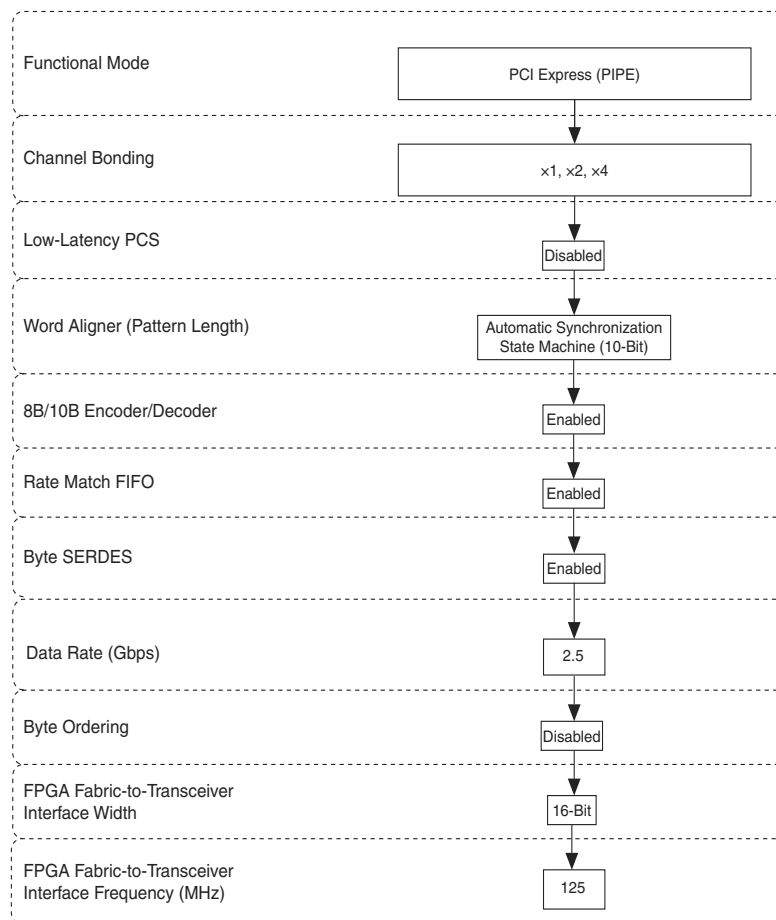


 For more information about PCIe implementation with hard IP module, refer to the *PCI Express Compiler User Guide*.

Figure 1-49 shows the transceiver configuration in PIPE mode.

Figure 1-49. Transceiver Configuration in PIPE Mode



 When configuring the transceiver into PIPE mode using ALTGX megafunction for PCIe implementation, the PHY-MAC, data link and transaction layers must be implemented in user logics. The PCIe hard IP block is bypassed in this configuration.

 The busy signal remains low for the first `reconfig_clk` clock cycle. It then gets asserted from the second `reconfig_clk` clock cycle. Subsequent deassertion of the busy signal indicates the completion of the offset cancellation process. This busy signal is required in transceiver reset sequences except for transmitter only channel configurations. Refer to the reset sequences shown in Figure 2–2 and the associated references listed in the notes for the figure.


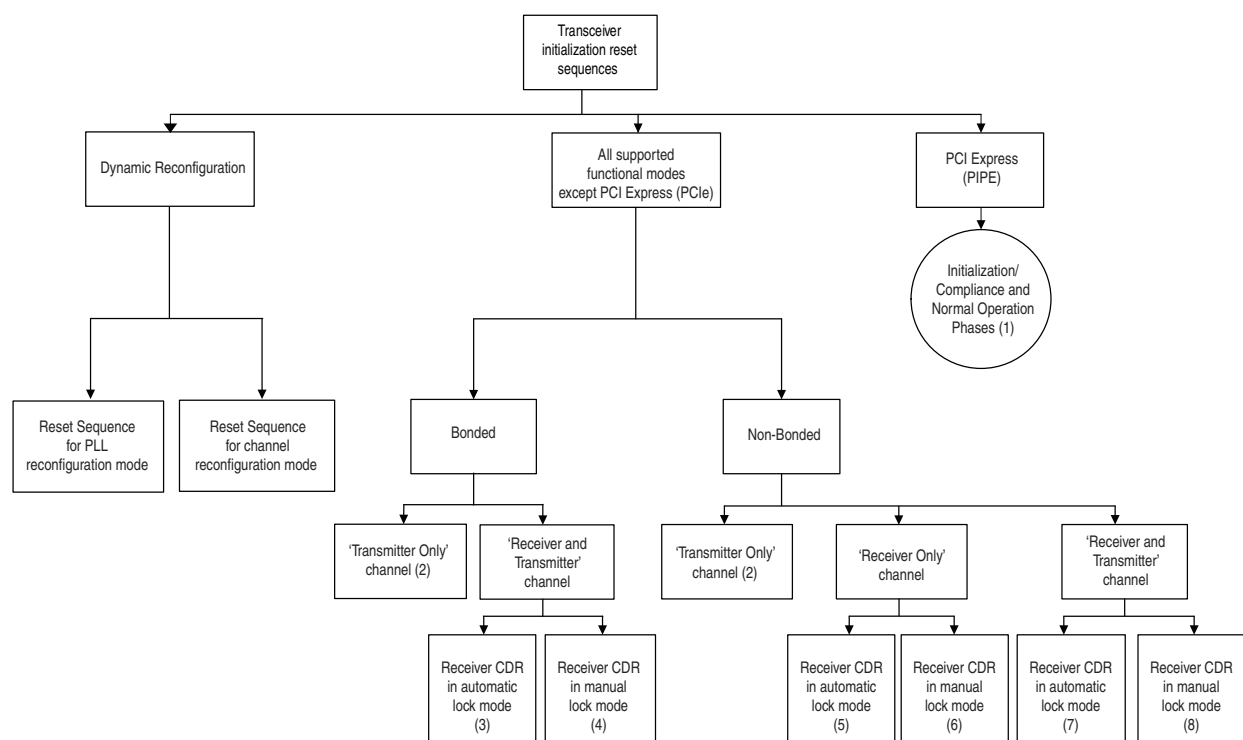
 Altera strongly recommends adhering to these reset sequences for proper operation of the Cyclone IV GX transceiver.

Figure 2–2 shows the transceiver reset sequences for Cyclone IV GX devices.

Figure 2–2. Transceiver Reset Sequences Chart




Notes to Figure 2–2:

- (1) Refer to the Timing Diagram in Figure 2–10.
- (2) Refer to the Timing Diagram in Figure 2–3.
- (3) Refer to the Timing Diagram in Figure 2–4.
- (4) Refer to the Timing Diagram in Figure 2–5.
- (5) Refer to the Timing Diagram in Figure 2–6.
- (6) Refer to the Timing Diagram in Figure 2–7.
- (7) Refer to the Timing Diagram in Figure 2–8.
- (8) Refer to the Timing Diagram in Figure 2–9.

The **Offset cancellation for Receiver channels** option is automatically enabled in both the ALTGX and ALTGX_RECONFIG MegaWizard Plug-In Managers for **Receiver and Transmitter** and **Receiver only** configurations. It is not available for **Transmitter only** configurations. For **Receiver and Transmitter** and **Receiver only** configurations, you must connect the necessary interface signals between the ALTGX_RECONFIG and ALTGX (with receiver channels) instances.

Offset cancellation is automatically executed once every time the device is powered on. The control logic for offset cancellation is integrated into the dynamic reconfiguration controller. You must connect the ALTGX_RECONFIG instance to the ALTGX instances (with receiver channels) in your design. You must connect the reconfig_fromgxb, reconfig_togxb, and necessary clock signals to both the ALTGX_RECONFIG and ALTGX (with receiver channels) instances.

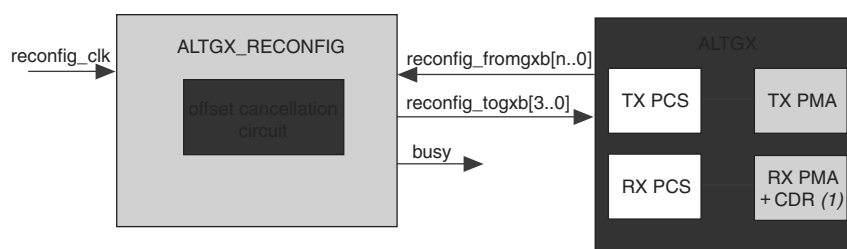
When the device powers up, the dynamic reconfiguration controller initiates offset cancellation on the receiver channel by disconnecting the receiver input pins from the receiver data path. Subsequently, the offset cancellation process goes through different states and culminates in the offset cancellation of the receiver buffer.

 Offset cancellation process only occurs one time after power up and does not occur when subsequent reconfig_reset is asserted. If you assert reconfig_reset after the offset cancellation process is completed, the offset cancellation process will not run again.

If you assert reconfig_reset upon power up; offset cancellation will not begin until reconfig_reset is deasserted. If you assert reconfig_reset after power up but before offset cancellation process is completed; offset cancellation will not complete and restart only when reconfig_reset is deasserted.


Figure 3-2 shows the connection for offset cancellation mode.


Figure 3-2. ALTGX and ALTGX_RECONFIG Connection for the Offset Cancellation Process



Note to Figure 3-2:

(1) This block is active during the offset cancellation process.

 The dynamic reconfiguration controller sends and receives data to the transceiver channel through the reconfig_togxb and reconfig_fromgxb signals.

 The gxb_powerdown signal must not be asserted during the offset cancellation sequence.

The following are the channel reconfiguration mode options:

- Channel interface reconfiguration
- Data rate division at receiver channel

Channel Interface Reconfiguration Mode

Enable this option if the reconfiguration of the transceiver channel involves the following changes:

- The reconfigured channel has a changed FPGA fabric-Transceiver channel interface data width
- The reconfigured channel has changed input control signals and output status signals
- The reconfigured channel has enabled and disabled the static PCS blocks of the transceiver channel

The following are the new input signals available when you enable this option:

- `tx_dataainfull`—the width of this input signal depends on the number of channels you set up in the ALTGX MegaWizard Plug-In Manager. It is 22 bits wide per channel. This signal is available only for **Transmitter only** and **Receiver and Transmitter** configurations. This port replaces the existing `tx_dataain` port.
- `rx_dataoutfull`—the width of this output signal depends on the number of channels you set up in the ALTGX MegaWizard Plug-In Manager. It is 32 bits wide per channel. This signal is available only for **Receiver only** and **Receiver and Transmitter** configurations. This port replaces the existing `rx_dataout` port.

The Quartus II software has legality checks for the connectivity of `tx_dataainfull` and `rx_dataoutfull` and the various control and status signals you enable in the **Clocking/Interface** screen. For example, the Quartus II software allows you to select and connect the `pipestatus` and `powerdn` signals. It assumes that you are planning to switch to and from PCI Express (PIPE) functional mode.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Parallel (AP) ⁽¹⁾	20 to 40	33	MHz
Active Serial (AS)	20 to 40	33	MHz

Note to Table 1–29:

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

Table 1–30. JTAG Timing Parameters for Cyclone IV Devices ⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	19	—	ns
t_{JCL}	TCK clock low time	19	—	ns
t_{JPSU_TDI}	JTAG port setup time for TDI	1	—	ns
t_{JPSU_TMS}	JTAG port setup time for TMS	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output ^{(2), (3)}	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output ^{(2), (3)}	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance ^{(2), (3)}	—	15	ns
t_{JSSU}	Capture register setup time	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 1–30:

- (1) For more information about JTAG waveforms, refer to “JTAG Waveform” in “Glossary” on page 1–37.
- (2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.
- (3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.054	1.924	3.387	4.017	3.411	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.010	1.875	3.341	4.252	3.367	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.641	0.631	1.111	1.377	1.124	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.971	0.931	1.684	2.298	1.684	ns

Notes to Table 1–40:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices ^{(1), (2)}

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.057	1.921	3.389	4.146	3.412	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.059	1.919	3.420	4.374	3.441	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.670	0.623	1.160	1.420	1.168	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.960	0.919	1.656	2.258	1.656	ns

Notes to Table 1–41:

- (1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.