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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3491
Number of Logic Elements/Cells	55856
Total RAM Bits	2396160
Number of I/O	374
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce55f29i8ln

This chapter provides additional information about the document and Altera.

About this Handbook

This handbook provides comprehensive information about the Altera® Cyclone® IV family of devices.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact ⁽¹⁾	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general) (software licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

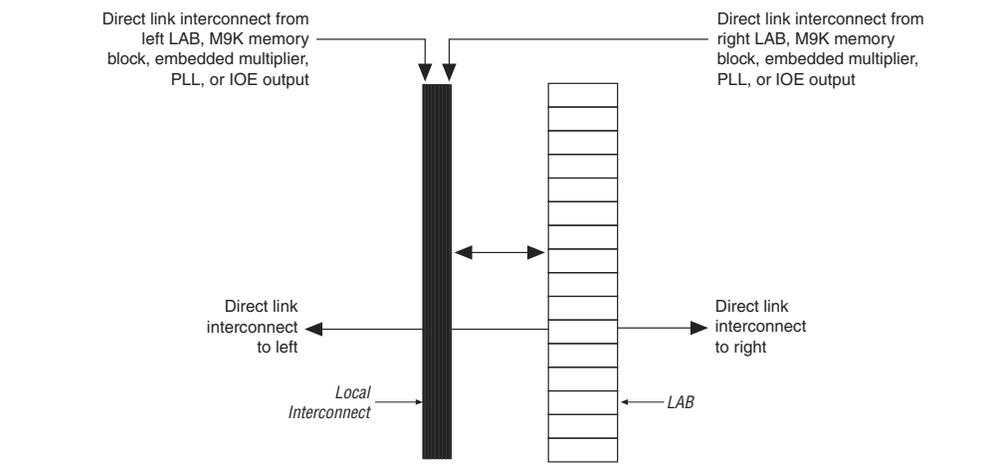
Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, <code>\qdesigns</code> directory, D: drive, and <code>chiptrip.gdf</code> file.
<i>Italic Type with Initial Capital Letters</i>	Indicate document titles. For example, <i>Stratix IV Design Guidelines</i> .
<i>italic type</i>	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>.pof file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
“Subheading Title”	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”

LAB Interconnects

The LAB local interconnect is driven by column and row interconnects and LE outputs in the same LAB. Neighboring LABs, phase-locked loops (PLLs), M9K RAM blocks, and embedded multipliers from the left and right can also drive the local interconnect of a LAB through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive up to 48 LEs through fast local and direct link interconnects.

Figure 2-5 shows the direct link connection.

Figure 2-5. Cyclone IV Device Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include:

- Two clocks
- Two clock enables
- Two asynchronous clears
- One synchronous clear
- One synchronous load

You can use up to eight control signals at a time. Register packing and synchronous load cannot be used simultaneously.

Each LAB can have up to four non-global control signals. You can use additional LAB control signals as long as they are global signals.

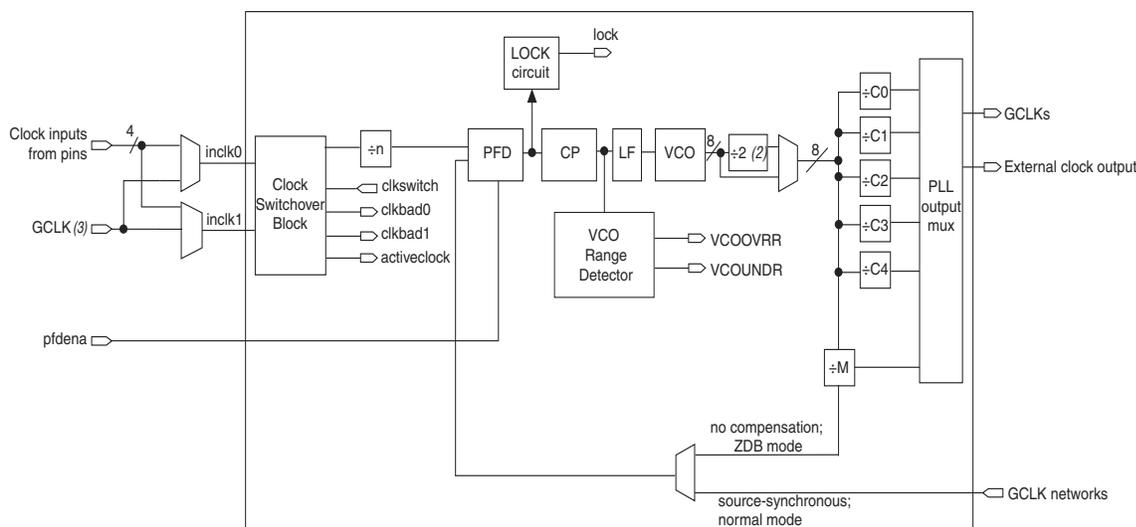
Synchronous clear and load signals are useful for implementing counters and other functions. The synchronous clear and synchronous load signals are LAB-wide signals that affect all registers in the LAB.

Table 5-2. GCLK Network Connections for EP4CGX30, EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 Devices ^{(1), (2)} (Part 2 of 4)

GCLK Network Clock Sources	GCLK Networks																													
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PLL_3_C0	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	✓	—	—	—	—	—	—	✓	—	—	✓	—	✓
PLL_3_C1	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—	—	—	✓	—	—	✓	—
PLL_3_C2	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—
PLL_3_C3	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—
PLL_3_C4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	✓	—	—	—	—	—	—	—	—	✓	—	✓	✓
PLL_4_C0	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	✓	✓	—	—	✓	—	✓	—	—	—	—	—	—
PLL_4_C1	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	—	✓	—	—	✓	—	—	—	—	—	—	—
PLL_4_C2	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—
PLL_4_C3	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—
PLL_4_C4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	✓	—	—	✓	—	✓	✓	—	—	—	—	—	—
PLL_5_C0	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_5_C1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_5_C2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_5_C3	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_5_C4	—	—	✓	—	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C0	✓	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_6_C4	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C0 ⁽³⁾	—	—	—	—	—	—	✓	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C1 ⁽³⁾	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C2 ⁽³⁾	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C3 ⁽³⁾	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL_7_C4 ⁽³⁾	—	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Figure 5-10 shows a simplified block diagram of the major components of the PLL of Cyclone IV E devices.

Figure 5-10. Cyclone IV E PLL Block Diagram ⁽¹⁾



Notes to Figure 5-10:

- (1) Each clock source can come from any of the four clock pins located on the same side of the device as the PLL.
- (2) This is the VCO post-scale counter K.
- (3) This input port is fed by a pin-driven dedicated GCLK, or through a clock control block if the clock control block is fed by an output from another PLL or a pin-driven dedicated GCLK. An internally generated global signal cannot drive the PLL.

 The VCO post-scale counter K is used to divide the supported VCO range by two. The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter value. Therefore, if the VCO post-scale counter has a value of 2, the frequency reported is lower than the f_{VCO} specification specified in the *Cyclone IV Device Datasheet* chapter.

External Clock Outputs

Each PLL of Cyclone IV devices supports one single-ended clock output or one differential clock output. Only the C0 output counter can feed the dedicated external clock outputs, as shown in Figure 5-11, without going through the GCLK. Other output counters can feed other I/O pins through the GCLK.

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figure 6-5 and Figure 6-6.

Figure 6-5. Cyclone IV Devices HSTL I/O Standard Termination

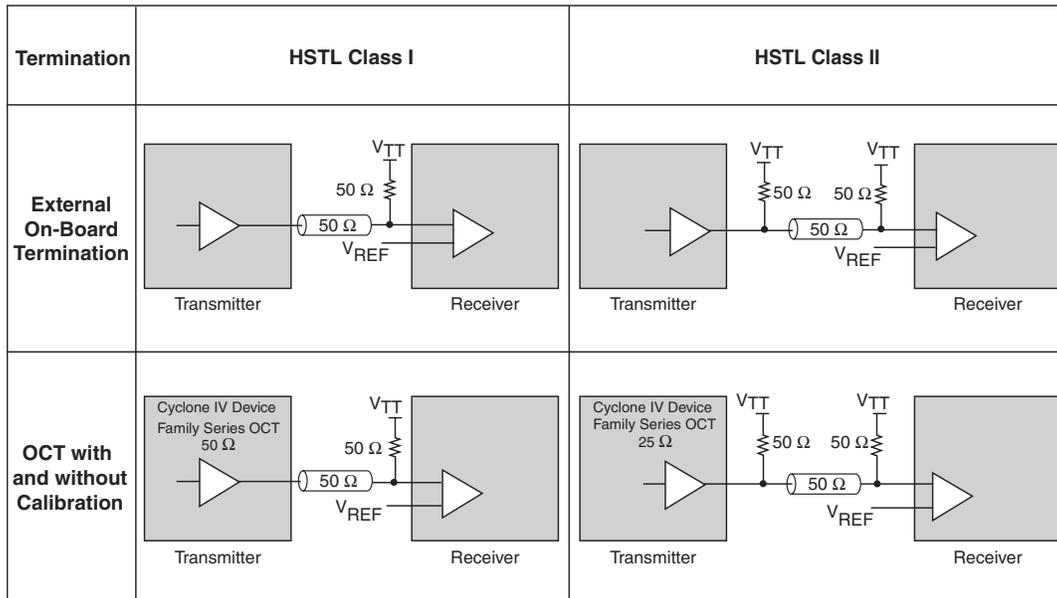
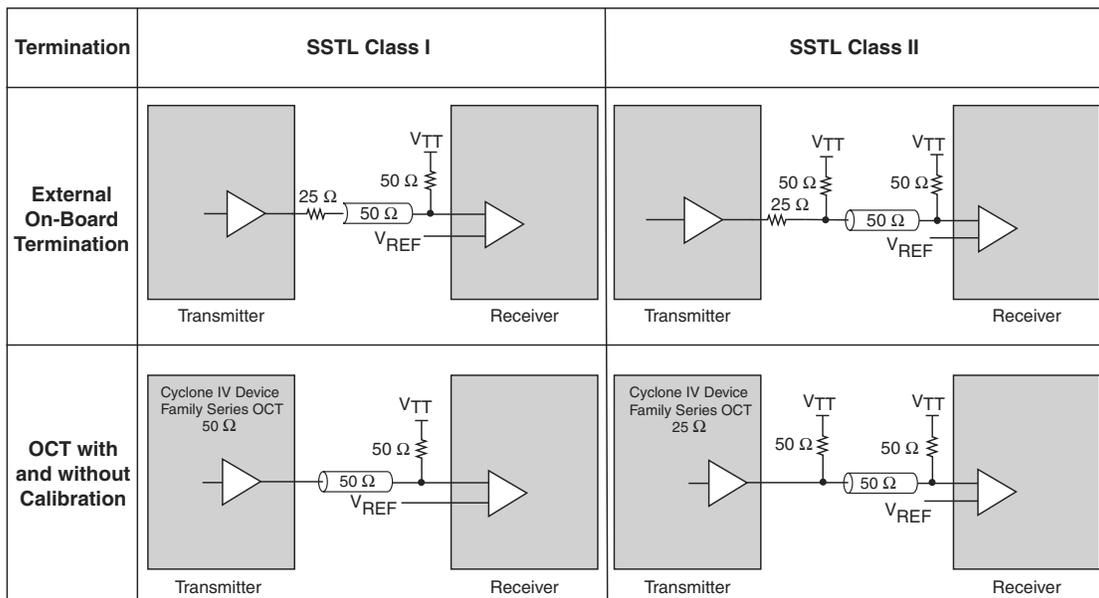


Figure 6-6. Cyclone IV Devices SSTL I/O Standard Termination



Designing with LVDS

Cyclone IV I/O banks support the LVDS I/O standard. The Cyclone IV GX right I/O banks support true LVDS transmitters while the Cyclone IV E left and right I/O banks support LVDS transmitters. On the top and bottom I/O banks, the emulated LVDS transmitters are supported using two single-ended output buffers with external resistors. One of the single-ended output buffers is programmed to have opposite polarity. The LVDS receiver requires an external 100- Ω termination resistor between the two signals at the input buffer.

Figure 6-12 shows a point-to-point LVDS interface using Cyclone IV devices true LVDS output and input buffers.

Figure 6-12. Cyclone IV Devices LVDS Interface with True Output Buffer on the Right I/O Banks

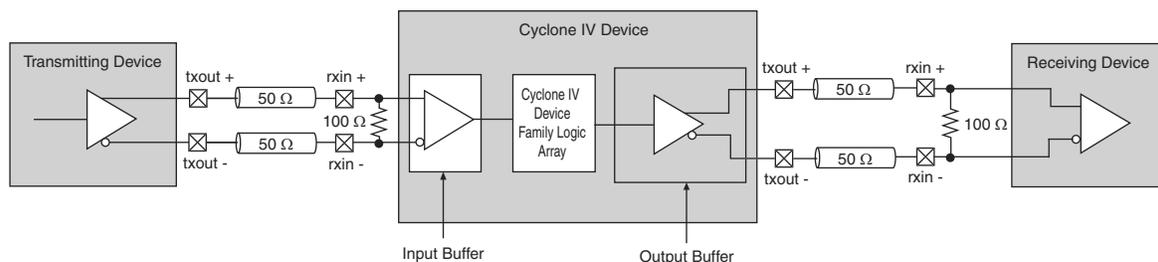
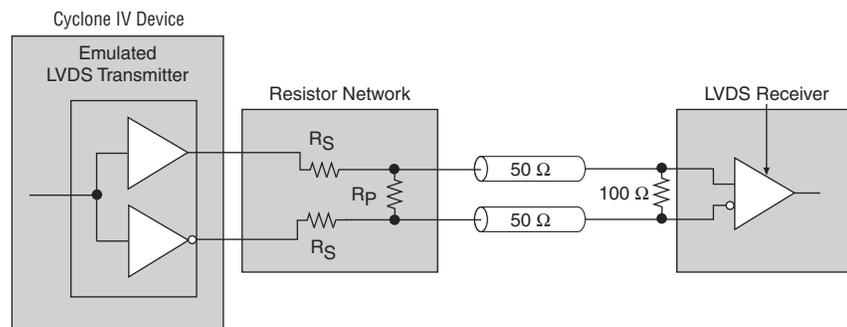


Figure 6-13 shows a point-to-point LVDS interface with Cyclone IV devices LVDS using two single-ended output buffers and external resistors.

Figure 6-13. LVDS Interface with External Resistor Network on the Top and Bottom I/O Banks (1)



Note to Figure 6-13:

(1) $R_S = 120 \Omega$. $R_P = 170 \Omega$.

BLVDS I/O Standard Support in Cyclone IV Devices

The BLVDS I/O standard is a high-speed differential data transmission technology that extends the benefits of standard point-to-point LVDS to multipoint configuration that supports bidirectional half-duplex communication. BLVDS differs from standard LVDS by providing a higher drive to achieve similar signal swings at the receiver while loaded with two terminations at both ends of the bus.

Table 8–2. Uncompressed Raw Binary File (.rbf) Sizes for Cyclone IV Devices (Part 2 of 2)

	Device	Data Size (bits)
Cyclone IV GX	EP4CGX15	3,805,568
	EP4CGX22	7,600,040
	EP4CGX30	7,600,040
		22,010,888 ⁽¹⁾
	EP4CGX50	22,010,888
	EP4CGX75	22,010,888
	EP4CGX110	39,425,016
	EP4CGX150	39,425,016

Note to Table 8–2:

(1) Only for the F484 package.

Use the data in Table 8–2 to estimate the file size before design compilation. Different configuration file formats, such as Hexadecimal (.hex) or Tabular Text File (.tff) formats, have different file sizes. However, for any specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you use compression, the file size varies after each compilation, because the compression ratio depends on the design.



For more information about setting device configuration options or creating configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook*.

Configuration and JTAG Pin I/O Requirements

Cyclone IV devices are manufactured using the TSMC 60-nm low-k dielectric process. Although Cyclone IV devices use TSMC 2.5-V transistor technology in the I/O buffers, the devices are compatible and able to interface with 2.5, 3.0, and 3.3-V configuration voltage standards by following specific requirements.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. When using a serial configuration device in an AS configuration scheme, you must connect a 25-Ω series resistor for the DATA [0] pin. When cascading the Cyclone IV device family in a multi-device configuration for AS, AP, FPP, and PS configuration schemes, you must connect the repeater buffers between the master and slave devices for the DATA and DCLK pins. When using the JTAG configuration scheme in a multi-device configuration, connect 25-Ω resistors on both ends of the TDO-TDI path if the TDO output driver is a non-Cyclone IV device.

The output resistance of the repeater buffers and the TDO path for all cases must fit the maximum overshoot equation shown in Equation 8–1.

Equation 8–1. ⁽¹⁾

$$0.8Z_O \leq R_E \leq 1.8Z_O$$

Note to Equation 8–1:(1) Z_O is the transmission line impedance and R_E is the equivalent resistance of the output buffer.

Altera recommends putting a buffer before the DATA and DCLK output from the master device to avoid signal strength and signal integrity issues. The buffer must not significantly change the DATA-to-DCLK relationships or delay them with respect to other AS signals (ASDI and nCS). Also, the buffer must only drive the slave devices to ensure that the timing between the master device and the serial configuration device is unaffected.

This configuration method supports both compressed and uncompressed .sof. Therefore, if the configuration bitstream size exceeds the capacity of a serial configuration device, you can enable the compression feature in the .sof or you can select a larger serial configuration device.

Guidelines for Connecting a Serial Configuration Device to Cyclone IV Devices for an AS Interface

For single- and multi-device AS configurations, the board trace length and loading between the supported serial configuration device and Cyclone IV device must follow the recommendations listed in Table 8-7.

Table 8-7. Maximum Trace Length and Loading for AS Configuration

Cyclone IV Device AS Pins	Maximum Board Trace Length from a Cyclone IV Device to a Serial Configuration Device (Inches)		Maximum Board Load (pF)
	Cyclone IV E	Cyclone IV GX	
DCLK	10	6	15
DATA [0]	10	6	30
nCSO	10	6	30
ASDO	10	6	30

Note to Table 8-7:

- (1) For multi-devices AS configuration using Cyclone IV E with 1.0 V core voltage, the maximum board trace-length from the serial configuration device to the junction-split on both DCLK and Data0 line is 3.5 inches.

Estimating AS Configuration Time

AS configuration time is dominated by the time it takes to transfer data from the serial configuration device to the Cyclone IV device. This serial interface is clocked by the Cyclone IV device DCLK output (generated from a 40-MHz internal oscillator for Cyclone IV E devices, a 20- or 40-MHz internal oscillator, or an external CLKUSR of up to 40 MHz for Cyclone IV GX devices).

Equation 8-2 and Equation 8-3 show the configuration time calculations.

Equation 8-2.

$$\text{Size} \times \left(\frac{\text{maximum DCLK period}}{1 \text{ bit}} \right) = \text{estimated maximum configuration time}$$

Equation 8-3.

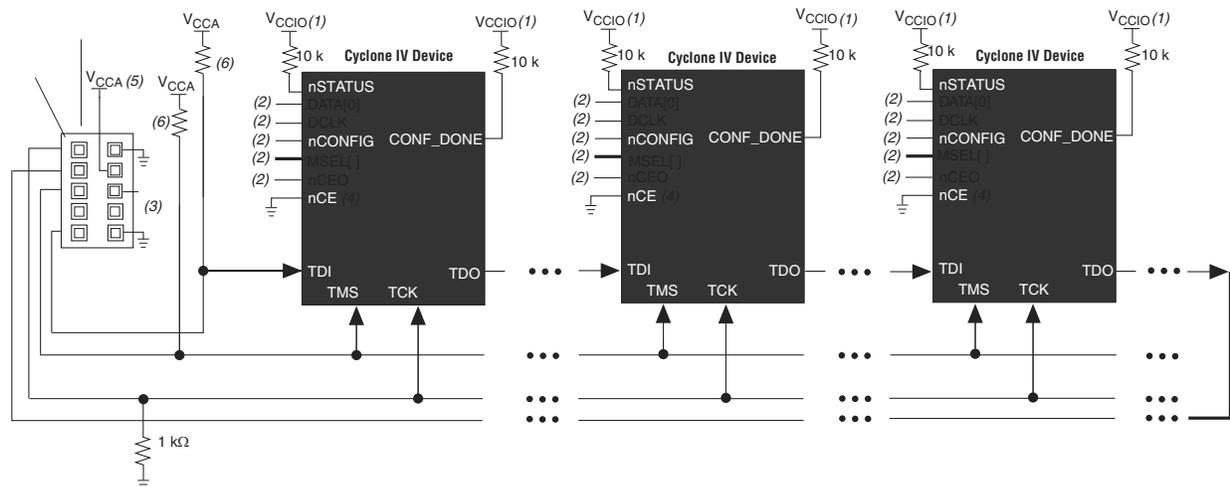
$$9,600,000 \text{ bits} \times \left(\frac{50 \text{ ns}}{1 \text{ bit}} \right) = 480 \text{ ms}$$

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system with JTAG BST circuitry. Figure 8-25 and Figure 8-26 show multi-device JTAG configuration.

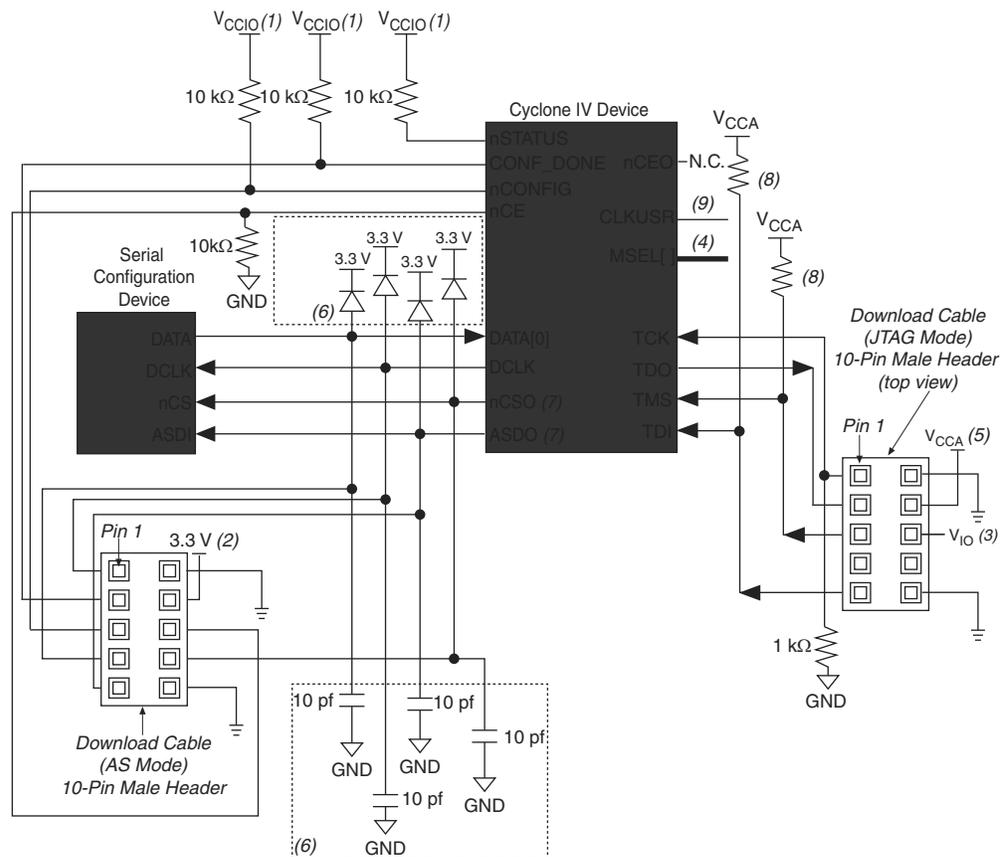
For devices using 2.5-, 3.0-, and 3.3-V V_{CCIO} supply, you must refer to Figure 8-25. All I/O inputs must maintain a maximum AC voltage of 4.1 V because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using 2.5-, 3.0-, and 3.3-V V_{CCIO} supply. You must power up the V_{CC} of the download cable with a 2.5-V V_{CCA} supply. For device using V_{CCIO} of 1.2, 1.5 V, and 1.8 V, refer to Figure 8-26. You can power up the V_{CC} of the download cable with the supply from V_{CCIO} .

Figure 8-25. JTAG Configuration of Multiple Devices Using a Download Cable (2.5, 3.0, and 3.3-V V_{CCIO} Powering the JTAG Pins)



Notes to Figure 8-25:

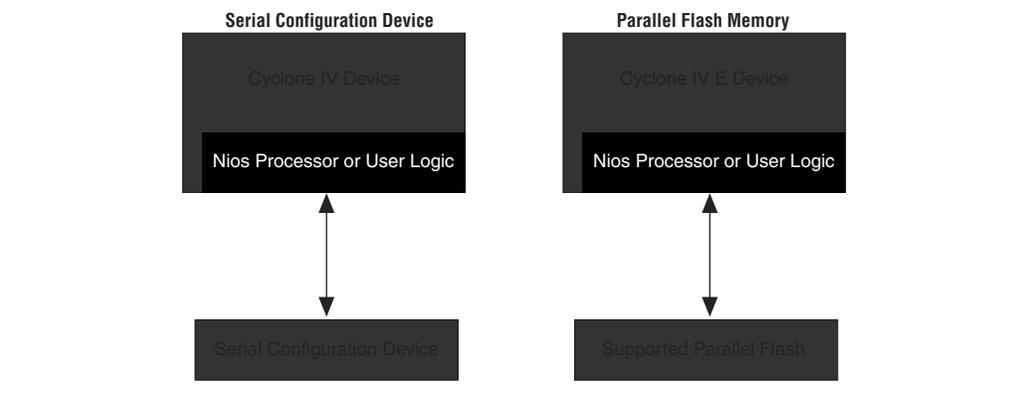
- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Connect the $nCONFIG$ and $nMSEL$ pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the $nCONFIG$ pin to logic-high and the $nMSEL$ pins to GND. In addition, pull $DCLK$ and $DATA[0]$ to either high or low, whichever is convenient on your board.
- (3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) You must connect the nCE pin to GND or driven low for successful JTAG configuration.
- (5) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V supply from V_{CCA} . Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.
- (6) Resistor value can vary from 1 k Ω to 10 k Ω .

Figure 8–28. Combining JTAG and AS Configuration Schemes**Notes to Figure 8–28:**

- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Power up the V_{CC} of the EthernetBlaster, ByteBlaster II, or USB-Blaster cable with the 3.3-V supply.
- (3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. The V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. When using the ByteBlasterMV download cable, this pin is a no connect. When using the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL for AS configuration schemes, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (5) Power up the V_{CC} of the EthernetBlaster, ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V V_{CCA} supply. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.
- (6) You must place the diodes and capacitors as close as possible to the Cyclone IV device. Altera recommends using the Schottky diode, which has a relatively lower forward diode voltage (VF) than the switching and Zener diodes, for effective voltage clamping.
- (7) These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as DATA[1] pin in AP and FPP modes.
- (8) Resistor value can vary from 1 kΩ to 10 kΩ.
- (9) Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK.

Figure 8–31 shows the block diagrams to implement remote system upgrade in Cyclone IV devices.

Figure 8–31. Remote System Upgrade Block Diagrams for AS and AP Configuration Schemes



The MSEL pin setting in the remote system upgrade mode is the same as the standard configuration mode. Standard configuration mode refers to normal Cyclone IV device configuration mode with no support for remote system upgrades (the remote system upgrade circuitry is disabled). When using remote system upgrade in Cyclone IV devices, you must enable the remote update mode option setting in the Quartus II software.

Enabling Remote Update

You can enable or disable remote update for Cyclone IV devices in the Quartus II software before design compilation (in the Compiler Settings menu). To enable remote update in the compiler settings of the project, perform the following steps:

1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.
2. Click **Device and Pin Options**. The **Device and Pin Options** dialog box appears.
3. Click the **Configuration** tab.
4. From the **Configuration Mode** list, select **Remote**.
5. Click **OK**.
6. In the **Settings** dialog box, click **OK**.

Configuration Image Types

When using remote system upgrade, Cyclone IV device configuration bitstreams are classified as factory configuration images or application configuration images. An image, also referred to as a configuration, is a design loaded into the device that performs certain user-defined functions. Each device in your system requires one factory image or with addition of one or more application images. The factory image is a user-defined fall-back or safe configuration and is responsible for administering remote updates with the dedicated circuitry. Application images implement user-defined functionality in the target Cyclone IV device. You can include the default application image functionality in the factory image.

Chapter Revision Dates

The chapters in this document, Cyclone IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

- Chapter 1. Cyclone IV Transceivers Architecture
Revised: *February 2015*
Part Number: *CYIV-52001-3.7*

- Chapter 2. Cyclone IV Reset Control and Power Down
Revised: *September 2014*
Part Number: *CYIV-52002-1.4*

- Chapter 3. Cyclone IV Dynamic Reconfiguration
Revised: *November 2011*
Part Number: *CYIV-52003-2.1*

For example, when operating an EP4CGX150 transmitter channel at 3.125 Gbps without byte serializer, the FPGA fabric frequency is 312.5 MHz (3.125 Gbps/10). This implementation violates the frequency limit and is not supported. Channel operation at 3.125 Gbps is supported when byte serializer is used, where the FPGA fabric frequency is 156.25 MHz (3.125 Gbps/20).

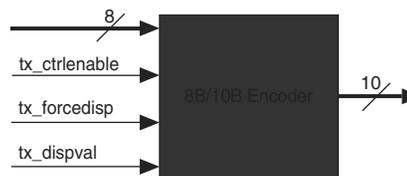
The byte serializer forwards the least significant byte first, followed by the most significant byte.

8B/10B Encoder

The optional 8B/10B encoder generates 10-bit code groups with proper disparity from the 8-bit data and 1-bit control identifier as shown in Figure 1-5.

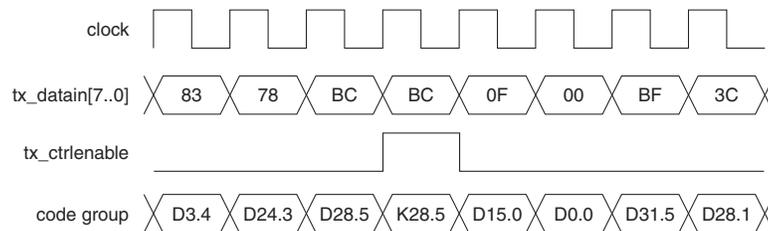
 The encoder is compliant with Clause 36 of the *IEEE 802.3 Specification*.

Figure 1-5. 8B/10B Encoder Block Diagram



The 1-bit control identifier (`tx_ctrlenable`) port controls the 8-bit translation to either a 10-bit data word ($Dx.y$) or a 10-bit control word ($Kx.y$). Figure 1-6 shows the 8B/10B encoding operation with the `tx_ctrlenable` port, where the second 8'hBC data is encoded as a control word when `tx_ctrlenable` port is asserted, while the rest of the data is encoded as a data word.

Figure 1-6. Control and Data Word Encoding with the 8B/10B Encoder



 The IEEE 802.3 8B/10B encoder specification identifies only a set of 8-bit characters for which the `tx_ctrlenable` port should be asserted. If you assert `tx_ctrlenable` port for any other set of characters, the 8B/10B encoder might encode the output 10-bit code as an invalid code (it does not map to a valid $Dx.y$ or $Kx.y$ code), or an unintended valid $Dx.y$ code, depending on the value entered. It is possible for a downstream 8B/10B decoder to decode an invalid control word into a valid $Dx.y$ code without asserting any code error flags. Altera recommends not to assert `tx_ctrlenable` port for unsupported 8-bit characters.

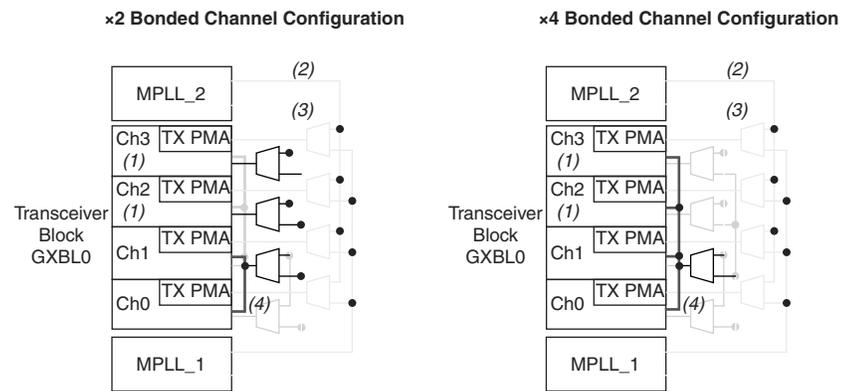
- Programmable equalization—boosts the high-frequency gain of the incoming signal up to 7 dB. This compensates for the low-pass filter effects of the transmission media. The amount of high-frequency gain required depends on the loss characteristics of the physical medium.
- Programmable DC gain—provides equal boost to incoming signal across the frequency spectrum with DC gain settings up to 6 dB.
- Programmable differential OCT—provides calibrated OCT at 100 Ω or 150 Ω with on-chip receiver common mode voltage at 0.82 V. The common mode voltage is tri-stated when you disable the OCT to use external termination.
- Offset cancellation—corrects the analog offset voltages that might exist from process variations between the positive and negative differential signals in the equalizer stage and CDR circuit.
- Signal detection—detects if the signal level present at the receiver input buffer is higher than the threshold with a built-in signal threshold detection circuitry. The circuitry has a hysteresis response that filters out any high-frequency ringing caused by ISI effects or high-frequency losses in the transmission medium. Detection is indicated by the assertion of the `rx_signaldetect` signal. Signal detection is only supported when 8B/10B encoder/decoder block is enabled. When not supported, the `rx_signaldetect` signal is forced high, bypassing the signal detection function.

 Disable OCT to use external termination if the link requires a 85 Ω termination, such as when you are interfacing with certain PCIe Gen1 or Gen2 capable devices.

 For specifications on programmable equalization and DC gain settings, refer to the *Cyclone IV Device Data Sheet*.

Figure 1-36 and Figure 1-37 show the independent high-speed clock and bonded low-speed clock distributions for transceivers in F324 and smaller packages, and in F484 and larger packages in bonded ($\times 2$ and $\times 4$) channel configuration.

Figure 1-36. Clock Distribution in Bonded ($\times 2$ and $\times 4$) Channel Configuration for Transceivers in F324 and Smaller Packages.



Notes to Figure 1-36:

- (1) Transceiver channels 2 and 3 are not available for devices in F169 and smaller packages.
- (2) High-speed clock.
- (3) Low-speed clock.
- (4) Bonded common low-speed clock path.

Table 1–25. PRBS, High and Low Frequency Patterns, and Channel Settings (Part 2 of 2)

Patterns	Polynomial	8-bit Channel Width				10-bit Channel Width			
		Channel Width of 8 bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages	Channel Width of 10-bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages
Low Frequency (2)	1111100000	N	—	—	—	Y	—	2.5	3.125

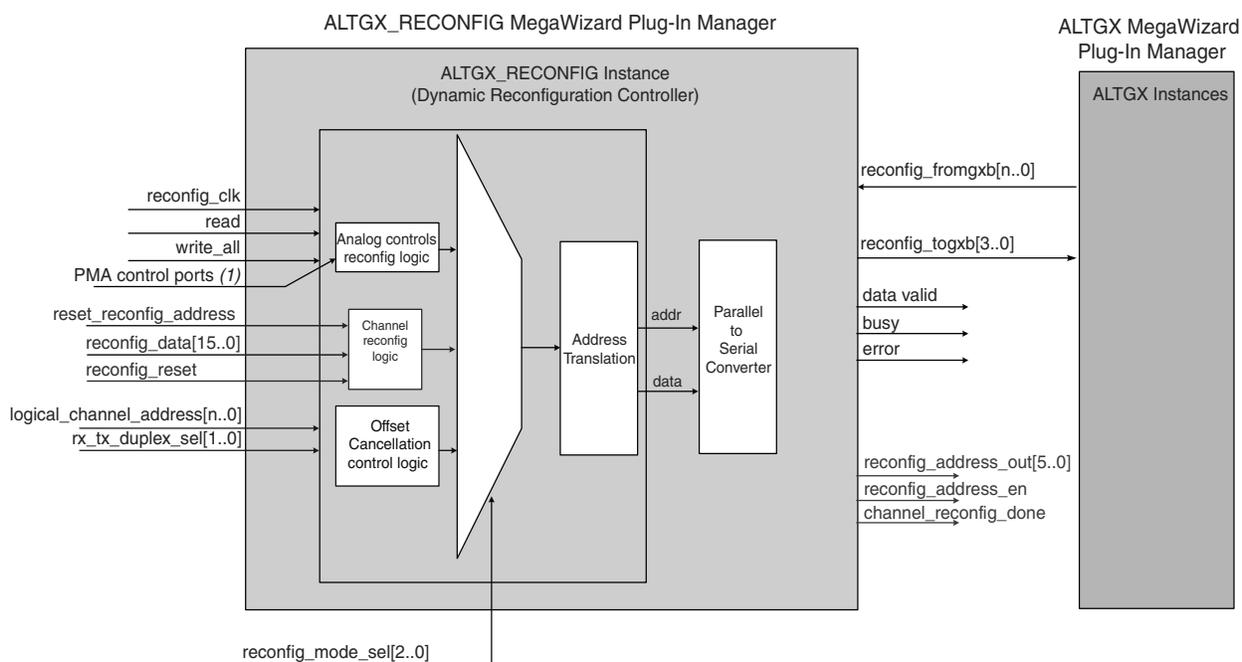
Notes to Table 1–25:

- (1) Channel width refers to the **What is the channel width?** option in the **General** screen of the ALTGX MegaWizard Plug-In Manager. Based on the selection, an 8 or 10 bits wide pattern is generated as indicated by a **Yes (Y)** or **No (N)**.
- (2) A verifier and associated `rx_bistdone` and `rx_bisterr` signals are not available for the specified patterns.

You can enable the serial loopback option to loop the generated PRBS patterns to the receiver channel for verifier to check the PRBS patterns. When the PRBS pattern is received, the `rx_bisterr` and `rx_bistdone` signals indicate the status of the verifier. After the word aligner restores the word boundary, the `rx_bistdone` signal is driven high when the verifier receives a complete pattern cycle and remains asserted until it is reset using the `rx_digitalreset` port. After the assertion of `rx_bistdone`, the `rx_bisterr` signal is asserted for a minimum of three `rx_clkout` cycles when errors are detected in the data and deasserts if the following PRBS sequence contains no error. You can reset the PRBS pattern generator and verifier by asserting the `tx_digitalreset` and `rx_digitalreset` ports, respectively.

Figure 3–1 shows a conceptual view of the dynamic reconfiguration controller architecture. For a detailed description of the inputs and outputs of the ALTGX_RECONFIG instance, refer to “Error Indication During Dynamic Reconfiguration” on page 3–36.

Figure 3–1. Dynamic Reconfiguration Controller



Note to Figure 3–1:

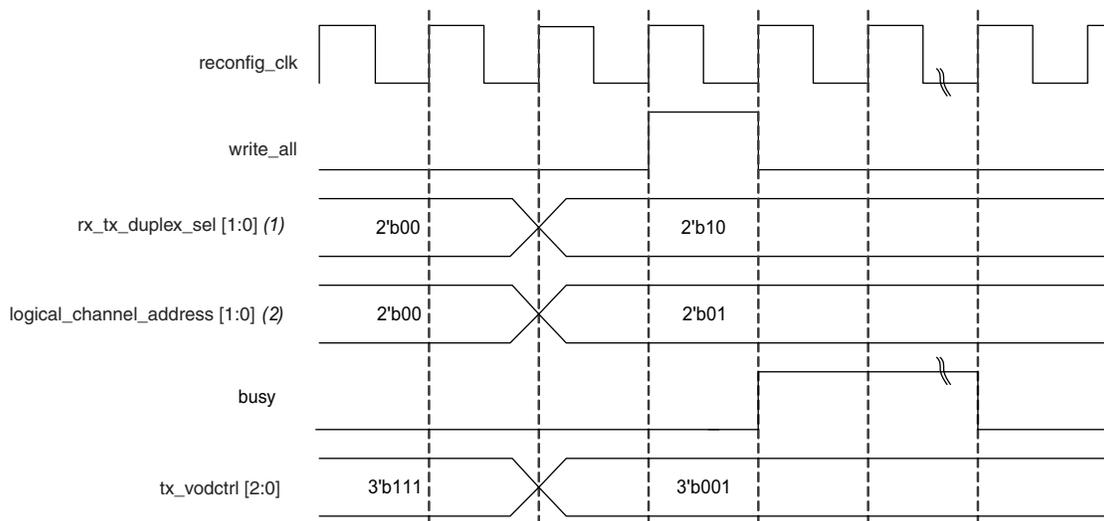
(1) The PMA control ports consist of the V_{OD} , pre-emphasis, DC gain, and manual equalization controls.

 Only PMA reconfiguration mode supports manual equalization controls.

 You can use one ALTGX_RECONFIG instance to control multiple transceiver blocks. However, you cannot use multiple ALTGX_RECONFIG instances to control one transceiver block.

Figure 3-4 shows the write transaction waveform for Method 1.

Figure 3-4. Write Transaction Waveform—Use 'logical_channel_address port' Option



Notes to Figure 3-4:

- (1) In this waveform example, you are writing to only the transmitter portion of the channel.
- (2) In this waveform example, the number of channels connected to the dynamic reconfiguration controller is four. Therefore, the logical_channel_address port is 2 bits wide.

Read Transaction

For example, to read the existing V_{OD} values from the transmit V_{OD} control registers of the transmitter portion of a specific channel controlled by the ALTGX_RECONFIG instance, perform the following steps:

1. Set the logical_channel_address input port to the logical channel address of the transceiver channel whose PMA controls you want to read (for example, tx_vodctrl_out).
2. Set the rx_tx_duplex_sel port to 2'b10 so that only the transmit PMA controls are read from the transceiver channel.
3. Ensure that the busy signal is low before you start a read transaction.
4. Assert the read signal for one reconfig_clk clock cycle. This initiates the read transaction.

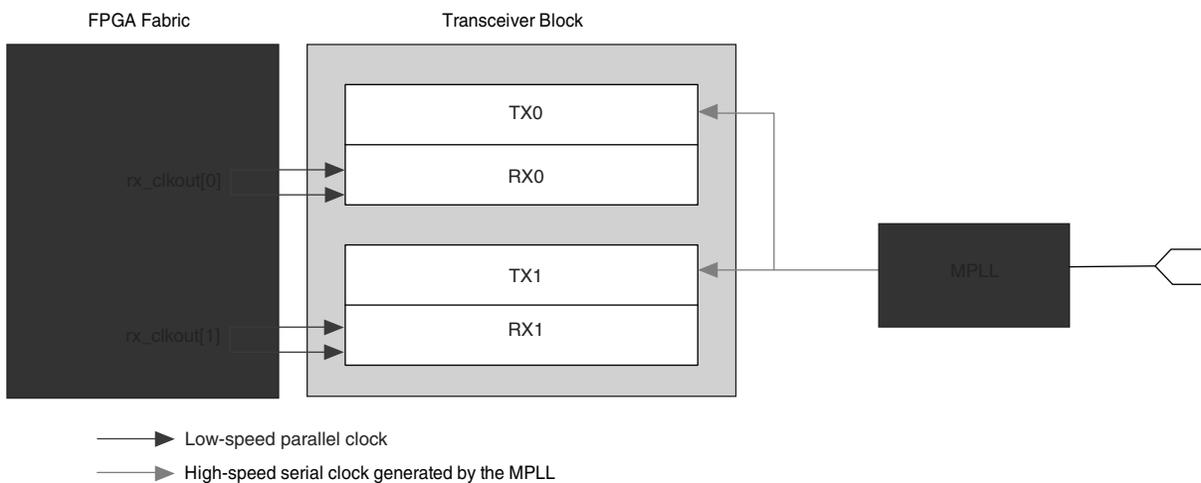
The busy output status signal is asserted high to indicate that the dynamic reconfiguration controller is busy reading the PMA control values. When the read transaction has completed, the busy signal goes low. The data_valid signal is asserted to indicate that the data available at the read control signal is valid.

Option 3: Use the Respective Channel Receiver Core Clocks

- Enable this option if you want the individual channel's rx_clkout signal to provide the read clock to its respective Receive Phase Compensation FIFO.
- This option is typically enabled when the channel is reconfigured from a Basic or Protocol configuration with or without rate matching to another Basic or Protocol configuration with or without rate matching.

Figure 3–15 shows the respective rx_clkout of each channel clocking the respective receiver channels of a transceiver block.

Figure 3–15. Option 3 for Receiver Core Clocking (Channel Reconfiguration Mode)



PLL Reconfiguration Mode

Cyclone IV GX device support the PLL reconfiguration support through the ALTPLL_RECONFIG MegaWizard. You can use this mode to reconfigure the multipurpose PLL or general purpose PLL used to clock the transceiver channel without affecting the remaining blocks of the channel. When you reconfigure the multipurpose PLL or general purpose PLL of a transceiver block to run at a different data rate, all the transceiver channels listening to this multipurpose PLL or general purpose PLL also get reconfigured to the new data rate. Channel settings are not affected. When you reconfigure the multipurpose PLL or general purpose PLL to support a different data rate, you must ensure that the functional mode of the transceiver channel supports the reconfigured data rate.

The PLL reconfiguration mode can be enabled by selecting the **Enable PLL Reconfiguration** option in the ALTGX MegaWizard under **Reconfiguration Setting** tab. For multipurpose PLL or general purpose PLL reconfiguration, .mif files are required to dynamically reconfigure the PLL setting in order to change the output frequency of the transceiver PLL to support different data rates.

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