

Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

| | |
|--------------------------------|---|
| Product Status | Active |
| Number of LABs/CLBs | 392 |
| Number of Logic Elements/Cells | 6272 |
| Total RAM Bits | 276480 |
| Number of I/O | 91 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP Exposed Pad |
| Supplier Device Package | 144-EQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep4ce6e22c8 |

1. Cyclone IV FPGA Device Family Overview

CYIV-51001-2.0

Altera's new Cyclone® IV FPGA device family extends the Cyclone FPGA series leadership in providing the market's lowest-cost, lowest-power FPGAs, now with a transceiver variant. Cyclone IV devices are targeted to high-volume, cost-sensitive applications, enabling system designers to meet increasing bandwidth requirements while lowering costs.

Built on an optimized low-power process, the Cyclone IV device family offers the following two variants:

- Cyclone IV E—lowest power, high functionality with the lowest cost
- Cyclone IV GX—lowest power and lowest cost FPGAs with 3.125 Gbps transceivers



Cyclone IV E devices are offered in core voltage of 1.0 V and 1.2 V.



For more information, refer to the *Power Requirements for Cyclone IV Devices* chapter.

Providing power and cost savings without sacrificing performance, along with a low-cost integrated transceiver option, Cyclone IV devices are ideal for low-cost, small-form-factor applications in the wireless, wireline, broadcast, industrial, consumer, and communications industries.

Cyclone IV Device Family Features

The Cyclone IV device family offers the following features:

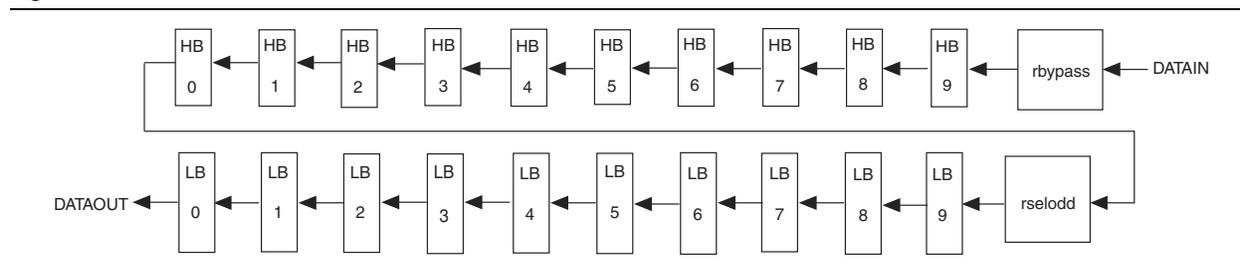
- Low-cost, low-power FPGA fabric:
 - 6K to 150K logic elements
 - Up to 6.3 Mb of embedded memory
 - Up to 360 18 × 18 multipliers for DSP processing intensive applications
 - Protocol bridging applications for under 1.5 W total power

© 2016 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.



Figure 5–25 shows the scan chain bit order sequence for one PLL post-scale counter in PLLs of Cyclone IV devices.

Figure 5–25. Scan Chain Bit Order



Charge Pump and Loop Filter

You can reconfigure the charge pump and loop filter settings to update the PLL bandwidth in real time. Table 5–8 through Table 5–10 list the possible settings for charge pump current (I_{CP}), loop filter resistor (R), and capacitor (C) values for PLLs of Cyclone IV devices.

Table 5–8. Charge Pump Bit Control

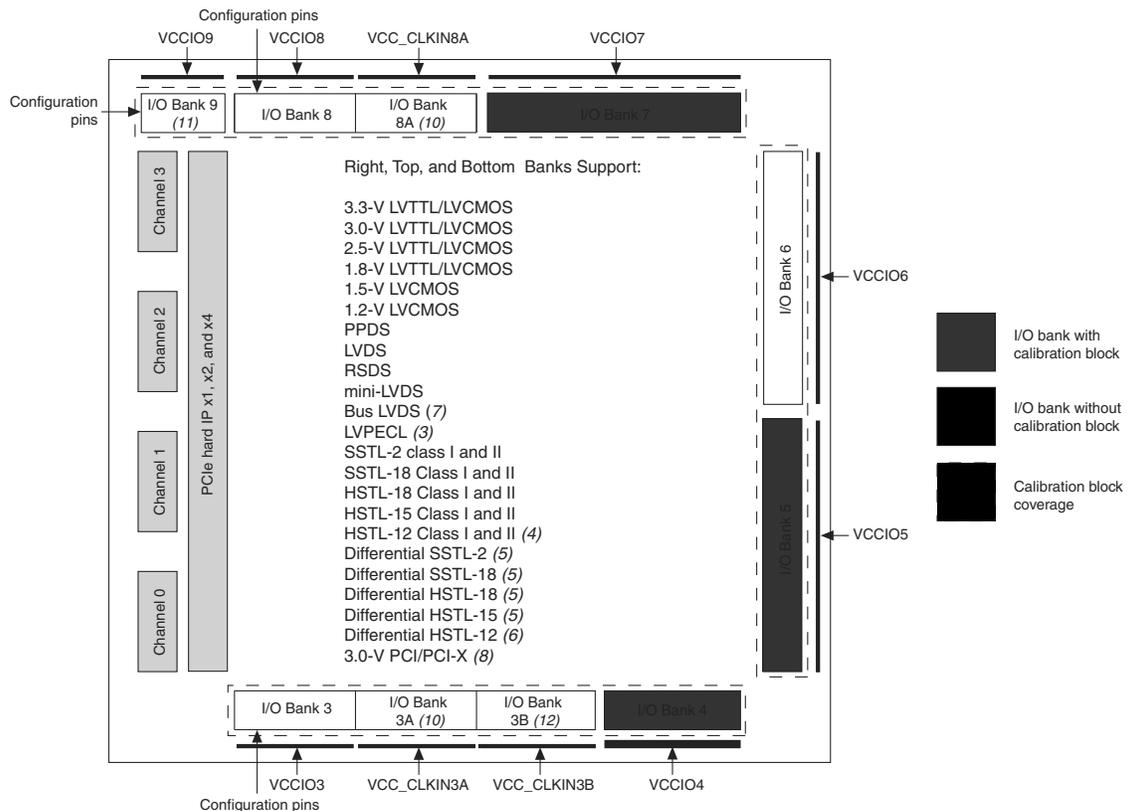
| CP[2] | CP[1] | CP[0] | Setting (Decimal) |
|-------|-------|-------|-------------------|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 3 |
| 1 | 1 | 1 | 7 |

Table 5–9. Loop Filter Resistor Value Control

| LFR[4] | LFR[3] | LFR[2] | LFR[1] | LFR[0] | Setting (Decimal) |
|--------|--------|--------|--------|--------|-------------------|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 0 | 0 | 16 |
| 1 | 0 | 0 | 1 | 1 | 19 |
| 1 | 0 | 1 | 0 | 0 | 20 |
| 1 | 1 | 0 | 0 | 0 | 24 |
| 1 | 1 | 0 | 1 | 1 | 27 |
| 1 | 1 | 1 | 0 | 0 | 28 |
| 1 | 1 | 1 | 1 | 0 | 30 |

Figure 6–10 and Figure 6–11 show the overview of Cyclone IV GX I/O banks.

Figure 6–10. Cyclone IV GX I/O Banks for EP4CGX15, EP4CGX22, and EP4CGX30 (1), (2), (9)



Notes to Figure 6–10:

- (1) This is a top view of the silicon die. For exact pin locations, refer to the pin list and the Quartus II software. Channels 2 and 3 are not available in EP4CGX15 and F169 package type in EP4CGX22 and EP4CGX30 devices.
- (2) True differential (PPDS, LVDS, mini-LVDS, and RSQS I/O standards) outputs are supported in row I/O banks 5 and 6 only. External resistors are needed for the differential outputs in column I/O banks.
- (3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
- (4) The HSTL-12 Class II is supported in column I/O banks 4, 7, and 8.
- (5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.
- (6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 4, 7, and 8.
- (7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses the LVDS input buffer.
- (8) The PCI-X I/O standard does not meet the IV curve requirement at the linear region.
- (9) The OCT block is located in the shaded banks 4, 5, and 7.
- (10) There are two dedicated clock input I/O banks (I/O bank 3A and I/O bank 8A) that can be used for either high-speed serial interface (HSSI) input reference clock pins or clock input pins.
- (11) There are dual-purpose I/O pins in bank 9. If input pins with V_{REF} I/O standards are used on these dual-purpose I/O pins during user mode, they share the V_{REF} pin in bank 8. These dual-purpose IO pins in bank 9 when used in user mode also support R_S OCT without calibration and they share the OCT block with bank 8.
- (12) There are four dedicated clock input in I/O bank 3B for the EP4CGX30F484 device that can be used for either HSSI input reference clock pins or clock input pins.

Table 6-7. Differential I/O Standards Supported in Cyclone IV GX I/O Banks

| Differential I/O Standards | I/O Bank Location | External Resistor Network at Transmitter | Transmitter (TX) | Receiver (RX) |
|-------------------------------------|-------------------|--|------------------|---------------|
| LVDS | 5,6 | Not Required | ✓ | ✓ |
| | 3,4,5,6,7,8 | Three Resistors | | |
| RSDS | 5,6 | Not Required | ✓ | — |
| | 3,4,7,8 | Three Resistors | | |
| | 3,4,5,6,7,8 | Single Resistor | | |
| mini-LVDS | 5,6 | Not Required | ✓ | — |
| | 3,4,5,6,7,8 | Three Resistors | | |
| PPDS | 5,6 | Not Required | ✓ | — |
| | 3,4,5,6,7,8 | Three Resistors | | |
| BLVDS ⁽¹⁾ | 3,4,5,6,7,8 | Single Resistor | ✓ | ✓ |
| LVPECL ⁽²⁾ | 3,4,5,6,7,8 | — | — | ✓ |
| Differential SSTL-2 ⁽³⁾ | 3,4,5,6,7,8 | — | ✓ | ✓ |
| Differential SSTL-18 ⁽³⁾ | 3,4,5,6,7,8 | — | ✓ | ✓ |
| Differential HSTL-18 ⁽³⁾ | 3,4,5,6,7,8 | — | ✓ | ✓ |
| Differential HSTL-15 ⁽³⁾ | 3,4,5,6,7,8 | — | ✓ | ✓ |
| Differential HSTL-12 ⁽³⁾ | 4,5,6,7,8 | — | ✓ | ✓ |

Notes to Table 6-7:

- (1) Transmitter and Receiver f_{MAX} depend on system topology and performance requirement.
- (2) The LVPECL I/O standard is only supported on dedicated clock input pins.
- (3) The differential SSTL-2, SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards are only supported on clock input pins and PLL output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

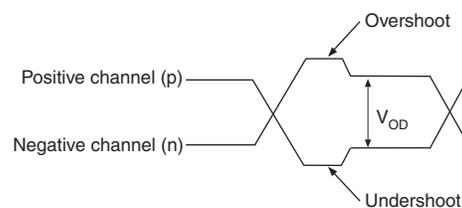
You can use I/O pins and internal logic to implement a high-speed differential interface in Cyclone IV devices. Cyclone IV devices do not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal phase-locked loops (PLLs), and I/O cells are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data. The differential interface data serializers and deserializers (SERDES) are automatically constructed in the core logic elements (LEs) with the Quartus II software ALTLVDS megafunction.

before the next edge; this may lead to pattern-dependent jitter. With pre-emphasis, the output current is momentarily boosted during switching to increase the output slew rate. The overshoot produced by this extra switching current is different from the overshoot caused by signal reflection. This overshoot happens only during switching, and does not produce ringing.

The Quartus II software allows two settings for programmable pre-emphasis control—**0** and **1**, in which **0** is pre-emphasis off and **1** is pre-emphasis on. The default setting is **1**. The amount of pre-emphasis needed depends on the amplification of the high-frequency components along the transmission line. You must adjust the setting to suit your designs, as pre-emphasis decreases the amplitude of the low-frequency component of the output signal.

Figure 6–20 shows the differential output signal with pre-emphasis.

Figure 6–20. The Output Signal with Pre-Emphasis



High-Speed I/O Timing

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Cyclone IV devices. Timing for source-synchronous signaling is based on skew between the data and clock signals.

High-speed differential data transmission requires timing parameters provided by IC vendors and requires you to consider the board skew, cable skew, and clock jitter. This section provides information about high-speed I/O standards timing parameters in Cyclone IV devices.

Table 6–11 defines the parameters of the timing diagram shown in Figure 6–21.

Table 6–11. High-Speed I/O Timing Definitions (Part 1 of 2)

| Parameter | Symbol | Description |
|--|--------|---|
| Transmitter channel-to-channel skew ⁽¹⁾ | TCCS | The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement. |
| Sampling window | SW | The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. $T_{SW} = T_{SU} + T_{hd} + \text{PLL jitter}$. |
| Time unit interval | TUI | The TUI is the data-bit timing budget allowed for skew, propagation delays, and data sampling window. |
| Receiver input skew margin | RSKM | RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: $\text{RSKM} = \frac{\text{TUI} - \text{SW} - \text{TCCS}}{2}$ |

Table 6-12. Document Revision History (Part 2 of 2)

| Date | Version | Changes |
|---------------|---------|---|
| February 2010 | 2.0 | <ul style="list-style-type: none"> ■ Added Cyclone IV E devices information for the Quartus II software version 9.1 SP1 release. ■ Updated Table 6-2, Table 6-3, and Table 6-10. ■ Updated “I/O Banks” section. ■ Added Figure 6-9. ■ Updated Figure 6-10 and Figure 6-11. ■ Added Table 6-4, Table 6-6, and Table 6-8. |
| November 2009 | 1.0 | Initial release. |

- “FPP Configuration” on page 8-40
- “JTAG Configuration” on page 8-45
- “Device Configuration Pins” on page 8-62

Configuration Features

Table 8-1 lists the configuration methods you can use in each configuration scheme.

Table 8-1. Configuration Features in Cyclone IV Devices

| Configuration Scheme | Configuration Method | Decompression | Remote System Upgrade ⁽¹⁾ |
|--------------------------|---------------------------------------|---------------|--------------------------------------|
| AS | Serial Configuration Device | ✓ | ✓ |
| AP | Supported Flash Memory ⁽²⁾ | — | ✓ |
| PS | External Host with Flash Memory | ✓ | ✓ ⁽³⁾ |
| | Download Cable | ✓ | — |
| FPP | External Host with Flash Memory | — | ✓ ⁽³⁾ |
| JTAG based configuration | External Host with Flash Memory | — | — |
| | Download Cable | — | — |

Notes to Table 8-1:

- (1) Remote update mode is supported when you use the Remote System Upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus® II software.
- (2) For more information about the supported device families for the Micron commodity parallel flash, refer to Table 8-10 on page 8-22.
- (3) Remote update mode is supported externally using the Parallel Flash Loader (PFL) with the Quartus II software.

Configuration Data Decompression

Cyclone IV devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and send the compressed bitstream to Cyclone IV devices. During configuration, Cyclone IV devices decompress the bitstream in real time and program the SRAM cells.

 Compression may reduce the configuration bitstream size by 35 to 55%.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time required to send the bitstream to the Cyclone IV device. The time required by a Cyclone IV device to decompress a configuration file is less than the time required to send the configuration data to the device. There are two methods for enabling compression for the Cyclone IV device bitstreams in the Quartus II software:

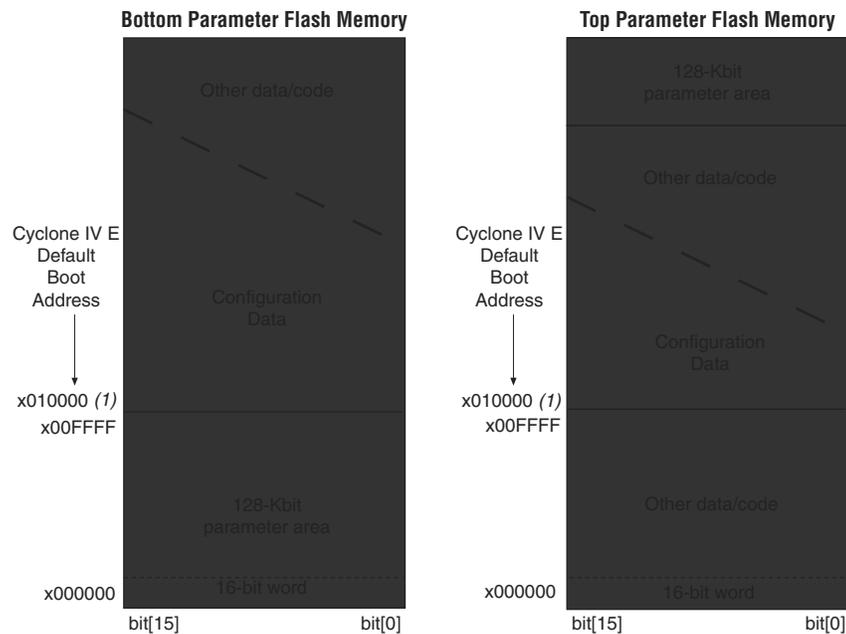
- Before design compilation (through the Compiler Settings menu)
- After design compilation (through the **Convert Programming Files** dialog box)

To enable compression in the compiler settings of the project in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.
2. Click **Device and Pin Options**. The **Device and Pin Options** dialog box appears.

The default configuration boot address allows the system to use special parameter blocks in the flash memory map. Parameter blocks are at the top or bottom of the memory map. Figure 8–12 shows the configuration boot address in the AP configuration scheme. You can change the default configuration default boot address 0×010000 to any desired address using the `APFC_BOOT_ADDR` JTAG instruction. For more information about the `APFC_BOOT_ADDR` JTAG instruction, refer to “JTAG Instructions” on page 8–57.

Figure 8–12. Configuration Boot Address in AP Flash Memory Map



Note to Figure 8–12:

(1) The default configuration boot address is $x010000$ when represented in 16-bit word addressing.

PS Configuration

You can perform PS configuration on Cyclone IV devices with an external intelligent host, such as a MAX[®] II device, microprocessor with flash memory, or a download cable. In the PS scheme, an external host controls the configuration. Configuration data is clocked into the target Cyclone IV device through `DATA[0]` at each rising edge of `DCLK`.

If your system already contains a common flash interface (CFI) flash memory, you can use it for Cyclone IV device configuration storage as well. The MAX II PFL feature provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control the configuration from the flash memory device to the Cyclone IV device.



For more information about the PFL, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.



Cyclone IV devices do not support enhanced configuration devices for PS configuration.

FPP Configuration

The FPP configuration in Cyclone IV devices is designed to meet the increasing demand for faster configuration time. Cyclone IV devices are designed with the capability of receiving byte-wide configuration data per clock cycle.

You can perform FPP configuration of Cyclone IV devices with an intelligent host, such as a MAX II device or microprocessor with flash memory. If your system already contains a CFI flash memory, you can use it for the Cyclone IV device configuration storage as well. The MAX II PFL feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone IV device.

-  For more information about the PFL, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.
-  FPP configuration is supported in EP4CGX30 (only for F484 package), EP4CGX50, EP4CGX75, EP4CGX110, EP4CGX150, and all Cyclone IV E devices.
-  The FPP configuration is not supported in E144 package of Cyclone IV E devices.
-  Cyclone IV devices do not support enhanced configuration devices for FPP configuration.

FPP Configuration Using an External Host

FPP configuration using an external host provides a fast method to configure Cyclone IV devices. In the FPP configuration scheme, you can use an external host device to control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone IV device. You can store configuration data in an **.rbf**, **.hex**, or **.ttf** format. When using the external host, a design that controls the configuration process, such as fetching the data from flash memory and sending it to

- In AP configuration scheme, the only way to re-engage the AP controller is to issue the `ACTIVE_ENGAGE` instruction. In this case, asserting the `nCONFIG` pin does not re-engage either active controller.

ACTIVE_ENGAGE

The `ACTIVE_ENGAGE` instruction allows you to re-engage a disengaged active controller. You can issue this instruction any time during configuration or user mode to re-engage an already disengaged active controller, as well as trigger reconfiguration of the Cyclone IV device in the active configuration scheme.

The `ACTIVE_ENGAGE` instruction functions as the `PULSE_NCONFIG` instruction when the device is in the PS or FPP configuration schemes. The `nCONFIG` pin is disabled when the `ACTIVE_ENGAGE` instruction is issued.

 Altera does not recommend using the `ACTIVE_ENGAGE` instruction, but it is provided as a fail-safe instruction for re-engaging the active configuration controller (AS and AP).

Overriding the Internal Oscillator

This feature allows you to override the internal oscillator during the active configuration scheme. The AS and AP configuration controllers use the internal oscillator as the clock source. You can change the clock source to `CLKUSR` through the JTAG instruction.

The `EN_ACTIVE_CLK` and `DIS_ACTIVE_CLK` JTAG instructions toggle on or off whether or not the active clock is sourced from the `CLKUSR` pin or the internal configuration oscillator. To source the active clock from the `CLKUSR` pin, issue the `EN_ACTIVE_CLK` instruction. This causes the `CLKUSR` pin to become the active clock source. When using the `EN_ACTIVE_CLK` instruction, you must enable the internal oscillator for the clock change to occur. By default, the configuration oscillator is disabled after configuration and initialization is complete as well as the device has entered user mode.

However, the internal oscillator is enabled in user mode by any of the following conditions:

- A reconfiguration event (for example, driving the `nCONFIG` pin to go low)
- Remote update is enabled
- Error detection is enabled

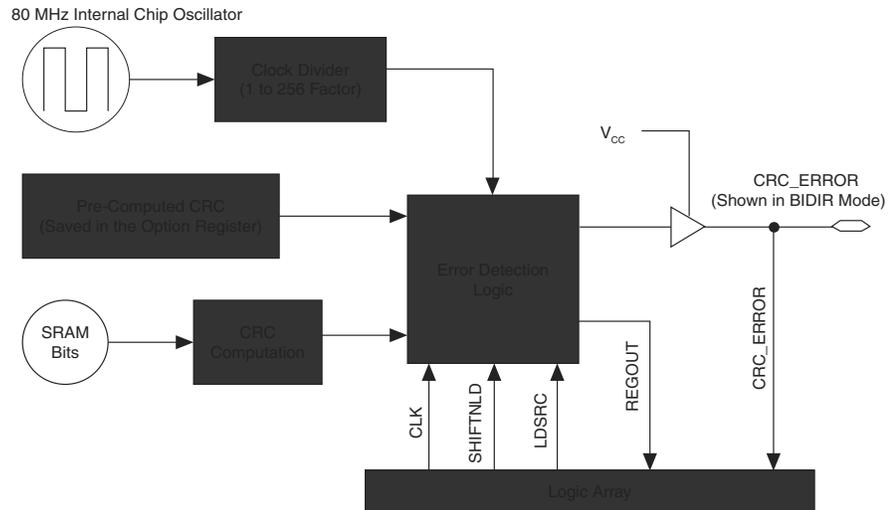
 When using the `EN_ACTIVE_CLK` and `DIS_ACTIVE_CLK` JTAG instructions to override the internal oscillator, you must clock the `CLKUSR` pin at two times the expected `DCLK` frequency. The `CLKUSR` pin allows a maximum frequency of 40 MHz (40 MHz `DCLK`).

Normally, a test instrument uses the `CLKUSR` pin when it wants to drive its own clock to control the AS state machine.

To revert the clock source back to the configuration oscillator, issue the `DIS_ACTIVE_CLK` instruction. After you issue the `DIS_ACTIVE_CLK` instruction, you must continue to clock the `CLKUSR` pin for 10 clock cycles. Otherwise, even toggling the `nCONFIG` pin does not revert the clock source and reconfiguration does not occur. A POR reverts the clock source back to the configuration oscillator. Toggling the `nCONFIG` pin or driving the JTAG state machine to reset state does not revert the clock source.

Figure 9-3 shows the error detection block diagram in FPGA devices and shows the interface that the WYSIWYG atom enables in your design.

Figure 9-3. Error Detection Block Diagram



 The user logic is affected by the soft error failure, so reading out the 32-bit CRC signature through the `regout` should not be relied upon to detect a soft error. You should rely on the `CRC_ERROR` output signal itself, because this `CRC_ERROR` output signal cannot be affected by a soft error.

To enable the `cycloneiv_crcblock` WYSIWYG atom, you must name the atom for each Cyclone IV device accordingly.

Example 9-1 shows an example of how to define the input and output ports of a WYSIWYG atom in a Cyclone IV device.

Example 9-1. Error Detection Block Diagram

```
cycloneiv_crcblock<crcblock_name>
(
  .clk(<clock source>),
  .shiftnld(<shiftnld source>),
  .ldsrc(<ldsrc source>),
  .crcerror(<crcerror out destination>),
  .regout(<output destination>),
);
```

Table 10-1. Boundary-Scan Register Length for Cyclone IV Devices (Part 2 of 2)

| Device | Boundary-Scan Register Length |
|-----------|-------------------------------|
| EP4CGX75 | 1006 |
| EP4CGX110 | 1495 |
| EP4CGX150 | 1495 |

Note to Table 10-1:

(1) For the F484 package of the EP4CGX30 device, the boundary-scan register length is 1006.

Table 10-2 lists the IDCODE information for Cyclone IV devices.

Table 10-2. IDCODE Information for 32-Bit Cyclone IV Devices

| Device | IDCODE (32 Bits) ⁽¹⁾ | | | |
|-------------------------|---------------------------------|-----------------------|---------------------------------|----------------------------|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | LSB (1 Bit) ⁽²⁾ |
| EP4CE6 | 0000 | 0010 0000 1111 0001 | 000 0110 1110 | 1 |
| EP4CE10 | 0000 | 0010 0000 1111 0001 | 000 0110 1110 | 1 |
| EP4CE15 | 0000 | 0010 0000 1111 0010 | 000 0110 1110 | 1 |
| EP4CE22 | 0000 | 0010 0000 1111 0011 | 000 0110 1110 | 1 |
| EP4CE30 | 0000 | 0010 0000 1111 0100 | 000 0110 1110 | 1 |
| EP4CE40 | 0000 | 0010 0000 1111 0100 | 000 0110 1110 | 1 |
| EP4CE55 | 0000 | 0010 0000 1111 0101 | 000 0110 1110 | 1 |
| EP4CE75 | 0000 | 0010 0000 1111 0110 | 000 0110 1110 | 1 |
| EP4CE115 | 0000 | 0010 0000 1111 0111 | 000 0110 1110 | 1 |
| EP4CGX15 | 0000 | 0010 1000 0000 0001 | 000 0110 1110 | 1 |
| EP4CGX22 | 0000 | 0010 1000 0001 0010 | 000 0110 1110 | 1 |
| EP4CGX30 ⁽³⁾ | 0000 | 0010 1000 0000 0010 | 000 0110 1110 | 1 |
| EP4CGX30 ⁽⁴⁾ | 0000 | 0010 1000 0010 0011 | 000 0110 1110 | 1 |
| EP4CGX50 | 0000 | 0010 1000 0001 0011 | 000 0110 1110 | 1 |
| EP4CGX75 | 0000 | 0010 1000 0000 0011 | 000 0110 1110 | 1 |
| EP4CGX110 | 0000 | 0010 1000 0001 0100 | 000 0110 1110 | 1 |
| EP4CGX150 | 0000 | 0010 1000 0000 0100 | 000 0110 1110 | 1 |

Notes to Table 10-2:

- (1) The MSB is on the left.
- (2) The IDCODE LSB is always 1.
- (3) The IDCODE is applicable for all packages except for the F484 package.
- (4) The IDCODE is applicable for the F484 package only.

IEEE Std.1149.6 mandates the addition of two new instructions: EXTEST_PULSE and EXTEST_TRAIN. These two instructions enable edge-detecting behavior on the signal path containing the AC pins.

1. Cyclone IV Transceivers Architecture

CYIV-52001-3.7

Cyclone® IV GX devices include up to eight full-duplex transceivers at serial data rates between 600 Mbps and 3.125 Gbps in a low-cost FPGA. Table 1–1 lists the supported Cyclone IV GX transceiver channel serial protocols.

Table 1–1. Serial Protocols Supported by the Cyclone IV GX Transceiver Channels

| Protocol | Data Rate (Gbps) | F324 and smaller packages | F484 and larger packages |
|--|-----------------------------------|---------------------------|--------------------------|
| PCI Express® (PCIe®) (1) | 2.5 | ✓ | ✓ |
| Gbps Ethernet (GbE) | 1.25 | ✓ | ✓ |
| Common Public Radio Interface (CPRI) | 0.6144, 1.2288, 2.4576, and 3.072 | ✓ (2) | ✓ |
| OBSAI | 0.768, 1.536, and 3.072 | ✓ (2) | ✓ |
| XAUI | 3.125 | — | ✓ |
| Serial digital interface (SDI) | HD-SDI at 1.485 and 1.4835 | ✓ | ✓ |
| | 3G-SDI at 2.97 and 2.967 | — | |
| Serial RapidIO® (SRIO) | 1.25, 2.5, and 3.125 | — | ✓ |
| Serial Advanced Technology Attachment (SATA) | 1.5 and 3.0 | — | ✓ |
| V-by-one | 3.125 | — | ✓ |
| Display Port | 1.62 and 2.7 | — | ✓ |

Notes to Table 1–1:

- (1) Provides the physical interface for PCI Express (PIPE)-compliant interface that supports Gen1 ×1, ×2, and ×4 initial lane width configurations. When implementing ×1 or ×2 interface, remaining channels in the transceiver block are available to implement other protocols.
- (2) Supports data rates up to 2.5 Gbps only.

You can implement these protocols through the ALTGX MegaWizard™ Plug-In Manager, which also offers the highly flexible Basic functional mode to implement proprietary serial protocols at the following serial data rates:

- 600 Mbps to 2.5 Gbps for devices in F324 and smaller packages
- 600 Mbps to 3.125 Gbps for devices in F484 and larger packages

For descriptions of the ports available when instantiating a transceiver using the ALTGX megafunction, refer to “Transceiver Top-Level Port Lists” on page 1–85.



For more information about Cyclone IV transceivers that run at ≥2.97 Gbps data rate, refer to the *Cyclone IV Device Family Pin Connection Guidelines*.

© 2015 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

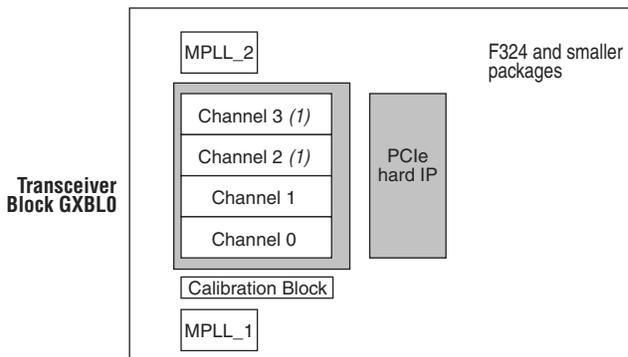


 The Cyclone IV GX device includes a hard intellectual property (IP) implementation of the PCIe MegaCore® functions, supporting Gen1 ×1, ×2, and ×4 initial lane widths configured in the root port or endpoint mode. For more information, refer to “PCI-Express Hard IP Block” on page 1-46.

Transceiver Architecture

Cyclone IV GX devices offer either one or two transceiver blocks per device, depending on the package. Each block consists of four full-duplex (transmitter and receiver) channels, located on the left side of the device (in a die-top view). Figure 1-1 and Figure 1-2 show the die-top view of the transceiver block and related resource locations in Cyclone IV GX devices.

Figure 1-1. F324 and Smaller Packages with Transceiver Channels for Cyclone IV GX Devices



Note to Figure 1-1:

(1) Channel 2 and Channel 3 are not available in the F169 and smaller packages.

Transmitter Channel Datapath

The following sections describe the Cyclone IV GX transmitter channel datapath architecture as shown in Figure 1-3:

- TX Phase Compensation FIFO
- Byte Serializer
- 8B/10B Encoder
- Serializer
- Transmitter Output Buffer

TX Phase Compensation FIFO

The TX phase compensation FIFO compensates for the phase difference between the low-speed parallel clock and the FPGA fabric interface clock, when interfacing the transmitter channel to the FPGA fabric (directly or through the PIPE and PCIe hard IP). The FIFO is four words deep, with latency between two to three parallel clock cycles. Figure 1-4 shows the TX phase compensation FIFO block diagram.

Figure 1-4. TX Phase Compensation FIFO Block Diagram



Note to Figure 1-4:

(1) The x refers to the supported 8-, 10-, 16-, or 20-bits transceiver channel width.

-  The FIFO can operate in registered mode, contributing to only one parallel clock cycle of latency in Deterministic Latency functional mode. For more information, refer to “Deterministic Latency Mode” on page 1-73.
-  For more information about FIFO clocking, refer to “FPGA Fabric-Transceiver Interface Clocking” on page 1-43.

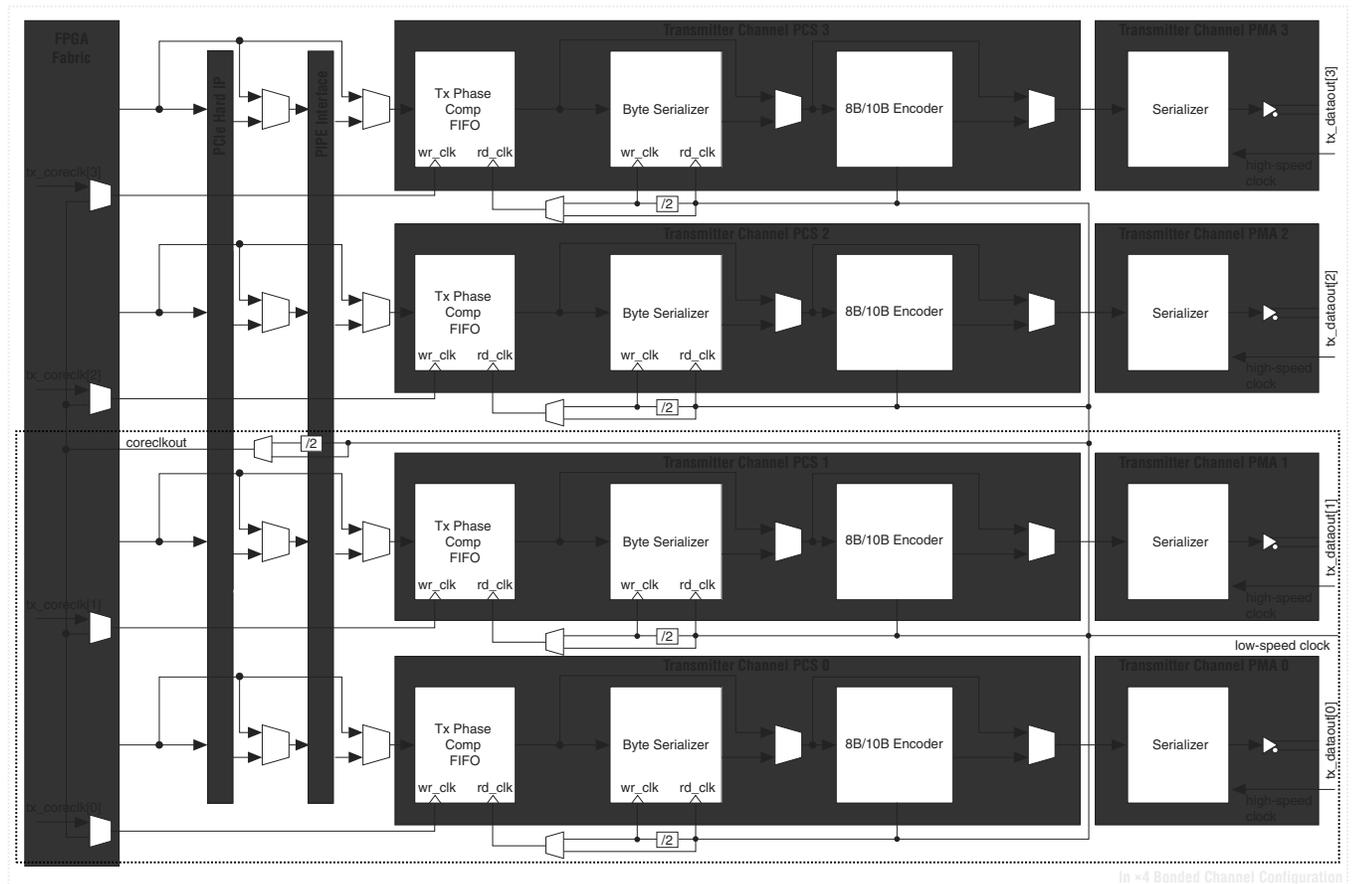
Byte Serializer

The byte serializer divides the input datapath width by two to allow transmitter channel operation at higher data rates while meeting the maximum FPGA fabric frequency limit. This module is required in configurations that exceed the maximum FPGA fabric-transceiver interface clock frequency limit and optional in configurations that do not.

-  For the FPGA fabric-transceiver interface frequency specifications, refer to the *Cyclone IV Device Data Sheet*.

When the byte serializer is enabled, the common bonded low-speed clock frequency is halved before feeding to the read clock of TX phase compensation FIFO. The common bonded low-speed clock is available in FPGA fabric as `coreclkout` port, which can be used in FPGA fabric to send transmitter data and control signals to the bonded channels.

Figure 1-38. Transmitter Only Datapath Clocking in Bonded Channel Configuration



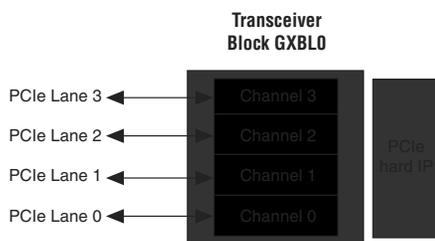
 Bonded channel configuration is not available for Receiver Only channel operation because each of the channels are individually clocked by its recovered clock.

The hard IP block supports 1, 2, or 4 initial lane configurations with a maximum payload of 256 bytes at Gen1 frequency. The application interface is 64 bits with a data width of 16 bits per channel running at up to 125 MHz. As a hard macro and a verified block, it uses very few FPGA resources, while significantly reducing design risk and the time required to achieve timing closure. It is compliant with the PCI Express Base Specification 1.1. You do not have to pay a licensing fee to use this module. Configuring the hard IP block requires using the PCI Express Compiler.

For more information about the hard IP block, refer to the *PCI Express Compiler User Guide*.

Figure 1-43 shows the lane placement requirements when implementing PCIe with hard IP block.

Figure 1-43. PCIe with Hard IP Block Lane Placement Requirements ⁽¹⁾



Note to Figure 1-43:

(1) Applicable for PCIe x1, x2, and x4 implementations with hard IP blocks only.

Transceiver Functional Modes

The Cyclone IV GX transceiver supports the functional modes as listed in Table 1-14 for protocol implementation.

Table 1-14. Transceiver Functional Modes for Protocol Implementation (Part 1 of 2)

| Functional Mode | Protocol | Key Feature | Reference |
|--------------------|---|--|--|
| Basic | Proprietary, SATA, V-by-One, Display Port | Low latency PCS, transmitter in electrical idle, signal detect at receiver, wider spread asynchronous SSC | “Basic Mode” on page 1-48 |
| PCI Express (PIPE) | PCIe Gen1 with PIPE Interface | PIPE ports, receiver detect, transmitter in electrical idle, electrical idle inference, signal detect at receiver, fast recovery, protocol-compliant word aligner and rate match FIFO, synchronous SSC | “PCI Express (PIPE) Mode” on page 1-52 |
| GIGE | GbE | Running disparity preservation, protocol-compliant word aligner, recovered clock port for applications such as Synchronous Ethernet | “GIGE Mode” on page 1-59 |
| Serial RapidIO | SRIO | Protocol-compliant word aligner | “Serial RapidIO Mode” on page 1-64 |
| XAUI | XAUI | Deskew FIFO, protocol-compliant word aligner and rate match FIFO | “XAUI Mode” on page 1-67 |

Table 1–25. PRBS, High and Low Frequency Patterns, and Channel Settings (Part 2 of 2)

| Patterns | Polynomial | 8-bit Channel Width | | | | 10-bit Channel Width | | | |
|-------------------|------------|-----------------------------|------------------------|--|---|------------------------------|------------------------|--|---|
| | | Channel Width of 8 bits (1) | Word Alignment Pattern | Maximum Data Rate (Gbps) for F324 and Smaller Packages | Maximum Data Rate (Gbps) for F484 and Larger Packages | Channel Width of 10-bits (1) | Word Alignment Pattern | Maximum Data Rate (Gbps) for F324 and Smaller Packages | Maximum Data Rate (Gbps) for F484 and Larger Packages |
| Low Frequency (2) | 1111100000 | N | — | — | — | Y | — | 2.5 | 3.125 |

Notes to Table 1–25:

- (1) Channel width refers to the **What is the channel width?** option in the **General** screen of the ALTGX MegaWizard Plug-In Manager. Based on the selection, an 8 or 10 bits wide pattern is generated as indicated by a **Yes (Y)** or **No (N)**.
- (2) A verifier and associated `rx_bistdone` and `rx_bisterr` signals are not available for the specified patterns.

You can enable the serial loopback option to loop the generated PRBS patterns to the receiver channel for verifier to check the PRBS patterns. When the PRBS pattern is received, the `rx_bisterr` and `rx_bistdone` signals indicate the status of the verifier. After the word aligner restores the word boundary, the `rx_bistdone` signal is driven high when the verifier receives a complete pattern cycle and remains asserted until it is reset using the `rx_digitalreset` port. After the assertion of `rx_bistdone`, the `rx_bisterr` signal is asserted for a minimum of three `rx_clkout` cycles when errors are detected in the data and deasserts if the following PRBS sequence contains no error. You can reset the PRBS pattern generator and verifier by asserting the `tx_digitalreset` and `rx_digitalreset` ports, respectively.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices ⁽¹⁾, ⁽²⁾

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | Unit |
|---|-----------------------------|--------------------|------------|-------------|-------|-------------|-------|-------|-------|------|
| | | | | Fast Corner | | Slow Corner | | | | |
| | | | | C6 | I7 | C6 | C7 | C8 | I7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.313 | 1.209 | 2.184 | 2.336 | 2.451 | 2.387 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.312 | 1.208 | 2.200 | 2.399 | 2.554 | 2.446 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.438 | 0.404 | 0.751 | 0.825 | 0.886 | 0.839 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.713 | 0.682 | 1.228 | 1.41 | 1.566 | 1.424 | ns |

Notes to Table 1–44:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices ⁽¹⁾, ⁽²⁾

| Parameter | Paths Affected | Number of Settings | Min Offset | Max Offset | | | | | | Unit |
|---|-----------------------------|--------------------|------------|-------------|-------|-------------|-------|-------|-------|------|
| | | | | Fast Corner | | Slow Corner | | | | |
| | | | | C6 | I7 | C6 | C7 | C8 | I7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 1.314 | 1.210 | 2.209 | 2.398 | 2.526 | 2.443 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 1.313 | 1.208 | 2.205 | 2.406 | 2.563 | 2.450 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.461 | 0.421 | 0.789 | 0.869 | 0.933 | 0.884 | ns |
| Input delay from dual-purpose clock pin to fan-out destinations | Pad to global clock network | 12 | 0 | 0.712 | 0.682 | 1.225 | 1.407 | 1.562 | 1.421 | ns |

Notes to Table 1–45:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.