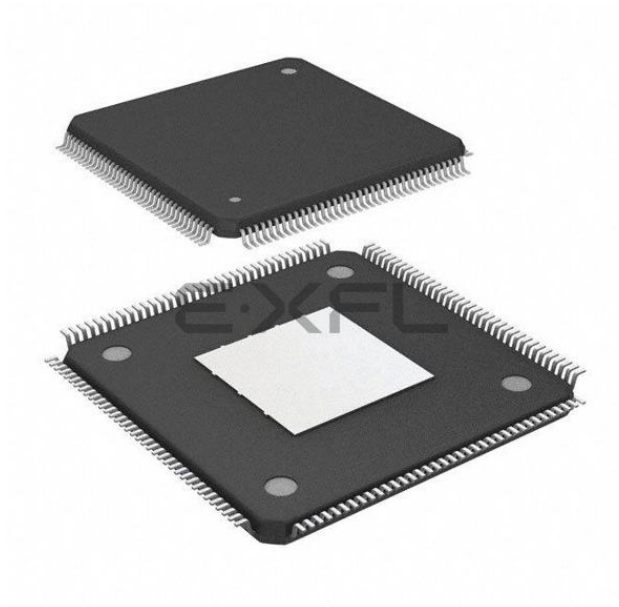

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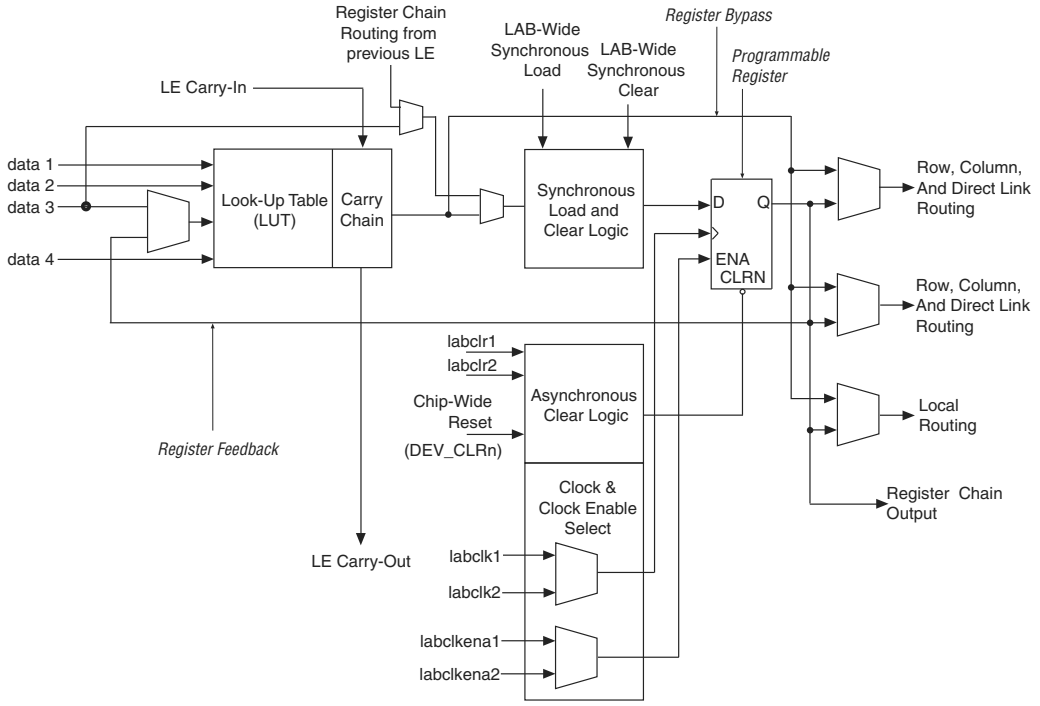
Details	
Product Status	Active
Number of LABs/CLBs	392
Number of Logic Elements/Cells	6272
Total RAM Bits	276480
Number of I/O	91
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	144-EQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce6e22c9l

Figure 2–1 shows the LEs for Cyclone IV devices.

Figure 2–1. Cyclone IV Device LEs



LE Features

You can configure the programmable register of each LE for D, T, JK, or SR flipflop operation. Each register has data, clock, clock enable, and clear inputs. Signals that use the global clock network, general-purpose I/O pins, or any internal logic can drive the clock and clear control signals of the register. Either general-purpose I/O pins or the internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output independently drives these three outputs. Two LE outputs drive the column or row and direct link routing connections, while one LE drives the local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. The LAB-wide synchronous load control signal is not available when using register packing. For more information about the synchronous load control signal, refer to "LAB Control Signals" on page 2–6.

The register feedback mode allows the register output to feed back into the LUT of the same LE to ensure that the register is packed with its own fan-out LUT, providing another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

Control Signals

The clock-enable control signal controls the clock entering the input and output registers and the entire M9K memory block. This signal disables the clock so that the M9K memory block does not see any clock edges and does not perform any operations.

The `rden` and `wren` control signals control the read and write operations for each port of M9K memory blocks. You can disable the `rden` or `wren` signals independently to save power whenever the operation is not required.

Parity Bit Support

Parity checking for error detection is possible with the parity bit along with internal logic resources. Cyclone IV devices M9K memory blocks support a parity bit for each storage byte. You can use this bit as either a parity bit or as an additional data bit. No parity function is actually performed on this bit.

Byte Enable Support

Cyclone IV devices M9K memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The `wren` signals, along with the byte-enable (`byteena`) signals, control the write operations of the RAM block. The default value of the `byteena` signals is high (enabled), in which case writing is controlled only by the `wren` signals. There is no clear port to the `byteena` registers. M9K blocks support byte enables when the write port has a data width of ×16, ×18, ×32, or ×36 bits.

Byte enables operate in one-hot manner, with the LSB of the `byteena` signal corresponding to the least significant byte of the data bus. For example, if `byteena = 01` and you are using a RAM block in ×18 mode, `data[8..0]` is enabled and `data[17..9]` is disabled. Similarly, if `byteena = 11`, both `data[8..0]` and `data[17..9]` are enabled. Byte enables are active high.

Table 3–2 lists the byte selection.

Table 3–2. byteena for Cyclone IV Devices M9K Blocks *(1)*

byteena[3..0]	Affected Bytes			
	datain ×16	datain ×18	datain ×32	datain ×36
[0] = 1	[7..0]	[8..0]	[7..0]	[8..0]
[1] = 1	[15..8]	[17..9]	[15..8]	[17..9]
[2] = 1	—	—	[23..16]	[26..18]
[3] = 1	—	—	[31..24]	[35..27]

Note to Table 3–2:

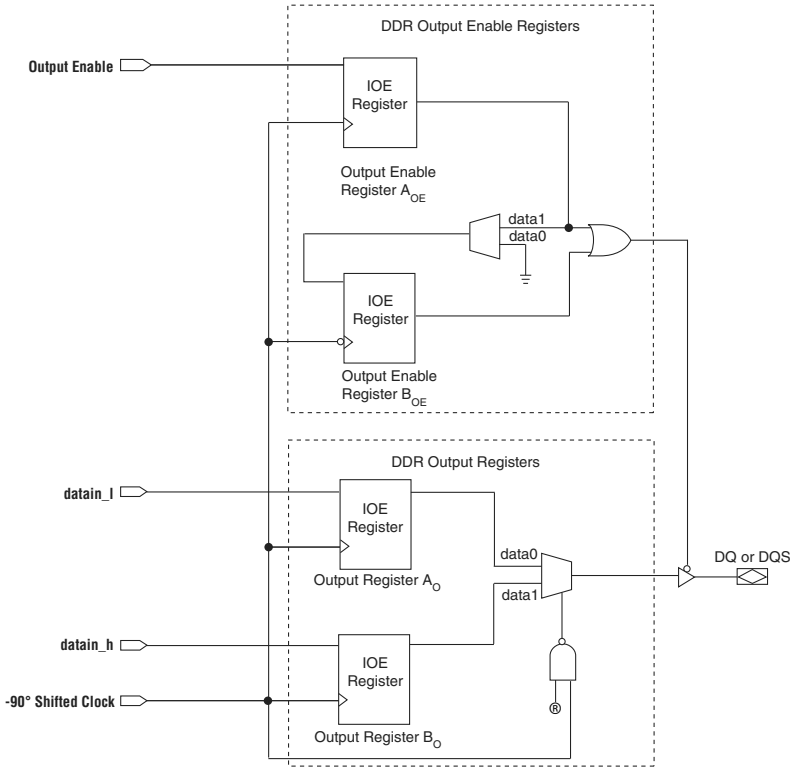
(1) Any combination of byte enables is possible.

DDR Output Registers

A dedicated write DDIO block is implemented in the DDR output and output enable paths.

Figure 7–8 shows how a Cyclone IV dedicated write DDIO block is implemented in the I/O element (IOE) registers.

Figure 7–8. Cyclone IV Dedicated Write DDIO



The two DDR output registers are located in the I/O element (IOE) block. Two serial data streams routed through `datain_l` and `datain_h`, are fed into two registers, `output register Ao` and `output register Bo`, respectively, on the same clock edge. The output from `output register Ao` is captured on the falling edge of the clock, while the output from `output register Bo` is captured on the rising edge of the clock. The registered outputs are multiplexed by the common clock to drive the DDR output pin at twice the data rate.

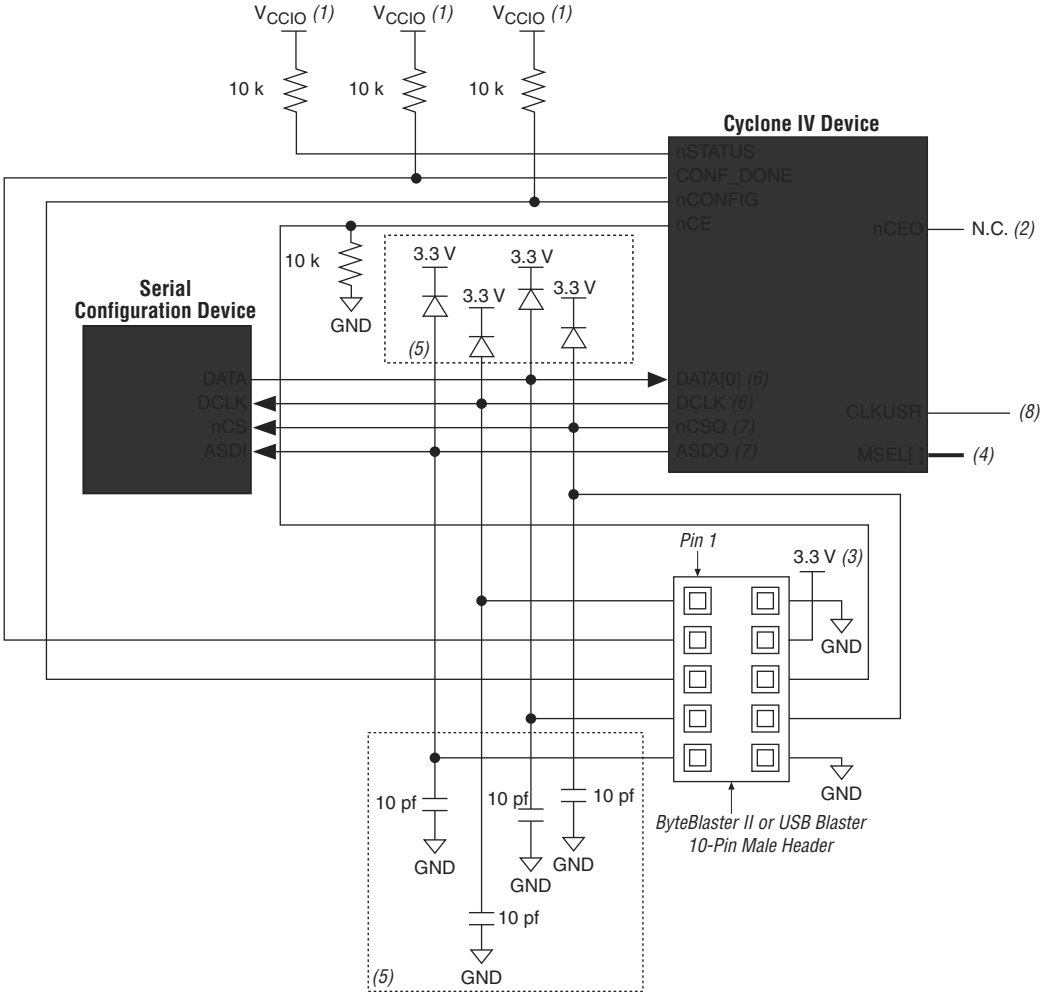
The DDR output enable path has a similar structure to the DDR output path in the IOE block. The second output enable register provides the write preamble for the `DQS` strobe in DDR external memory interfaces. This active-low output enable register extends the high-impedance state of the pin by half a clock cycle to provide the external memory's `DQS` write preamble time specification.

For more information about Cyclone IV IOE registers, refer to the *Cyclone IV Device I/O Features* chapter.

For more information about the USB-Blaster download cable, refer to the *USB-Blaster Download Cable User Guide*. For more information about the ByteBlaster II download cable, refer to the *ByteBlaster II Download Cable User Guide*.

Figure 8–6 shows the download cable connections to the serial configuration device.

Figure 8–6. In-System Programming of Serial Configuration Devices



Notes to Figure 8–6:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.

(3) Power up the V_{CC} of the ByteBlaster II or USB-Blaster download cable with the 3.3-V supply.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.

(5) The diodes and capacitors must be placed as close as possible to the Cyclone IV device. You must ensure that the diodes and capacitors maintain a maximum AC voltage of 4.1 V. The external diodes and capacitors are required to prevent damage to the Cyclone IV device AS configuration input pins due to possible overshoot when programming the serial configuration device with a download cable. Altera recommends using the Schottky diode, which has a relatively lower forward diode voltage (VF) than the switching and Zener diodes, for effective voltage clamping.

(6) When cascading Cyclone IV devices in a multi-device AS configuration, connect the repeater buffers between the master and slave devices for DATA[0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 8–5.

(7) These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as DATA[1] pin in AP and FPP modes.

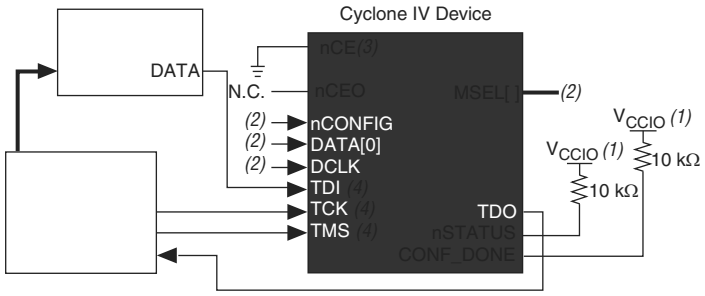
(8) Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK.

JTAG configuration allows an unlimited number of Cyclone IV devices to be cascaded in a JTAG chain.

For more information about configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera FPGA Chains* chapter in volume 2 of the *Configuration Handbook*.

Figure 8–27 shows JTAG configuration with a Cyclone IV device and a microprocessor.

Figure 8–27. JTAG Configuration of a Single Device Using a Microprocessor



Notes to Figure 8–27:

(1) You must connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain.

(2) Connect the `nCONFIG` and `MSEL` pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the `nCONFIG` pin to logic-high and the `MSEL` pins to GND. In addition, pull `DCLK` and `DATA[0]` to either high or low, whichever is convenient on your board.

(3) You must connect the `nCE` pin to GND or driven low for successful JTAG configuration.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. Signals driving into `TDI`, `TMS`, and `TCK` must fit the maximum overshoot outlined in Equation 8–1 on page 8–5.

Configuring Cyclone IV Devices with Jam STAPL

Jam™ STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP) purposes. Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems, using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard. The Jam Player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information about JTAG and Jam STAPL in embedded environments, refer to *AN 425: Using Command-Line Jam STAPL Solution for Device Programming*. To download the Jam Player, visit the Altera website (www.altera.com).

Configuring Cyclone IV Devices with the JRunner Software Driver

The JRunner software driver allows you to configure Cyclone IV devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The supported programming input file is in **.rbf** format. The JRunner software driver also requires a Chain Description File (**.cdf**) generated by the Quartus II software. The JRunner software driver is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

Table 8–25 lists the contents of previous state register 1 and previous state register 2 in the status register. The status register bit in Table 8–25 shows the bit positions in a 3-bit register. The previous state register 1 and previous state register 2 have the same bit definitions. The previous state register 1 reflects the current application configuration and the previous state register 2 reflects the previous application configuration.

Table 8–25. Remote System Upgrade Previous State Register 1 and Previous State Register 2 Contents in Status Register

Status Register Bit	Definition	Description
30	nCONFIG source	One-hot, active-high field that describes the reconfiguration source that caused the Cyclone IV device to leave the previous application configuration. If there is a tie, the higher bit order indicates precedence. For example, if nCONFIG and remote system upgrade nCONFIG reach the reconfiguration state machine at the same time, the nCONFIG precedes the remote system upgrade nCONFIG.
29	CRC error source	
28	nSTATUS source	
27	User watchdog timer source	
26	Remote system upgrade nCONFIG source	
25:24	Master state machine current state	The state of the master state machine during reconfiguration causes the Cyclone IV device to leave the previous application configuration.
23:0	Boot address	The address used by the configuration scheme to load the previous application configuration.

If a capture is inappropriately done while capturing a previous state before the system has entered remote update application configuration for the first time, a value outputs from the shift register to indicate that the capture is incorrectly called.

Remote System Upgrade State Machine

The remote system upgrade control and update registers have identical bit definitions, but serve different roles (Table 8–22 on page 8–75). While both registers can only be updated when the device is loaded with a factory configuration image, the update register writes are controlled by the user logic, and the control register writes are controlled by the remote system upgrade state machine.

In factory configurations, the user logic should send the option bits (Cd_early and Osc_int), the configuration address, and watchdog timer settings for the next application configuration bit to the update register. When the logic array configuration reset (RU_nCONFIG) goes high, the remote system upgrade state machine updates the control register with the contents of the update register and starts system reconfiguration from the new application page.

☞ To ensure the successful reconfiguration between the pages, assert the RU_nCONFIG signal for a minimum of 250 ns. This is equivalent to strobing the reconfig input of the ALTREMOTE_UPDATE megafunction high for a minimum of 250 ns.

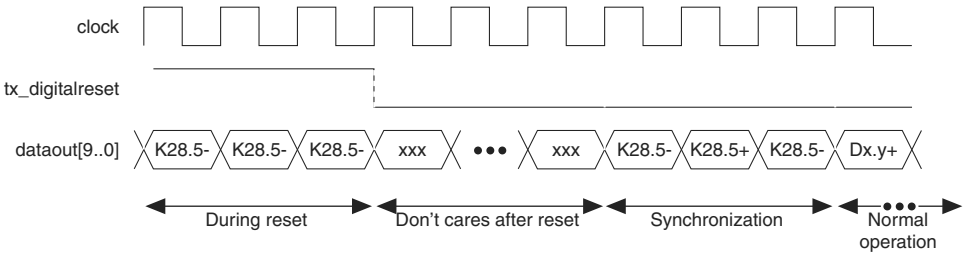
If there is an error or reconfiguration trigger condition, the remote system upgrade state machine directs the system to load a factory or application configuration (based on mode and error condition) by setting the control register accordingly.

Table 8–26 lists the contents of the control register after such an event occurs for all possible error or trigger conditions.

The following describes the 8B/10B encoder behavior in reset condition (as shown in Figure 1–7):

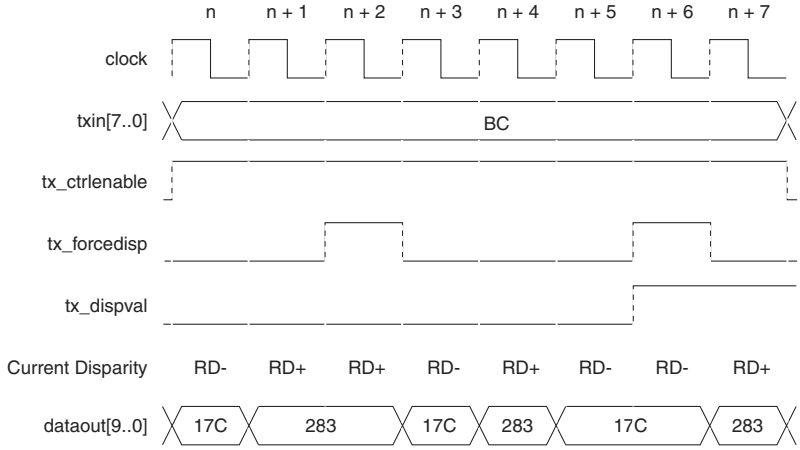
- During reset, the 8B/10B encoder ignores the inputs (`tx_datain` and `tx_ctrlenable` ports) from the FPGA fabric and outputs the K28.5 pattern from the RD- column continuously until the `tx_digitalreset` port is deasserted.
- Upon deassertion of the `tx_digitalreset` port, the 8B/10B encoder starts with a negative disparity and transmits three K28.5 code groups for synchronization before it starts encoding and transmitting data on its output.
- Due to some pipelining of the transmitter PCS, some "don't cares" (10'hxxx) are sent before the three synchronizing K28.5 code groups.

Figure 1–7. 8B/10B Encoder Behavior in Reset Condition



The encoder supports forcing the running disparity to either positive or negative disparity with `tx_forcedisp` and `tx_dispval` ports. Figure 1–8 shows an example of `tx_forcedisp` and `tx_dispval` port use, where data is shown in hexadecimal radix.

Figure 1–8. Force Running Disparity Operation



In this example, a series of K28.5 code groups are continuously sent. The stream alternates between a positive disparity K28.5 (RD+) and a negative disparity K28.5 (RD-) to maintain a neutral overall disparity. The current running disparity at time $n + 1$ indicates that the K28.5 in time $n + 2$ should be encoded with a negative disparity. Because `tx_forcedisp` is high at time $n + 2$, and `tx_dispval` is low, the K28.5

After updating the word boundary, word aligner status signals (rx_syncstatus and rx_patterndetect) are driven high for one parallel clock cycle synchronous to the most significant byte of the word alignment pattern. The rx_syncstatus and rx_patterndetect signals have the same latency as the datapath and are forwarded to the FPGA fabric to indicate the word aligner status. Any word alignment pattern received thereafter in the same word boundary causes only the rx_patterndetect signal to go high for one clock cycle.

Figure 1–17 shows the manual alignment mode word aligner operation in 10-bit data width mode. In this example, a /K28.5/ (10'b0101111100) is specified as the word alignment pattern.

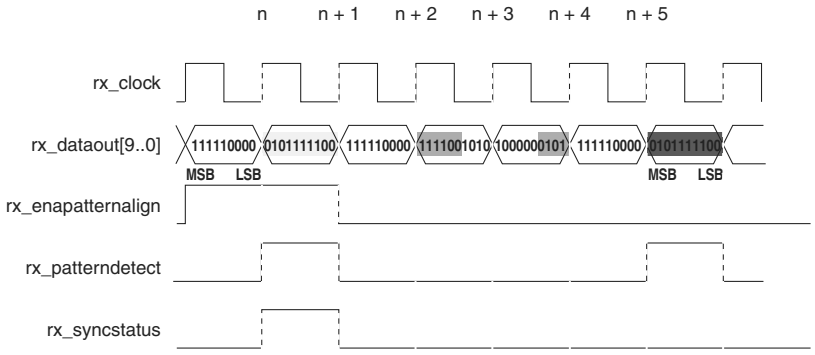
The word aligner aligns to the /K28.5/ alignment pattern (red) in cycle *n* because the rx_enapatternalign signal is asserted high. The rx_syncstatus signal goes high for one clock cycle indicating alignment to a new word boundary. The rx_patterndetect signal also goes high for one clock cycle to indicate initial word alignment.

At time *n* + 1, the rx_enapatternalign signal is deasserted to instruct the word aligner to lock the current word boundary.

The alignment pattern is detected again (green) in a new word boundary across cycles *n* + 2 and *n* + 3. The word aligner does not align to this new word boundary because the rx_enapatternalign signal is held low.

The /K28.5/ word alignment pattern is detected again (blue) in the current word boundary during cycle *n* + 5 causing the rx_patterndetect signal to go high for one parallel clock cycle.

Figure 1–17. Word Aligner in 10-bit Manual Alignment Mode



If the word alignment pattern is known to be unique and does not appear between word boundaries, you can hold the rx_enapatternalign signal constantly high because there is no possibility of false word alignment. If there is a possibility of the word alignment pattern occurring across word boundaries, you must control the rx_enapatternalign signal to lock the word boundary after the desired word alignment is achieved to avoid re-alignment to an incorrect word boundary.

Table 1–4 lists the synchronization state machine parameters for the word aligner in this mode.

Table 1–4. Synchronization State Machine Parameters

Parameter	Allowed Values
Number of erroneous code groups received to lose synchronization	1–64
Number of continuous good code groups received to reduce the error count by one	1–256

After deassertion of the rx_digitalreset signal in automatic synchronization state machine mode, the word aligner starts looking for the synchronization code groups, word alignment pattern or its complement in the received data stream. When the programmed number of valid synchronization code groups or ordered sets are received, the rx_syncstatus signal is driven high to indicate that synchronization is acquired. The rx_syncstatus signal is constantly driven high until the programmed number of erroneous code groups are received without receiving intermediate good groups; after which the rx_syncstatus signal is driven low. The word aligner indicates loss of synchronization (rx_syncstatus signal remains low) until the programmed number of valid synchronization code groups are received again.

In addition to restoring word boundaries, the word aligner supports the following features:

- Programmable run length violation detection—detects consecutive 1s or 0s in the data stream, and asserts run length violation signal (rx_rlv) when a preset run length threshold (maximum number of consecutive 1s or 0s) is detected. The rx_rlv signal in each channel is clocked by its parallel recovered clock and is asserted for a minimum of two recovered clock cycles to ensure that the FPGA fabric clock can latch the rx_rlv signal reliably because the FPGA fabric clock might have phase differences, ppm differences (in asynchronous systems), or both, with the recovered clock. Table 1–5 lists the run length violation circuit detection capabilities.

Table 1–5. Run Length Violation Circuit Detection Capabilities

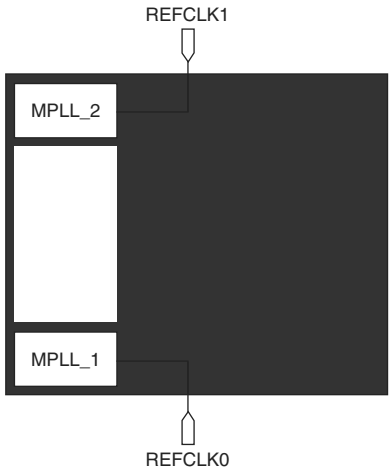
Supported Data Width	Detector Range		Increment Step Settings
	Minimum	Maximum	
8-bit	4	128	4
10-bit	5	160	5

Input Reference Clocking

When used for transceiver, the left PLLs synthesize the input reference clock to generate the required clocks for the transceiver channels. Figure 1–25 and Figure 1–26 show the sources of input reference clocks for PLLs used in the transceiver operation.

☞ Clock output from PLLs in the FPGA core cannot feed into PLLs used by the transceiver as input reference clock.

Figure 1–25. PLL Input Reference Clocks in Transceiver Operation for F324 and Smaller Packages (1), (2)



Notes to Figure 1–25:

(1) The REFCLK0 and REFCLK1 pins are dual-purpose CLK, REFCLK, or DIFFCLK pins that reside in banks 3A and 8A respectively.

(2) Using any clock input pins other than the designated REFCLK pins as shown here to drive the MPLLs may have reduced jitter performance.

Table 1–9 lists the high- and low-speed clock sources for each channel.

Table 1–9. High- and Low-Speed Clock Sources for Each Channel in Non-Bonded Channel Configuration

Package	Transceiver Block	Transceiver Channel	High- and Low-Speed Clocks Sources	
			Option 1	Option 2
F324 and smaller	GXBL0	All channels	MPLL_1	MPLL_2
F484 and larger	GXBL0	Channels 0, 1	MPLL_5/GPLL_1	MPLL_6
		Channels 2, 3	MPLL_5	MPLL_6/MPLL_7 (1)
	GXBL1 (1)	Channels 0, 1	MPLL_7/MPLL_6	MPLL_8
		Channels 2, 3	MPLL_7	MPLL_8/GPLL_2

Note to Table 1–9:

(1) MPLL_7 and GXBL1 are not applicable for transceivers in F484 package

Document Revision History

Table 1–30 lists the revision history for this chapter.

Table 1–30. Document Revision History

Date	Version	Changes
February 2015	3.7	■ Updated the GiGE row in Table 1–14. ■ Updated the "GIGE Mode" section. ■ Updated the note in the "Clock Frequency Compensation" section.
October 2013	3.6	Updated Figure 1–15 and Table 1–4.
May 2013	3.5	Updated Table 1–27 by setting "rx_locktodata" and "rx_locktorefclk" to "Input"
October 2012	3.4	■ Updated the data rate for the V-by-one protocol and the F324 package support in HD-SDI in Table 1–1. ■ Updated note (1) to Figure 1–27. ■ Added latency information to Figure 1–67.
November 2011	3.3	■ Updated "Word Aligner" and "Basic Mode" sections. ■ Updated Figure 1–37.
December 2010	3.2	■ Updated for the Quartus II software version 10.1 release. ■ Updated Table 1–1, Table 1–5, Table 1–11, Table 1–14, Table 1–24, Table 1–25, Table 1–26, Table 1–27, Table 1–28, and Table 1–29. ■ Updated "8B/10B Encoder", "Transmitter Output Buffer", "Receiver Input Buffer", "Clock Data Recovery", "Miscellaneous Transmitter PCS Features", "Miscellaneous Receiver PCS Feature", "Input Reference Clocking", "PCI Express (PIPE) Mode", "Channel Deskewing", "Lane Synchronization", "Serial Loopback", and "Self Test Modes" sections. ■ Added Figure 1–9, Figure 1–10, Figure 1–19, Figure 1–20, and Figure 1–43. ■ Updated Figure 1–53, Figure 1–55, Figure 1–59, Figure 1–60, Figure 1–69, Figure 1–70, Figure 1–71, Figure 1–72, Figure 1–73, and Figure 1–74.
November 2010	3.1	Updated Introductory information.
July 2010	3.0	■ Updated information for the Quartus II software version 10.0 release. ■ Reset control, power down, and dynamic reconfiguration information moved to new *Cyclone IV Reset Control and Power Down* and *Cyclone IV Dynamic Reconfiguration* chapters.

Table 2–3. Blocks Affected by Reset and Power-Down Signals (Part 2 of 2)

Transceiver Block	rx_digitalreset	rx_analogreset	tx_digitalreset	pll_areset	gxb_powerdown
Serializer	—	—	✓	—	✓
Transmitter Buffer	—	—	—	—	✓
Transmitter XAUI State Machine	—	—	✓	—	✓
Receiver Buffer	—	—	—	—	✓
Receiver CDR	—	✓	—	—	✓
Receiver Deserializer	—	—	—	—	✓
Receiver Word Aligner	✓	—	—	—	✓
Receiver Deskew FIFO	✓	—	—	—	✓
Receiver Clock Rate Compensation FIFO	✓	—	—	—	✓
Receiver 8B/10B Decoder	✓	—	—	—	✓
Receiver Byte Deserializer	✓	—	—	—	✓
Receiver Byte Ordering	✓	—	—	—	✓
Receiver Phase Compensation FIFO	✓	—	—	—	✓
Receiver XAUI State Machine	✓	—	—	—	✓
BIST Verifiers	✓	—	—	—	✓

Transceiver Reset Sequences

You can configure transceiver channels in Cyclone IV GX devices in various configurations. In all functional modes except XAUI functional mode, transceiver channels can be either bonded or non-bonded. In XAUI functional mode, transceiver channels must be bonded. In PCI Express® (PCIe®) functional mode, transceiver channels can be either bonded or non-bonded and need to follow a specific reset sequence.

The two categories of reset sequences for Cyclone IV GX devices described in this chapter are:

- "All Supported Functional Modes Except the PCIe Functional Mode" on page 2–6—describes the reset sequences in bonded and non-bonded configurations.
- "PCIe Functional Mode" on page 2–17—describes the reset sequence for the initialization/compliance phase and the normal operation phase in PCIe functional modes.

Table 3–7 lists the ALTGX megafunction ports for PLL Reconfiguration mode.

Table 3–7. ALTGX Megafunction Port List for PLL Reconfiguration Mode

Port Name (1)	Input/ Output	Description	Comments
pll_areset [n..0]	Input	Resets the transceiver PLL. The pll_areset are asserted in two conditions: ■ Used to reset the transceiver PLL during the reset sequence. During reset sequence, this signal is user controlled. ■ After the transceiver PLL is reconfigured, this signal is asserted high by the ALTPLL_RECONFIG controller. At this time, this signal is not user controlled.	You must connect the pll_areset port of ALTGX to the pll_areset port of the ALTPLL_RECONFIG megafunction. The ALTPLL_RECONFIG controller asserts the pll_areset port at the next rising clock edge after the pll_reconfig_done signal from the ALTGX megafunction goes high. After the pll_reconfig_done signal goes high, the transceiver PLL is reset. When the PLL reconfiguration is completed, this reset is performed automatically by the ALTPLL_RECONFIG megafunction and is not user controlled.
pll_scandata [n..0]	Input	Receives the scan data input from the ALTPLL_RECONFIG megafunction.	The reconfigurable transceiver PLL received the scan data input through this port for the dynamically reconfigurable bits from the ALTPLL_RECONFIG controller.
pll_scanclk [n..0]	Input	Drives the scanclk port on the reconfigurable transceiver PLL.	Connect the pll_scanclk port of the ALTGX megafunction to the ALTPLL_RECONFIG scanclk port.
pll_scanclkena [n..0]	Input	Acts as a clock enable for the scanclk port on the reconfigurable transceiver PLL.	Connect the pll_scanclkena port of the ALTGX megafunction to the ALTPLL_RECONFIG scanclk port.
pll_configupdate [n..0]	Input	Drives the configupdate port on the reconfigurable transceiver PLL.	This port is connected to the pll_configupdate port from the ALTPLL_RECONFIG controller. After the final data bit is sent out, the ALTPLL_RECONFIG controller asserts this signal.
pll_reconfig_done[n..0]	Output	This signal is asserted to indicate the reconfiguration process is done.	Connect the pll_reconfig_done port to the pll_scandone port on the ALTPLL_RECONFIG controller. The transceiver PLL scandone output signal drives this port and determines when the PLL is reconfigured.
pll_scandataout [n..0]	Output	This port scan out the current configuration of the transceiver PLL.	Connect the pll_scandataout port to the pll_scandataout port of the ALTPLL_RECONFIG controller. This port reads the current configuration of the transceiver PLL and send it to the ALTPLL_RECONFIG megafunction.

Note to Table 3–7:

(1) *<n>* = (number of transceiver PLLs configured in the ALTGX MegaWizard) - 1.

For more information about the ALTPLL_RECONFIG megafunction port list, description and usage, refer to the *Phase-Locked Loop Reconfiguration (ALTPL_RECONFIG) Megafunction User Guide*.

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (F324 and smaller package) *(15)*	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package) *(15)*	—	600	—	3125	600	—	3125	600	—	2500	Mbps
Absolute V_{MAX} for a receiver pin *(3)*	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{ICM} = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps	0.1	—	2.7	0.1	—	2.7	0.1	—	2.7	V
V_{ICM}	V_{ICM} = 0.82 V setting	—	820 ± 10%	—	—	820 ± 10%	—	—	820 ± 10%	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150–Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI	Compliant									—
Programmable ppm detector *(4)*	—	± 62.5, 100, 125, 200, 250, 300									ppm
Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)	—	—	—	±300 *(5)*, ±350 *(6)*, *(7)*	—	—	±300 *(5)*, ±350 *(6)*, *(7)*	—	—	±300 *(5)*, ±350 *(6)*, *(7)*	ppm
CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) *(8)*	—	—	—	350 to –5350 *(7)*, *(9)*	—	—	350 to –5350 *(7)*, *(9)*	—	—	350 to –5350 *(7)*, *(9)*	ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	No Equalization	—	—	1.5	—	—	1.5	—	—	1.5	dB
	Medium Low	—	—	4.5	—	—	4.5	—	—	4.5	dB
	Medium High	—	—	5.5	—	—	5.5	—	—	5.5	dB
	High	—	—	7	—	—	7	—	—	7	dB

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{LOCK} (2)	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–32:

(1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	400	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	400	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	400	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	400	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	400	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	400	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	400	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} (3)	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–33:

(1) Applicable for true and emulated mini-LVDS transmitter.

(2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.
Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.