Intel - EP4CE6F17C8L Datasheet





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Details

Product Status	Active
Number of LABs/CLBs	392
Number of Logic Elements/Cells	6272
Total RAM Bits	276480
Number of I/O	179
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce6f17c8l

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In addition to the three general routing outputs, LEs in an LAB have register chain outputs, which allows registers in the same LAB to cascade together. The register chain output allows the LUTs to be used for combinational functions and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources.

LE Operating Modes

Cyclone IV LEs operate in the following modes:

- Normal mode
- Arithmetic mode

The Quartus[®] II software automatically chooses the appropriate mode for common functions, such as counters, adders, subtractors, and arithmetic functions, in conjunction with parameterized functions such as the library of parameterized modules (LPM) functions. You can also create special-purpose functions that specify which LE operating mode to use for optimal performance, if required.

Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (Figure 2–2). The Quartus II Compiler automatically selects the carry-in (cin) or the data3 signal as one of the inputs to the LUT. LEs in normal mode support packed registers and register feedback.

Figure 2–2 shows LEs in normal mode.





2–3

Figure 3–3 and Figure 3–4 show the address clock enable waveform during read and write cycles, respectively.



Figure 3–3. Cyclone IV Devices Address Clock Enable During Read Cycle Waveform

Figure 3-4. Cyclone IV Devices Address Clock Enable During Write Cycle Waveform



Mixed-Width Support

M9K memory blocks support mixed data widths. When using simple dual-port, true dual-port, or FIFO modes, mixed width support allows you to read and write different data widths to an M9K memory block. For more information about the different widths supported per memory mode, refer to "Memory Modes" on page 3–7.

Figure 5–14 shows a waveform example of the phase relationship of the PLL clocks in this mode.



Figure 5-14. Phase Relationship Between PLL Clocks in Normal Mode

Note to Figure 5-14:

(1) The external clock output can lead or lag the PLL internal clock signals.

Zero Delay Buffer Mode

In zero delay buffer (ZDB) mode, the external clock output pin is phase-aligned with the clock input pin for zero delay through the device. When using this mode, use the same I/O standard on the input clock and output clocks to guarantee clock alignment at the input and output pins.

Figure 5–15 shows an example waveform of the phase relationship of the PLL clocks in ZDB mode.





Post-Scale Counter Cascading

PLLs of Cyclone IV devices support post-scale counter cascading to create counters larger than 512. This is implemented by feeding the output of one C counter into the input of the next C counter, as shown in Figure 5–16.

Figure 5–16. Counter Cascading



When cascading counters to implement a larger division of the high-frequency VCO clock, the cascaded counters behave as one counter with the product of the individual counter settings.

For example, if C0 = 4 and C1 = 2, the cascaded value is $C0 \times C1 = 8$.

Post-scale counter cascading is automatically set by the Quartus II software in the configuration file. Post-scale counter cascading cannot be performed using the PLL reconfiguration.

Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on the PLL post-scale counters. You can achieve the duty cycle setting by a low and high time count setting for the post-scale counters. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices. The post-scale counter value determines the precision of the duty cycle. The precision is defined by 50% divided by the post-scale counter value. For example, if the C0 counter is 10, steps of 5% are possible for duty cycle choices between 5 to 90%.

Combining the programmable duty cycle with programmable phase shift allows the generation of precise non-overlapping clocks.

PLL Control Signals

You can use the pfdena, areset, and locked signals to observe and control the PLL operation and resynchronization.



For more information about the PLL control signals, refer to the *ALTPLL Megafunction User Guide*.

- Low time count = 1 cycle
- rselodd = 1 effectively equals:
 - High time count = 1.5 cycles
 - Low time count = 1.5 cycles
 - Duty cycle = (1.5/3)% high time count and (1.5/3)% low time count

Scan Chain Description

Cyclone IV PLLs have a 144-bit scan chain.

Table 5–7 lists the number of bits for each component of the PLL.

Table 5–7.	Cyclone	IV PLL	Reprogramming Bits
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Plack Nomo	Number of Bits									
DIUCK Name	Counter	Other	Total							
C4 (1)	16	2 (2)	18							
C3	16	2 (2)	18							
C2	16	2 (2)	18							
C1	16	2 (2)	18							
CO	16	2 (2)	18							
М	16	2 (2)	18							
Ν	16	2 (2)	18							
Charge Pump	9	0	9							
Loop Filter ⁽³⁾	9	0	9							
Total number of bits:			144							

Notes to Table 5-7:

(1) LSB bit for C4 low-count value is the first bit shifted into the scan chain.

- (2) These two control bits include <code>rbypass</code>, for bypassing the counter, and <code>rselodd</code>, to select the output clock duty cycle.
- (3) MSB bit for loop filter is the last bit shifted into the scan chain.

Figure 5–24 shows the scan chain order of the PLL components.

Figure 5–24. PLL Component Scan Chain Order



The CLKIN/REFCLK pins are powered by dedicated V_{CC_CLKIN3A}, V_{CC_CLKIN3B}, V_{CC_CLKIN3B}, v_{CC_CLKIN8A}, and V_{CC_CLKIN8B} power supplies separately in their respective I/O banks to avoid the different power level requirements in the same bank for GPIO.

				VCC_C	LKIN Level	I/O Pin Type			
I/O Standard	HSSI Protocol	Coupling	Termination	Input	Output	Column I/O	Row I/O	Supported I/O Banks	
LVDS	All		Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B	
LVPECL	All	Differential AC (Need	Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B	
	All	off chip resistor to	Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B	
1.2V, 1.5V, 3.3V PCML	All	restore V _{CM})	Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B	
	All		Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B	
HCSL	PCIe	Differential DC	Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B	

Table 6–10. Cyclone IV GX HSSI REFCLK I/O Standard Support Using GPIO CLKIN Pins (1), (2)

Notes to Table 6-10:

(1) The EP4CGX15, EP4CGX22, and EP4CGX30 devices have two pairs of dedicated clock input pins in banks 3A and 8A for HSSI input reference clock. I/O banks 3B and 8B are not available in EP4CGX15, EP4CGX22, and EP4CGX30 devices.

(2) The EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have four pairs of dedicated clock input pins in banks 3A, 3B, 8A, and 8B for HSSI input or single-ended clock input.

To For more information about the AC-coupled termination scheme for the HSSI reference clock, refer to the *Cyclone IV Transceivers Architecture* chapter.

LVDS I/O Standard Support in Cyclone IV Devices

The LVDS I/O standard is a high-speed, low-voltage swing, low power, and GPIO interface standard. Cyclone IV devices meet the ANSI/TIA/EIA-644 standard with the following exceptions:

- The maximum differential output voltage (V_{OD}) is increased to 600 mV. The maximum V_{OD} for ANSI specification is 450 mV.
- The input voltage range is reduced to the range of 1.0 V to 1.6 V, 0.5 V to 1.85 V, or 0 V to 1.8 V based on different frequency ranges. The ANSI/TIA/EIA-644 specification supports an input voltage range of 0 V to 2.4 V.
- For LVDS I/O standard electrical specifications in Cyclone IV devices, refer to the *Cyclone IV Device Datasheet* chapter.

implements either a high-speed deserializer receiver or a high-speed serializer transmitter. There is a list of parameters in the ALTLVDS megafunction that you can set to customize your SERDES based on your design requirements. The megafunction is optimized to use Cyclone IV devices resources to create high-speed I/O interfaces in the most effective manner.



When you use Cyclone IV devices with the ALTLVDS megafunction, the interface always sends the MSB of your parallel data first.

C For more details about designing your high-speed I/O systems interfaces using the ALTLVDS megafunction, refer to the *ALTLVDS Megafunction User Guide* and the *Quartus II Handbook*.

Document Revision History

Table 6–12 lists the revision history for this chapter.

Date	Version	Changes						
March 2016	2.7	 Updated Table 6–5 and Table 6–9 to remove support for the N148 package. 						
May 2013	2.6	■ Updated Table 6–2 by adding Note (9).						
Way 2013	2.0	■ Updated Table 6–4 and Table 6–8 to add new device options and packages.						
February 2013	2.5	Updated Table 6–4 and Table 6–8 to add new device options and packages.						
		 Updated "I/O Banks" and "High Speed Serial Interface (HSSI) Input Reference Clock Support " sections. 						
October 2012	2.4	■ Updated Table 6–3 and Table 6–5.						
		■ Updated Figure 6–10.						
November 2011		 Updated "Differential SSTL I/O Standard Support in Cyclone IV Devices" and "Differential HSTL I/O Standard Support in Cyclone IV Devices" sections. 						
	2.3	■ Updated Table 6–1, Table 6–8, and Table 6–9.						
		■ Updated Figure 6–1.						
		 Updated for the Quartus II software version 10.1 release. 						
		 Added Cyclone IV E new device package information. 						
December 2010	2.2	 Added "Clock Pins Functionality" section. 						
		■ Updated Table 6–4 and Table 6–8.						
		 Minor text edits. 						
		 Updated "Cyclone IV I/O Elements", "Programmable Pull-Up Resistor", "I/O Banks", "High-Speed I/O Interface", and "Designing with BLVDS" sections. 						
July 2010	2.1	■ Updated Table 6–6 and Table 6–7.						
		■ Updated Figure 6–19.						

Table 6–12. Document Revision History (Part 1 of 2)

- 3. Click the **Configuration** tab.
- 4. Turn on Generate compressed bitstreams.
- 5. Click OK.
- 6. In the **Settings** dialog box, click **OK**.

You can enable compression when creating programming files from the **Convert Programming Files** dialog box. To enable compression, perform the following steps:

- 1. On the File menu, click Convert Programming Files.
- 2. Under **Output programming file**, select your desired file type from the **Programming file type** list.
- 3. If you select **Programmer Object File (.pof)**, you must specify the configuration device in the **Configuration device** list.
- 4. Under Input files to convert, select SOF Data.
- 5. Click Add File to browse to the Cyclone IV device SRAM object files (.sof).
- 6. In the **Convert Programming Files** dialog box, select the **.pof** you added to **SOF Data** and click **Properties**.
- 7. In the SOF File Properties dialog box, turn on the Compression option.

When multiple Cyclone IV devices are cascaded, you can selectively enable the compression feature for each device in the chain. Figure 8–1 shows a chain of two Cyclone IV devices. The first device has compression enabled and receives compressed bitstream from the configuration device. The second device has the compression feature disabled and receives uncompressed data. You can generate programming files for this setup in the **Convert Programming Files** dialog box.

Figure 8–1. Compressed and Uncompressed Configuration Data in the Same Configuration File



Configuration Requirement

This section describes Cyclone IV device configuration requirement and includes the following topics:

- "Power-On Reset (POR) Circuit" on page 8–4
- "Configuration File Size" on page 8–4
- "Power Up" on page 8–6

Configuration Process

This section describes Cyclone IV device configuration requirements and includes the following topics:

- "Power Up" on page 8–6
- "Reset" on page 8–6
- "Configuration" on page 8–6
- "Configuration Error" on page 8–7
- "Initialization" on page 8–7
- "User Mode" on page 8–7
- ***** For more information about the Altera[®] FPGA configuration cycle state machine, refer to the *Configuring Altera FPGAs* chapter in volume 1 of the *Configuration Handbook*.

Power Up

If the device is powered up from the power-down state, V_{CCINT} , V_{CCA} , and V_{CCIO} (for the I/O banks in which the configuration and JTAG pins reside) must be powered up to the appropriate level for the device to exit from POR.

Reset

After power up, Cyclone IV devices go through POR. POR delay depends on the MSEL pin settings, which correspond to your configuration scheme. During POR, the device resets, holds nSTATUS and CONF_DONE low, and tri-states all user I/O pins (for PS and FPP configuration schemes only).

To tri-state the configuration bus for AS and AP configuration schemes, you must tie nCE high and nCONFIG low.

The user I/O pins and dual-purpose I/O pins have weak pull-up resistors, which are always enabled (after POR) before and during configuration. When the device exits POR, all user I/O pins continue to tri-state. While nCONFIG is low, the device is in reset. When nCONFIG goes high, the device exits reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-k Ω pull-up resistor. After nSTATUS is released, the device is ready to receive configuration data and the configuration stage starts.

... For more information about the value of the weak pull-up resistors on the I/O pins that are on before and during configuration, refer to the Cyclone IV Device Datasheet chapter.

Configuration

Configuration data is latched into the Cyclone IV device at each DCLK cycle. However, the width of the data bus and the configuration time taken for each scheme are different. After the device receives all the configuration data, the device releases the open-drain CONF_DONE pin, which is pulled high by an external 10-k Ω pull-up resistor. A low-to-high transition on the CONF_DONE pin indicates that the configuration is complete and initialization of the device can begin.

resistors.

Default read mode of the supported parallel flash memory and all writes to the parallel flash memory are asynchronous. Both the parallel flash families support a synchronous read mode, with data supplied on the positive edge of DCLK.

The serial clock (DCLK) generated by Cyclone IV E devices controls the entire configuration cycle and provides timing for the parallel interface.

Multi-Device AP Configuration

You can configure multiple Cyclone IV E devices using a single parallel flash. You can cascade multiple Cyclone IV E devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to GND. You must connect its nCEO pin to the nCE pin of the next device in the chain. Use an external 10-k Ω pull-up resistor to pull the nCEO signal high to its V_{CCIO} level to help the internal weak pull-up resistor. When the first device captures all its configuration data from the bitstream, it drives the nCEO pin low, enabling the next device in the chain. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in the chain is a Cyclone IV E device. The nCONFIG, nSTATUS, CONF_DONE, DCLK, DATA[15..8], and DATA[7..0] pins of each device in the chain are connected (Figure 8–8 on page 8–26 and Figure 8–9 on page 8–27).

The first Cyclone IV E device in the chain, as shown in Figure 8–8 on page 8–26 and Figure 8–9 on page 8–27, is the configuration master device and controls the configuration of the entire chain. You must connect its MSEL pins to select the AP configuration scheme. The remaining Cyclone IV E devices are used as configuration slaves. You must connect their MSEL pins to select the FPP configuration scheme. Any other Altera device that supports FPP configuration can also be part of the chain as a configuration slave.

The following are the configurations for the DATA [15..0] bus in a multi-device AP configuration:

- Byte-wide multi-device AP configuration
- Word-wide multi-device AP configuration

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system with JTAG BST circuitry. Figure 8–25 and Figure 8–26 show multi-device JTAG configuration.

For devices using 2.5-, 3.0-, and 3.3-V V_{CCIO} supply, you must refer to Figure 8–25. All I/O inputs must maintain a maximum AC voltage of 4.1 V because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using 2.5-, 3.0-, and 3.3- V V_{CCIO} supply. You must power up the V_{CC} of the download cable with a 2.5-V V_{CCA} supply. For device using V_{CCIO} of 1.2, 1.5 V, and 1.8 V, refer to Figure 8–26. You can power up the V_{CC} of the download cable with the supply from V_{CCIO}.

Figure 8–25. JTAG Configuration of Multiple Devices Using a Download Cable (2.5, 3.0, and 3.3-V V_{CCIO} Powering the JTAG Pins)



Notes to Figure 8-25:

- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Connect the nCONFIG and MSEL pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA [0] to either high or low, whichever is convenient on your board.
- (3) Pin 6 of the header is a V₁₀ reference voltage for the MasterBlaster output driver. V₁₀ must match the V_{CCA} of the device. For this value, refer to the MasterBlaster Serial/USB Communications Cable User Guide. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) You must connect the nCE pin to GND or driven low for successful JTAG configuration.
- (5) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.
- (6) Resistor value can vary from 1 k Ω to 10 k Ω .

IEEE Std. 1149.6 Boundary-Scan Register

The boundary-scan cell (BSC) for HSSI transmitters ($GXB_TX[p,n]$) and receivers ($GXB_RX[p,n]$) in Cyclone IV GX devices are different from the BSCs for I/O pins.

Figure 10–1 shows the Cyclone IV GX HSSI transmitter boundary-scan cell.





Cyclone IV Device Handbook,

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Serial loopback mode can only be dynamically enabled or disabled during user mode by performing a dynamic channel reconfiguration.

Figure 1–71. Serial Loopback Path⁽¹⁾



Note to Figure 1–71:

(1) Grayed-Out Blocks are Not Active in this mode.

Reverse Serial Loopback

The reverse serial loopback mode is available for all functional modes except for XAUI mode. The two reverse serial loopback options from the receiver to the transmitter are:

- Pre-CDR mode where data received through the RX input buffer is looped back to the TX output buffer using the **Reverse serial loopback (pre-CDR)** option
- Post-CDR mode where retimed data through the receiver CDR from the RX input buffer is looped back to the TX output buffer using the Reverse serial loopback option

The received data is also available to the FPGA logic. In the transmitter channel, only the transmitter buffer is active.

- The transmitter pre-emphasis feature is not available in reverse serial loopback (pre-CDR) mode.
- Reverse serial loopback modes can only be dynamically enabled or disabled during user mode by performing a dynamic channel reconfiguration.



cancellation process on the receiver channel.

The deassertion of the busy signal indicates proper completion of the offset

Figure 2–13. Sample Reset Sequence of a Receiver and Transmitter Channels-Receiver CDR in Automatic Lock Mode with the Optional gxb_powerdown Signal ⁽¹⁾

Notes to Figure 2-13:

- (1) The $gxb_powerdown$ signal must not be asserted during the offset cancellation sequence.
- (2) For t_{LTD_Auto} duration, refer to the *Cyclone IV Device Datasheet* chapter.
- (3) The busy signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the busy signal is asserted and deasserted only if there is a read or write operation to the ALTGX_RECONFIG megafunction.

Simulation Requirements

The following are simulation requirements:

- The gxb_powerdown port is optional. In simulation, if the gxb_powerdown port is not instantiated, you must assert the tx_digitalreset, rx_digitalreset, and rx_analogreset signals appropriately for correct simulation behavior.
- If the gxb_powerdown port is instantiated, and the other reset signals are not used, you must assert the gxb_powerdown signal for at least 1 µs for correct simulation behavior.
- You can deassert the rx_digitalreset signal immediately after the rx_freqlocked signal goes high to reduce the simulation run time. It is not necessary to wait for t_{LTD_Auto} (as suggested in the actual reset sequence).
- The busy signal is deasserted after about 20 parallel reconfig_clk clock cycles in order to reduce simulation run time. For silicon behavior in hardware, you can follow the reset sequences described in the previous pages.

Functional Simulation of the Dynamic Reconfiguration Process

This section describes the points to be considered during functional simulation of the dynamic reconfiguration process.

- You must connect the ALTGX_RECONFIG instance to the ALTGX_instance/ALTGX instances in your design for functional simulation.
- The functional simulation uses a reduced timing model of the dynamic reconfiguration controller. The duration of the offset cancellation process is 16 reconfig_clk clock cycles for functional simulation only.
- The gxb_powerdown signal must not be asserted during the offset cancellation sequence (for functional simulation and silicon).

Document Revision History

Table 3–8 lists the revision history for this chapter.

 Table 3–8.
 Document Revision History

Date	Version	Changes
November 2011	2.1	 Updated "Dynamic Reconfiguration Controller Architecture", "PMA Controls Reconfiguration Mode", "PLL Reconfiguration Mode", and "Error Indication During Dynamic Reconfiguration" sections.
		■ Updated Table 3–2 and Table 3–4.
		 Updated for the Quartus II software version 10.1 release.
		■ Updated Table 3–1, Table 3–2, Table 3–3, Table 3–4, Table 3–5, and Table 3–6.
		■ Added Table 3–7.
December 2010	2.0	■ Updated Figure 3–1, Figure 3–11, Figure 3–13, and Figure 3–14.
		 Updated "Offset Cancellation Feature", "Error Indication During Dynamic Reconfiguration", "Data Rate Reconfiguration Mode Using RX Local Divider", "PMA Controls Reconfiguration Mode", and "Control and Status Signals for Channel Reconfiguration" sections.
July 2010	1.0	Initial release.

Chapter Revision Dates

The chapters in this document, Cyclone IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Cyclone IV Device Datasheet Revised: December 2016 Part Number: CYIV-53001-2.1 A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit			
		V ₁ = 4.20	100	%			
		V ₁ = 4.25	98	%			
		V ₁ = 4.30	65	%			
		V ₁ = 4.35	43	%			
Vi	AC Input Voltage	V ₁ = 4.40	29	%			
	Voltago	V ₁ = 4.45	20	%			
		$V_1 = 4.50$	13	%			
		V ₁ = 4.55	9	%			
		$V_1 = 4.60$	6	%			

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.





***** For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices (1)

I/O Standard SSTL-2	v	/ _{ccio} (V)	V _{Swing(DC)} (V)		V _{X(AC)} (V)			V _{Swing(AC)} (V)		V _{OX(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V _{CCIO}	$V_{CC10}/2 - 0.2$	_	V _{CCI0} /2 + 0.2	0.7	V _{CCI} 0	V _{CCIO} /2 – 0.125		V _{CCI0} /2 + 0.125
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V _{CCIO}	V _{CCIO} /2 – 0.175	_	V _{CCI0} /2 + 0.175	0.5	V _{CCI} 0	V _{CCIO} /2 – 0.125		V _{CCI0} /2 + 0.125

Note to Table 1-18:

(1) Differential SSTL requires a V_{REF} input.

Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾

	١	/ _{ccio} (V)	V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)				V _{DIF(AC)} (V)	
I/O Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Mi n	Max	
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.85	_	0.95	0.85		0.95	0.4		
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.71	_	0.79	0.71		0.79	0.4	_	
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO}	$0.48 \times V_{CCIO}$	_	0.52 x V _{CCI0}	0.48 x V _{CCIO}		0.52 x V _{CCI0}	0.3	0.48 x V _{CCI0}	

Note to Table 1-19:

(1) Differential HSTL requires a V_{REF} input.

 Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices ⁽¹⁾ (Part 1 of 2)

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)		V _{ICM} (V) ⁽²⁾				V _{OD} (mV) ⁽³⁾			V _{0S} (V) ⁽³⁾		
i/U Stanuaru	Min	Тур	Max	Min	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max	
					_	0.05	$D_{MAX} \leq 500 \; Mbps$	1.80							
(Row I/Os) (6)	2.375	2.5	2.625	100		0.55	$\begin{array}{l} 500 \text{ Mbps} \leq \text{ D}_{\text{MAX}} \\ \leq 700 \text{ Mbps} \end{array}$	1.80	_	—		—	_		
						1.05	D _{MAX} > 700 Mbps	1.55							
LVPECL (Column			2.625	100		0.05	$D_{MAX} \leq ~500~Mbps$	1.80		_	_	_		_	
	2.375	2.5				0.55	$\begin{array}{l} 500 \text{ Mbps} \leq \text{D}_{\text{MAX}} \\ \leq 700 \text{ Mbps} \end{array}$	1.80	_						
1,00)						1.05	D _{MAX} > 700 Mbps	1.55							
						0.05	$D_{MAX} \leq 500 \; Mbps$	1.80						1.375	
LVDS (Row I/Os)	2.375	2.5	2.5 2.625	100	_	0.55	$\begin{array}{l} 500 \mbox{ Mbps} \leq D_{MAX} \\ \leq \mbox{ 700 } \mbox{ Mbps} \end{array}$	1.80	247	—	600	1.125	1.25		
						1.05	D _{MAX} > 700 Mbps	1.55							

Symbol/	a		C6			C7, 17			C8		
Description	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Signal detect/loss threshold	PIPE mode	65	_	175	65	_	175	65	_	175	mV
t _{LTR} (10)	—		_	75		_	75	_	—	75	μs
t _{LTR-LTD_Manual} (11)	—	15	_	_	15	—		15	_	—	μs
t _{LTD} (12)	—	0	100	4000	0	100	4000	0	100	4000	ns
t _{LTD_Manual} <i>(13)</i>	—		_	4000			4000	_		4000	ns
t _{LTD_Auto} (14)	—	_	_	4000		—	4000		_	4000	ns
Receiver buffer and CDR offset cancellation time (per channel)	_	_	_	17000	_	_	17000	_	_	17000	recon fig_c lk cycles
	DC Gain Setting = 0		0	_	_	0	_	_	0	_	dB
Programmable DC gain	DC Gain Setting = 1	_	3	_	_	3	_	_	3	_	dB
	DC Gain Setting = 2	_	6	_	_	6	_	_	6	_	dB
Transmitter											
Supported I/O Standards	1.5 V PCML										
Data rate (F324 and smaller package)	_	600	_	2500	600	_	2500	600	_	2500	Mbps
Data rate (F484 and larger package)	_	600	_	3125	600	_	3125	600	_	2500	Mbps
V _{OCM}	0.65 V setting	_	650	_		650		_	650	_	mV
Differential on-chip	100– Ω setting	_	100	_		100		_	100	—	Ω
termination resistors	150– Ω setting	_	150	_	_	150		_	150	—	Ω
Differential and common mode return loss	PIPE, CPRI LV, Serial Rapid I/O SR, SDI, XAUI, SATA		Compliant -								
Rise time	—	50	_	200	50	—	200	50	—	200	ps
Fall time		50	_	200	50	—	200	50	—	200	ps
Intra-differential pair skew	_	_	_	15	_	_	15	_	_	15	ps
Intra-transceiver block skew	_	_	_	120	_	_	120	_	_	120	ps

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 3 of 4)