Intel - EP4CE6U14I7N Datasheet





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Details

Product Status	Active
Number of LABs/CLBs	392
Number of Logic Elements/Cells	6272
Total RAM Bits	276480
Number of I/O	179
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LFBGA
Supplier Device Package	256-UBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce6u14i7n

Email: info@E-XFL.COM

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To For more information, refer to the *External Memory Interfaces in Cyclone IV Devices* chapter.

Configuration

Cyclone IV devices use SRAM cells to store configuration data. Configuration data is downloaded to the Cyclone IV device each time the device powers up. Low-cost configuration options include the Altera EPCS family serial flash devices and commodity parallel flash configuration options. These options provide the flexibility for general-purpose applications and the ability to meet specific configuration and wake-up time requirements of the applications.

Table 1–9 lists which configuration schemes are supported by Cyclone IV devices.

Table 1–9. Configuration Schemes for Cyclone IV Device Family

Devices	Supported Configuration Scheme
Cyclone IV GX	AS, PS, JTAG, and FPP (1)
Cyclone IV E	AS, AP, PS, FPP, and JTAG

Note to Table 1-9:

(1) The FPP configuration scheme is only supported by the EP4CGX30F484 and EP4CGX50/75/110/150 devices.

IEEE 1149.6 (AC JTAG) is supported on all transceiver I/O pins. All other pins support IEEE 1149.1 (JTAG) for boundary scan testing.

For more information, refer to the *JTAG Boundary-Scan Testing for Cyclone IV Devices* chapter.

For Cyclone IV GX devices to meet the PCIe 100 ms wake-up time requirement, you must use passive serial (PS) configuration mode for the EP4CGX15/22/30 devices and use fast passive parallel (FPP) configuration mode for the EP4CGX30F484 and EP4CGX50/75/110/150 devices.

For more information, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.

The cyclical redundancy check (CRC) error detection feature during user mode is supported in all Cyclone IV GX devices. For Cyclone IV E devices, this feature is only supported for the devices with the core voltage of 1.2 V.



For more information about CRC error detection, refer to the *SEU Mitigation in Cyclone IV Devices* chapter.

High-Speed Transceivers (Cyclone IV GX Devices Only)

Cyclone IV GX devices contain up to eight full duplex high-speed transceivers that can operate independently. These blocks support multiple industry-standard communication protocols, as well as Basic mode, which you can use to implement your own proprietary protocols. Each transceiver channel has its own pre-emphasis and equalization circuitry, which you can set at compile time to optimize signal integrity and reduce bit error rates. Transceiver blocks also support dynamic reconfiguration, allowing you to change data rates and protocols on-the-fly.

Document Revision History

Table 4–3 lists the revision history for this chapter.

Table 4–3. Document Revision History

Date	Version	Changes
February 2010	1.1	Added Cyclone IV E devices in Table 4–1 for the Quartus II software version 9.1 SP1 release.
November 2009	1.0	Initial release.

Figure 6–9 shows the overview of Cyclone IV E I/O banks.

Figure 6–9. Cyclone IV E I/O Banks (1), (2)



Notes to Figure 6-9:

- (1) This is a top view of the silicon die. This is only a graphical representation. For exact pin locations, refer to the pin list and the Quartus II software.
- (2) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only. External resistors are needed for the differential outputs in column I/O banks.
- (3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
- (4) The HSTL-12 Class II is supported in column I/O banks 3, 4, 7, and 8 only.
- (6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 3, 4, 7, and 8.
- (7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses true LVDS input buffer.

RSDS, Mini-LVDS, and PPDS I/O Standard Support in Cyclone IV Devices

The RSDS, mini-LVDS, and PPDS I/O standards are used in chip-to-chip applications between the timing controller and the column drivers on the display panels such as LCD monitor panels and LCD televisions. Cyclone IV devices meet the National Semiconductor Corporation RSDS Interface Specification, Texas Instruments mini-LVDS Interface Specification, and National Semiconductor Corporation PPDS Interface Specification to support RSDS, mini-LVDS and PPDS output standards, respectively.

- ***** For Cyclone IV devices RSDS, mini-LVDS, and PPDS output electrical specifications, refer to the *Cyclone IV Device Datasheet* chapter.
- **To** For more information about the RSDS I/O standard, refer to the RSDS specification from the National Semiconductor website (www.national.com).

Designing with RSDS, Mini-LVDS, and PPDS

Cyclone IV I/O banks support RSDS, mini-LVDS, and PPDS output standards. The right I/O banks support true RSDS, mini-LVDS, and PPDS transmitters. On the top and bottom I/O banks, RSDS, mini-LVDS, and PPDS transmitters are supported using two single-ended output buffers with external resistors. The two single-ended output buffers are programmed to have opposite polarity.

Figure 6–15 shows an RSDS, mini-LVDS, or PPDS interface with a true output buffer.

Figure 6–15. Cyclone IV Devices RSDS, Mini-LVDS, or PPDS Interface with True Output Buffer on the Right I/O Banks



Figure 6–16 shows an RSDS, mini-LVDS, or PPDS interface with two single-ended output buffers and external resistors.

Figure 6–16. RSDS, Mini-LVDS, or PPDS Interface with External Resistor Network on the Top and Bottom I/O Banks (1)



Table 6–11. High-Speed I/O Timing Definitions (Part 2 of 2)

Parameter	Symbol	Description
Input jitter tolerance (peak-to-peak)	_	Allowed input jitter on the input clock to the PLL that is tolerable while maintaining PLL lock.
Output jitter (peak-to-peak)	—	Peak-to-peak output jitter from the PLL.

Note to Table 6-11:

(1) The TCCS specification applies to the entire bank of differential I/O as long as the SERDES logic is placed in the logic array block (LAB) adjacent to the output pins.

Figure 6–21. High-Speed I/O Timing Diagram



Figure 6-22 shows the Cyclone IV devices high-speed I/O timing budget.

Figure 6–22. Cyclone IV Devices High-Speed I/O Timing Budget (1)

Note to Figure 6-22:

```
(1) The equation for the high-speed I/O timing budget is:
    eriod = 0.5 \times TCCS + RSKM + SW + RSKM + 0.5 \times TCCS
```

For more information, refer to the Cyclone IV Device Datasheet chapter.

Design Guidelines

This section provides guidelines for designing with Cyclone IV devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, you must observe some restrictions on the placement of single-ended I/O pins in relation to differential pads.

IP For guidelines on placing single-ended pads with respect to differential pads in Cyclone IV devices, refer to "Pad Placement and DC Guidelines" on page 6-23.

PS Configuration Using an External Host

In the PS configuration scheme, you can use an intelligent host such as a MAX II device or microprocessor that controls the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone IV device. You can store the configuration data in **.rbf**, **.hex**, or **.ttf** format.

Figure 8–13 shows the configuration interface connections between a Cyclone IV device and an external host device for single-device configuration.

Figure 8–13. Single-Device PS Configuration Using an External Host

Notes to Figure 8-13:

- (1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. V_{CC} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host.
- (2) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect the MSEL pins, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA [0] and DCLK must fit the maximum overshoot outlined in Equation 8–1 on page 8–5.

To begin the configuration, the external host device must generate a low-to-high transition on the nCONFIG pin. When nSTATUS is pulled high, the external host device must place the configuration data one bit at a time on DATA[0]. If you use configuration data in **.rbf**, **.ttf**, or **.hex**, you must first send the LSB of each data byte. For example, if the **.rbf** contains the byte sequence 02 1B EE 01 FA, the serial bitstream you must send to the device is:

0100-0000 1101-1000 0111-0111 1000-0000 0101-1111

Cyclone IV devices receive configuration data on DATA[0] and the clock is received on DCLK. Data is latched into the device on the rising edge of DCLK. Data is continuously clocked into the target device until CONF_DONE goes high and the device enters initialization state.

Two DCLK falling edges are required after CONF_DONE goes high to begin the initialization of the device.

INIT_DONE is released and pulled high when initialization is complete. The external host device must be able to detect this low-to-high transition which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

For device using V_{CCIO} of 2.5, 3.0, and 3.3 V, refer to Figure 8–23. All I/O inputs must maintain a maximum AC voltage of 4.1 V because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using V_{CCIO} of 2.5, 3.0, and 3.3 V. You must power up the V_{CC} of the download cable with a 2.5-V supply from V_{CCA}. For device using V_{CCIO} of 1.2, 1.5, and 1.8 V, refer to Figure 8–24. You can power up the V_{CC} of the download cable with the supply from V_{CCIO}.

Notes to Figure 8-23:

- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Connect the nCONFIG and MSEL pins to support a non-JTAG configuration scheme. If you only use JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.
- (3) Pin 6 of the header is a V₁₀ reference voltage for the MasterBlaster output driver. V₁₀ must match the device's V_{CCA}. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. When using the USB-Blaster, ByteBlaster II, ByteBlasterMV, and EthernetBlaster cables, this pin is a no connect.
- (4) The nCE pin must be connected to GND or driven low for successful JTAG configuration.
- (5) The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
- (6) Power up the V_{CC} of the EthernetBlaster, ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V supply from V_{CCA} . Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.
- (7) Resistor value can vary from 1 k Ω to 10 k Ω ..

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system with JTAG BST circuitry. Figure 8–25 and Figure 8–26 show multi-device JTAG configuration.

For devices using 2.5-, 3.0-, and 3.3-V V_{CCIO} supply, you must refer to Figure 8–25. All I/O inputs must maintain a maximum AC voltage of 4.1 V because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using 2.5-, 3.0-, and 3.3- V V_{CCIO} supply. You must power up the V_{CC} of the download cable with a 2.5-V V_{CCA} supply. For device using V_{CCIO} of 1.2, 1.5 V, and 1.8 V, refer to Figure 8–26. You can power up the V_{CC} of the download cable with the supply from V_{CCIO}.

Figure 8–25. JTAG Configuration of Multiple Devices Using a Download Cable (2.5, 3.0, and 3.3-V V_{CCIO} Powering the JTAG Pins)

Notes to Figure 8-25:

- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Connect the nCONFIG and MSEL pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA [0] to either high or low, whichever is convenient on your board.
- (3) Pin 6 of the header is a V₁₀ reference voltage for the MasterBlaster output driver. V₁₀ must match the V_{CCA} of the device. For this value, refer to the MasterBlaster Serial/USB Communications Cable User Guide. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) You must connect the nCE pin to GND or driven low for successful JTAG configuration.
- (5) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.
- (6) Resistor value can vary from 1 k Ω to 10 k Ω .

Cyclone IV Device Handbook,

Volume 2

101 Innovation Drive San Jose, CA 95134 www.altera.com

CYIV-5V2-1.9

1. Cyclone IV Transceivers Architecture

Cyclone[®] IV GX devices include up to eight full-duplex transceivers at serial data rates between 600 Mbps and 3.125 Gbps in a low-cost FPGA. Table 1–1 lists the supported Cyclone IV GX transceiver channel serial protocols.

Protocol	Data Rate (Gbps)	F324 and smaller packages	F484 and larger packages
PCI Express® (PCIe [®]) ⁽¹⁾	2.5	\checkmark	\checkmark
Gbps Ethernet (GbE)	1.25	~	\checkmark
Common Public Radio Interface (CPRI)	0.6144, 1.2288, 2.4576, and 3.072	 (2) 	\checkmark
OBSAI	0.768, 1.536, and 3.072	✓ (2)	\checkmark
XAUI	3.125	—	\checkmark
Sorial digital interface (SDI)	HD-SDI at 1.485 and 1.4835	~	
Senar digitar internace (SDI)	3G-SDI at 2.97 and 2.967	—	v
Serial RapidIO [®] (SRIO)	1.25, 2.5, and 3.125	—	\checkmark
Serial Advanced Technology Attachment (SATA)	1.5 and 3.0	_	\checkmark
V-by-one	3.125		\checkmark
Display Port	1.62 and 2.7	—	\checkmark

Table 1-1.	Serial	Protocols	Supported	by the	Cyclone I	V GX	Transceiver	Channels
------------	--------	-----------	-----------	--------	------------------	------	-------------	----------

Notes to Table 1-1:

(1) Provides the physical interface for PCI Express (PIPE)-compliant interface that supports Gen1 ×1, ×2, and ×4 initial lane width configurations. When implementing ×1 or ×2 interface, remaining channels in the transceiver block are available to implement other protocols.

(2) Supports data rates up to 2.5 Gbps only.

You can implement these protocols through the ALTGX MegaWizard[™] Plug-In Manager, which also offers the highly flexible Basic functional mode to implement proprietary serial protocols at the following serial data rates:

- 600 Mbps to 2.5 Gbps for devices in F324 and smaller packages
- 600 Mbps to 3.125 Gbps for devices in F484 and larger packages

For descriptions of the ports available when instantiating a transceiver using the ALTGX megafunction, refer to "Transceiver Top-Level Port Lists" on page 1–85.

For more information about Cyclone IV transceivers that run at ≥2.97 Gbps data rate, refer to the *Cyclone IV Device Family Pin Connection Guidelines*.

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Figure 1–26. PLL Input Reference Clocks in Transceiver Operation for F484 and Larger Packages $^{(1)}$, $^{(2)}$, $^{(3)}$

Notes to Figure 1-26:

- (1) The REFCLK2 and REFCLK3 pins are dual-purpose CLKIO, REFCLK, or DIFFCLK pins that reside in banks 3A and 8A respectively.
- (2) The REFCLK[1..0] and REFCLK[5..4] pins are dual-purpose differential REFCLK or DIFFCLK pins that reside in banks 3B and 8B respectively. These clock input pins do not have access to the clock control blocks and GCLK networks. For more details, refer to the *Clock Networks and PLLs in Cyclone IV Devices* chapter.
- (3) Using any clock input pins other than the designated REFCLK pins as shown here to drive the MPLLs and GPLLs may have reduced jitter performance.

The input reference clocks reside in banks 3A, 3B, 8A, and 8B have dedicated $V_{CC_CLKIN3A}$, $V_{CC_CLKIN3B}$, $V_{CC_CLKIN8A}$, and $V_{CC_CLKIN8B}$ power supplies separately in their respective I/O banks to avoid the different power level requirements in the same bank for general purpose I/Os (GPIOs). Table 1–6 lists the supported I/O standard for the REFCLK pins.

	ЦССІ		Torminatio	VCC_	CLKIN Level	I/O Pin Type		
I/O Standard	Protocol	Coupling	n	Input	Output	Column I/O	Row I/O	Supported Banks
LVDS	ALL	Differential	Off-chip	2.5 V	Not Supported	Yes	No	3A, 3B, 8A, 8B
LVPECL	ALL	AC (Needs off-chip resistor to restore	Off-chip	2.5 V	Not Supported	Yes	No	3A, 3B, 8A, 8B
1.2 V, 1.5 V, 3 3 V PCMI	ALL		Off-chip	2.5 V	Not Supported	Yes	No	3A, 3B, 8A, 8B
	ALL		Off-chip	2.5 V	Not Supported	Yes	No	3A, 3B, 8A, 8B
	ALL	V _{CM})	Off-chip	2.5 V	Not Supported	Yes	No	3A, 3B, 8A, 8B
HCSL	PCle	Differential DC	Off-chip	2.5 V	Not Supported	Yes	No	3A, 3B, 8A, 8B

Table 1–6. REFCLK I/O Standard Support

The CDR unit in each receiver channel gets the CDR clocks from one of the two multipurpose PLLs directly adjacent to the transceiver block. The CDR clocks distribution network is segmented by bidirectional tri-state buffers as shown in Figure 1–29 and Figure 1–30. This requires the CDR clocks from either one of the two multipurpose PLLs to drive a number of contiguous segmented paths to reach the intended receiver channel. Interleaving the CDR clocks from the two multipurpose PLLs is not supported.

For example, based on Figure 1–29, a combination of MPLL_1 driving receiver channels 0, 1, and 3, while MPLL_2 driving receiver channel 2 is not supported. In this case, only one multipurpose PLL can be used for the receiver channels.

Figure 1–29. CDR Clocking for Transceiver Channels in F324 and Smaller Packages

Note to Figure 1-29:

(1) Transceiver channels 2 and 3 are not available for devices in F169 and smaller packages.

Figure 1–30. CDR Clocking for Transceiver Channels in F484 and Larger Packages

Figure 1–50 and Figure 1–51 show the detection mechanism example for a successful and unsuccessful receiver detection scenarios respectively. The tx_forceelecidle port must be asserted at least 10 parallel clock cycles prior to assertion of tx_detectrxloop port to ensure the transmitter buffer is properly tri-stated. Detection completion is indicated by pipephydonestatus assertion, with detection successful indicated by 3'b011 on pipestatus[2..0] port, or detection unsuccessful by 3'b000 on pipestatus[2..0] port.

Figure 1–51. Example of Unsuccessful Receiver Detect Operation

powerdown[10]	2'b10(P1)
tx_detectrxloopback	
pipephydonestatus	
pipestatus[20]	Х З'ю000

Electrical Idle Control

The Cyclone IV GX transceivers support transmitter buffer in electrical idle state using the tx_forceelecidle port. During electrical idle, the transmitter buffer differential and common mode output voltage levels are compliant to the PCIe Base Specification 2.0 for Gen1 signaling rate.

Figure 1–52 shows the relationship between assertion of the $tx_forceelecidle$ port and the transmitter buffer output on the $tx_dataout$ port.

Figure 1–52. Transmitter Buffer Electrical Idle State

Notes to Figure 1-52:

- (1) The protocol requires the transmitter buffer to transition to a valid electrical idle after sending an electrical idle ordered set within 8 ns.
- (2) The protocol requires transmitter buffer to stay in electrical idle for a minimum of 20 ns for Gen1 signaling rate.

Port Name	Input/ Output	Description				
		This signal is always available for you to select in the Channel reconfiguration screen. This signal is applicable only in the dynamic reconfiguration modes grouped under Channel reconfiguration mode including channel interface and Use RX local divider option.				
reconfig_address _out[50]	Output	This signal represents the current address used by the ALTGX_RECONFIG instance when writing the .mif into the transceiver channel. This signal increments by 1, from 0 to the last address, then starts at 0 again. You can use this signal to indicate the end of all the .mif write transactions (reconfig_address_out[50] changes from the last address to 0 at the end of all the .mif write transactions).				
reconfig_address	Outout	This is an optional signal you can select in the Channel reconfiguration screen. This signal is applicable only in dynamic reconfiguration modes grouped under the Channel reconfiguration option.				
_en	Output	The dynamic reconfiguration controller asserts reconfig_address_en to indicate that reconfig_address_out [50] has changed. This signal is asserted only after the dynamic reconfiguration controller completes writing one 16-bit word of the .mif .				
reset_reconfig_ address	Input	This is an optional signal you can select in the Channel reconfiguration screen. This signal is applicable only in dynamic reconfiguration modes grouped under the Channel reconfiguration option.				
		Enable this signal and assert it for one reconfig_clk clock cycle if you want to reset the reconfiguration address used by the ALTGX_RECONFIG instance during reconfiguration.				
reconfig_data [150]	Input	This signal is applicable only in the dynamic reconfiguration modes grouped under the Channel reconfiguration option. This is a 16-bit word carrying the reconfiguration information. It is stored in a .mif that you must generate. The ALTGX_RECONFIG instance requires that you provide reconfig_data [150] on every .mif write transaction using the write_all signal.				
reconfig_reset ⁽⁴⁾	Input	You can use this signal to reset all the reconfiguration process in Channel reconfiguration mode. Asserting this port will reset all the register in the reconfiguration controller logics. This port only shows up in Channel reconfiguration mode.				
		If you are feeding into this port, synchronize the reset signal to the $\tt reconfig_clk$ domain.				
channel_reconfig _done	Output	This signal goes high to indicate that the dynamic reconfiguration controller has finished writing all the words of the .mif . The channel_reconfig_done signal is automatically deasserted at the start of a new dynamic reconfiguration write sequence. This signal is applicable only in channel reconfiguration mode.				

Table 3–2. Dynamic Reconfiguration Controller Port List (ALTGX_RECONFIG Instance) (Part 7 of 7)

Notes to Table 3-2:

(1) Not all combinations of input bits are legal values.

(2) This setting is required for compliance to PCI Express® (PIPE) functional mode.

(3) PLL reconfiguration is performed using ALTPLL_RECONFIG controller. Hence it is not selected through the reconfig_mode_sel[2..0] port.

(4) reconfig_reset will not restart the offset cancellation operation. Offset cancellation only occurs one time after power up and does not occur when subsequent reconfig_reset is asserted.

Offset Cancellation Feature

The Cyclone IV GX devices provide an offset cancellation circuit per receiver channel to counter the offset variations due to process, voltage, and temperature (PVT). These variations create an offset in the analog circuit voltages, pushing them out of the expected range. In addition to reconfiguring the transceiver channel, the dynamic reconfiguration controller performs offset cancellation on all receiver channels connected to it on power up.

The following are the channel reconfiguration mode options:

- Channel interface reconfiguration
- Data rate division at receiver channel

Channel Interface Reconfiguration Mode

Enable this option if the reconfiguration of the transceiver channel involves the following changes:

- The reconfigured channel has a changed FPGA fabric-Transceiver channel interface data width
- The reconfigured channel has changed input control signals and output status signals
- The reconfigured channel has enabled and disabled the static PCS blocks of the transceiver channel

The following are the new input signals available when you enable this option:

- tx_datainfull—the width of this input signal depends on the number of channels you set up in the ALTGX MegaWizard Plug-In Manager. It is 22 bits wide per channel. This signal is available only for Transmitter only and Receiver and Transmitter configurations. This port replaces the existing tx_datain port.
- rx_dataoutfull—the width of this output signal depends on the number of channels you set up in the ALTGX MegaWizard Plug-In Manager. It is 32 bits wide per channel. This signal is available only for **Receiver only** and **Receiver and Transmitter** configurations. This port replaces the existing rx_dataout port.

The Quartus II software has legality checks for the connectivity of tx_datainfull and rx_dataoutfull and the various control and status signals you enable in the **Clocking/Interface** screen. For example, the Quartus II software allows you to select and connect the pipestatus and powerdn signals. It assumes that you are planning to switch to and from PCI Express (PIPE) functional mode.

If you are reconfiguring the multipurpose PLL with a different M counter value, follow these steps:

- 1. During transceiver PLL reconfiguration, assert tx_digitalreset, rx_digitalreset, and rx_analogreset signals.
- 2. Perform PLL reconfiguration to update the multipurpose PLL with the PLL **.mif** files.
- 3. Perform channel reconfiguration and update the transceiver with the GXB reconfiguration **.mif** files. If you have multiple channel instantiations connected to the same multipurpose PLL, reconfigure each channel.
- 4. Deassert tx_digitalreset and rx_analogreset signals.
- 5. After the rx_freqlocked signal goes high, wait for at least 4 µs, and then deassert the rx_digitalreset signal.

Error Indication During Dynamic Reconfiguration

The ALTGX_RECONFIG MegaWizard Plug-In Manager provides an error status signal when you select the **Enable illegal mode checking** option or the **Enable self recovery** option in the **Error checks/data rate switch** screen. The conditions under which the error signal is asserted are:

- Enable illegal mode checking option—when you select this option, the dynamic reconfiguration controller checks whether an attempted operation falls under one of the conditions listed below. The dynamic reconfiguration controller detects these conditions within two reconfig_clk cycles, deasserts the busy signal, and asserts the error signal for two reconfig_clk cycles.
 - PMA controls, read operation—none of the output ports (rx_eqctrl_out, rx_eqdcgain_out, tx_vodctrl_out, and tx_preemp_out) are selected in the ALTGX_RECONFIG instance and the read signal is asserted.
 - PMA controls, write operation—none of the input ports (rx_eqctrl, rx_eqdcgain, tx_vodctrl, and tx_preemp) are selected in the ALTGX_RECONFIG instance and the write_all signal is asserted.
- Channel reconfiguration and PMA reconfiguration mode select read operation option:
 - The reconfig_mode_sel input port is set to 3'b001 (Channel reconfiguration mode)
 - The read signal is asserted
- Enable self recovery option—when you select this option, the ALTGX_RECONFIG MegaWizard Plug-In Manager provides the error output port. The dynamic reconfiguration controller quits an operation if it did not complete within the expected number of clock cycles. After recovering from the illegal operation, the dynamic reconfiguration controller deasserts the busy signal and asserts the error output port for two reconfig_clk cycles.
- The error signal is not asserted when an illegal value is written to any of the PMA controls.

Figure 1–4 shows the differential receiver input waveform.

Figure 1–5 shows the transmitter output waveform.

Table 1–22 lists the typical V_{OD} for Tx term that equals 100 Ω .

Table 1–22. Typical V_{0D} Setting, Tx Term = 100 Ω

Sumbol	V _{oD} Setting (mV)						
Symbol	1	2	3	4 (1)	5	6	
V _{OD} differential peak to peak typical (mV)	400	600	800	900	1000	1200	

Note to Table 1-22:

(1) This setting is required for compliance with the PCIe protocol.

Document Revision History

Table 1–47 lists the revision history for this chapter.

	Table 1-47.	Document	Revision	History
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Date	Version	Changes		
December 2016	2.1	Added note to Table 1–9 and Table 1–10.		
March 2016	2.0	Updated note (5) in Table 1–21 to remove support for the N148 package.		
October 2014	10	Updated maximum value for V _{CCD_PLL} in Table 1–1.		
	1.9	Removed extended temperature note in Table 1–3.		
December 2013	1.8	Updated Table 1–21 by adding Note (15).		
May 2013	1.7	Updated Table 1–15 by adding Note (4).		
	1.6	■ Updated the maximum value for V _I , V _{CCD_PLL} , V _{CCIO} , V _{CC_CLKIN} , V _{CCH_GXB} , and V _{CCA_GXB} Table 1–1.		
		■ Updated Table 1–11 and Table 1–22.		
October 2012		 Updated Table 1–21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock. 		
		■ Updated Table 1–29 to include the typical DCLK value.		
		 Updated the minimum f_{HSCLK} value in Table 1–31, Table 1–32, Table 1–33, Table 1–34, and Table 1–35. 		
November 2011	1.5	 Updated "Maximum Allowed Overshoot or Undershoot Voltage", "Operating Conditions", and "PLL Specifications" sections. 		
		■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21.		
		■ Updated Figure 1–1.		
	1.4	 Updated for the Quartus II software version 10.1 release. 		
December 2010		■ Updated Table 1–21 and Table 1–25.		
		Minor text edits.		
July 2010	1.3	Updated for the Quartus II software version 10.0 release:		
		■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45.		
		■ Updated Figure 1–2 and Figure 1–3.		
		Removed SW Requirement and TCCS for Cyclone IV Devices tables.		
		 Minor text edits. 		
March 2010	1.2	Updated to include automotive devices:		
		 Updated the "Operating Conditions" and "PLL Specifications" sections. 		
		■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43.		
		Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os.		
		 Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices. 		
		 Minor text edits. 		