### Intel - EP4CE75F23C7N Datasheet





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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

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#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	4713
Number of Logic Elements/Cells	75408
Total RAM Bits	2810880
Number of I/O	292
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce75f23c7n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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### Chapter 5. Clock Networks and PLLs in Cyclone IV Devices

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**To** For more information, refer to the *External Memory Interfaces in Cyclone IV Devices* chapter.

## Configuration

Cyclone IV devices use SRAM cells to store configuration data. Configuration data is downloaded to the Cyclone IV device each time the device powers up. Low-cost configuration options include the Altera EPCS family serial flash devices and commodity parallel flash configuration options. These options provide the flexibility for general-purpose applications and the ability to meet specific configuration and wake-up time requirements of the applications.

Table 1–9 lists which configuration schemes are supported by Cyclone IV devices.

Table 1–9. Configuration Schemes for Cyclone IV Device Family

Devices	Supported Configuration Scheme
Cyclone IV GX	AS, PS, JTAG, and FPP (1)
Cyclone IV E	AS, AP, PS, FPP, and JTAG

Note to Table 1-9:

(1) The FPP configuration scheme is only supported by the EP4CGX30F484 and EP4CGX50/75/110/150 devices.

IEEE 1149.6 (AC JTAG) is supported on all transceiver I/O pins. All other pins support IEEE 1149.1 (JTAG) for boundary scan testing.

For more information, refer to the *JTAG Boundary-Scan Testing for Cyclone IV Devices* chapter.

For Cyclone IV GX devices to meet the PCIe 100 ms wake-up time requirement, you must use passive serial (PS) configuration mode for the EP4CGX15/22/30 devices and use fast passive parallel (FPP) configuration mode for the EP4CGX30F484 and EP4CGX50/75/110/150 devices.

For more information, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.

The cyclical redundancy check (CRC) error detection feature during user mode is supported in all Cyclone IV GX devices. For Cyclone IV E devices, this feature is only supported for the devices with the core voltage of 1.2 V.



For more information about CRC error detection, refer to the *SEU Mitigation in Cyclone IV Devices* chapter.

## High-Speed Transceivers (Cyclone IV GX Devices Only)

Cyclone IV GX devices contain up to eight full duplex high-speed transceivers that can operate independently. These blocks support multiple industry-standard communication protocols, as well as Basic mode, which you can use to implement your own proprietary protocols. Each transceiver channel has its own pre-emphasis and equalization circuitry, which you can set at compile time to optimize signal integrity and reduce bit error rates. Transceiver blocks also support dynamic reconfiguration, allowing you to change data rates and protocols on-the-fly.

# **Document Revision History**

Table 1–10 lists the revision history for this chapter.

### Table 1–10. Document Revision History

Date	Version	Changes
March 2016	2.0	■ Updated Table 1–4 and Table 1–5 to remove support for the N148 package.
March 2016	2.0	■ Updated Figure 1–2 to remove support for the N148 package.
April 2014	1.9	Updated "Packaging Ordering Information for the Cyclone IV E Device".
May 2013	1.8	Updated Table 1–3, Table 1–6 and Figure 1–3 to add new device options and packages.
February 2013	1.7	Updated Table 1–3, Table 1–6 and Figure 1–3 to add new device options and packages.
October 2012	1.6	Updated Table 1–3 and Table 1–4.
November 2011	1.5	<ul> <li>Updated "Cyclone IV Device Family Features" section.</li> </ul>
	1.5	■ Updated Figure 1–2 and Figure 1–3.
		<ul> <li>Updated for the Quartus II software version 10.1 release.</li> </ul>
	1.4	<ul> <li>Added Cyclone IV E new device package information.</li> </ul>
December 2010		■ Updated Table 1–1, Table 1–2, Table 1–3, Table 1–5, and Table 1–6.
		■ Updated Figure 1–3.
		<ul> <li>Minor text edits.</li> </ul>
July 2010	1.3	Updated Table 1–2 to include F484 package information.
		■ Updated Table 1–3 and Table 1–6.
March 2010	1.2	■ Updated Figure 1–3.
		<ul> <li>Minor text edits.</li> </ul>
		<ul> <li>Added Cyclone IV E devices in Table 1–1, Table 1–3, and Table 1–6 for the Quartus II software version 9.1 SP1 release.</li> </ul>
	10 1.1	<ul> <li>Added the "Cyclone IV Device Family Speed Grades" and "Configuration" sections.</li> </ul>
February 2010		<ul> <li>Added Figure 1–3 to include Cyclone IV E Device Packaging Ordering Information.</li> </ul>
		■ Updated Table 1–2, Table 1–4, and Table 1–5 for Cyclone IV GX devices.
		<ul> <li>Minor text edits.</li> </ul>
November 2009	1.0	Initial release.

### **Read or Write Clock Mode**

Cyclone IV devices M9K memory blocks can implement read or write clock mode for FIFO and simple dual-port memories. In this mode, a write clock controls the data inputs, write address, and wren registers. Similarly, a read clock controls the data outputs, read address, and rden registers. M9K memory blocks support independent clock enables for both the read and write clocks.

When using read or write mode, if you perform a simultaneous read or write to the same address location, the output read data is unknown. If you require the output data to be a known value, use either single-clock mode, input clock mode, or output clock mode and choose the appropriate read-during-write behavior in the MegaWizard Plug-In Manager.

## **Single-Clock Mode**

Cyclone IV devices M9K memory blocks can implement single-clock mode for FIFO, ROM, true dual-port, simple dual-port, and single-port memories. In this mode, you can control all registers of the M9K memory block with a single clock together with clock enable.

## **Design Considerations**

This section describes designing with M9K memory blocks.

## **Read-During-Write Operations**

"Same-Port Read-During-Write Mode" on page 3–16 and "Mixed-Port Read-During-Write Mode" on page 3–16 describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address.

There are two read-during-write data flows: same-port and mixed-port. Figure 3–13 shows the difference between these flows.





Figure 5–11 shows the external clock outputs for PLLs.





#### Notes to Figure 5-11:

- (1) These external clock enable signals are available only when using the ALTCLKCTRL megafunction.
- (2) PLL#\_CLKOUTp and PLL#\_CLKOUTn pins are dual-purpose I/O pins that you can use as one single-ended clock output or one differential clock output. When using both pins as single-ended I/Os, one of them can be the clock output while the other pin is configured as a regular user I/O.

Each pin of a differential output pair is 180° out of phase. The Quartus II software places the NOT gate in your design into the I/O element to implement 180° phase with respect to the other pin in the pair. The clock output pin pairs support the same I/O standards as standard output pins.

**To** determine which I/O standards are supported by the PLL clock input and output pins, refer to the *Cyclone IV Device I/O Features* chapter.

Cyclone IV PLLs can drive out to any regular I/O pin through the GCLK. You can also use the external clock output pins as GPIO pins if external PLL clocking is not required.

# **High-Speed I/O Interface**

Cyclone IV E I/Os are separated into eight I/O banks, as shown in Figure 6–9 on page 6–17. Cyclone IV GX I/Os are separated into six user I/O banks with the left side of the device as the transceiver block, as shown in Figure 6–10 on page 6–18. Each bank has an independent power supply. True output drivers for LVDS, RSDS, mini-LVDS, and PPDS are on the right I/O banks. On the Cyclone IV E row I/O banks and the Cyclone IV GX right I/O banks, some of the differential pin pairs (p and n pins) of the true output drivers are not located on adjacent pins. In these cases, a power pin is located between the p and n pins. These I/O standards are also supported on all I/O banks using two single-ended output with the second output programmed as inverted, and an external resistor network. True input buffers for these I/O standards are supported on the top, bottom, and right I/O banks except for I/O bank 9.

Table 6–6 and Table 6–7 summarize which I/O banks support these I/O standards in the Cyclone IV device family.

Differential I/O Standards	I/O Bank Location	External Resistor Network at Transmitter	Transmitter (TX)	Receiver (RX)	
	1,2,5,6	Not Required			
	All	Three Resistors	<b>↓</b>	~	
	1,2,5,6	Not Required			
RSDS	3,4,7,8	Three Resistors	✓	_	
	All	Single Resistor			
	1,2,5,6	Not Required		_	
	All	Three Resistors	•		
פחסס	1,2,5,6	Not Required			
FFUS	All	Three Resistors	<b>`</b>		
BLVDS (1)	All	Single Resistor	~	$\checkmark$	
LVPECL (2)	All	—	—	$\checkmark$	
Differential SSTL-2 <sup>(3)</sup>	All	—	$\checkmark$	$\checkmark$	
Differential SSTL-18 <sup>(3)</sup>	All	—	$\checkmark$	$\checkmark$	
Differential HSTL-18 (3)	All	—	$\checkmark$	$\checkmark$	
Differential HSTL-15 (3)	All	_	~	$\checkmark$	
Differential HSTL-12 <sup>(3)</sup> , <sup>(4)</sup>	All	_	✓	✓	

#### Notes to Table 6-6:

(1) Transmitter and Receiver f<sub>MAX</sub> depend on system topology and performance requirement.

(2) The LVPECL I/O standard is only supported on dedicated clock input pins.

(3) The differential SSTL-2, SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards are only supported on clock input pins and PLL output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-15, and HSTL-12 I/O standards.

(4) Differential HSTL-12 Class II is supported only in column I/O banks.

Figure 7–2 shows the location and numbering of the DQS, DQ, or CQ# pins in the Cyclone IV GX I/O banks.



Figure 7–2. DQS, CQ, or CQ# Pins in Cyclone IV GX I/O Banks <sup>(1)</sup>

#### Note to Figure 7–2:

(1) The DQS, CQ, or CQ# pin locations in this diagram apply to all packages in Cyclone IV GX devices except devices in 169-pin FBGA and 324-pin FBGA.

Figure 7–9 illustrates how the second output enable register extends the DQS high-impedance state by half a clock cycle during a write operation.



#### Figure 7–9. Extending the OE Disable by Half a Clock Cycle for a Write Transaction <sup>(1)</sup>

#### Note to Figure 7-9:

(1) The waveform reflects the software simulation result. The OE signal is an active low on the device. However, the Quartus II software implements the signal as an active high and automatically adds an inverter before the A<sub>OE</sub> register D input.

### **OCT** with Calibration

Cyclone IV devices support calibrated on-chip series termination ( $R_S$  OCT) in both vertical and horizontal I/O banks. To use the calibrated OCT, you must use the RUP and RDN pins for each  $R_S$  OCT control block (one for each side). You can use each OCT calibration block to calibrate one type of termination with the same  $V_{CCIO}$  for that given side.

 For more information about the Cyclone IV devices OCT calibration block, refer to the Cyclone IV Device I/O Features chapter.

### PLL

When interfacing with external memory, the PLL is used to generate the memory system clock, the write clock, the capture clock and the logic-core clock. The system clock generates the DQS write signals, commands, and addresses. The write-clock is shifted by -90° from the system clock and generates the DQ signals during writes. You can use the PLL reconfiguration feature to calibrate the read-capture phase shift to balance the setup and hold margins.

- The PLL is instantiated in the ALTMEMPHY megafunction. All outputs of the PLL are used when the ALTMEMPHY megafunction is instantiated to interface with external memories. PLL reconfiguration is used in the ALTMEMPHY megafunction to calibrate and track the read-capture phase to maintain the optimum margin.
- **For more information about usage of PLL outputs by the ALTMEMPHY** megafunction, refer to the *External Memory Interface Handbook*.

- 3. Click the **Configuration** tab.
- 4. Turn on Generate compressed bitstreams.
- 5. Click OK.
- 6. In the **Settings** dialog box, click **OK**.

You can enable compression when creating programming files from the **Convert Programming Files** dialog box. To enable compression, perform the following steps:

- 1. On the File menu, click Convert Programming Files.
- 2. Under **Output programming file**, select your desired file type from the **Programming file type** list.
- 3. If you select **Programmer Object File (.pof)**, you must specify the configuration device in the **Configuration device** list.
- 4. Under Input files to convert, select SOF Data.
- 5. Click Add File to browse to the Cyclone IV device SRAM object files (.sof).
- 6. In the **Convert Programming Files** dialog box, select the **.pof** you added to **SOF Data** and click **Properties**.
- 7. In the SOF File Properties dialog box, turn on the Compression option.

When multiple Cyclone IV devices are cascaded, you can selectively enable the compression feature for each device in the chain. Figure 8–1 shows a chain of two Cyclone IV devices. The first device has compression enabled and receives compressed bitstream from the configuration device. The second device has the compression feature disabled and receives uncompressed data. You can generate programming files for this setup in the **Convert Programming Files** dialog box.

Figure 8–1. Compressed and Uncompressed Configuration Data in the Same Configuration File



### **Configuration Requirement**

This section describes Cyclone IV device configuration requirement and includes the following topics:

- "Power-On Reset (POR) Circuit" on page 8–4
- "Configuration File Size" on page 8–4
- "Power Up" on page 8–6

devices. The internal oscillator is designed to ensure that its maximum frequency is guaranteed to meet EPCS device specifications. Cyclone IV devices offer the option to select CLKUSR as the external clock source for DCLK. You can change the clock source option in the Quartus II software in the **Configuration** tab of the **Device and Pin Options** dialog box.

P

EPCS1 does not support Cyclone IV devices because of its insufficient memory capacity.

Table 8-6. AS DCLK Output Frequency

Oscillator	Minimum	Typical	Maximum	Unit
40 MHz	20	30	40	MHz

In configuration mode, the Cyclone IV device enables the serial configuration device by driving the nCSO output pin low, which connects to the nCS pin of the configuration device. The Cyclone IV device uses the DCLK and DATA[1] pins to send operation commands and read address signals to the serial configuration device. The configuration device provides data on its DATA pin, which connects to the DATA[0] input of the Cyclone IV device.

All AS configuration pins (DATA[0], DCLK, nCSO, and DATA[1]) have weak internal pullup resistors that are always active. After configuration, these pins are set as input tristated and are driven high by the weak internal pull-up resistors.

The timing parameters for AS mode are not listed here because the  $t_{CF2CD}$ ,  $t_{CF2ST0}$ ,  $t_{CFG}$ ,  $t_{STATUS}$ ,  $t_{CF2ST1}$ , and  $t_{CD2UM}$  timing parameters are identical to the timing parameters for PS mode shown in Table 8–12 on page 8–36.

four devices. During the first configuration cycle, the master device reads its configuration data from the serial configuration device while holding nCEO high. After completing its configuration cycle, the master device drives nCE low and sends the second copy of the configuration data to all three slave devices, configuring them simultaneously.

The advantage of the setup in Figure 8–4 is that you can have a different **.sof** for the master device. However, all the slave devices must be configured with the same **.sof**. You can either compress or uncompress the **.sof** in this configuration method.

You can still use this method if the master and slave devices use the same **.sof**.

Gumbal	Deveneter	Minimum		Maximum		11 14	
Symbol	Parameter	Cyclone IV (1) Cyclone IV E (4)		Cyclone IV <sup>(1)</sup>	Cyclone IV E <sup>(2)</sup>	UNIC	
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	_	_	230 (4)		μs	
t <sub>сғ2ск</sub>	nCONFIG high to first rising edge on DCLK	230	(3)	_		μs	
t <sub>sт2СК</sub>	nSTATUS high to first rising edge of DCLK	2		_		μs	
t <sub>DH</sub>	Data hold time after rising edge on DCLK	0 —		_	ns		
t <sub>cd2UM</sub>	CONF_DONE high to user mode (5)	300		650		μs	
t <sub>cd2cu</sub>	CONF_DONE high to CLKUSR enabled	$4 \times maximum DCLK period$		-			
t <sub>cd2UMC</sub>	CONF_DONE high to user mode with <b>CLKUSR</b> option on	t <sub>CD2CU</sub> + (3,192 × CLKUSR period)			_		
t <sub>DSU</sub>	Data setup time before rising edge on DCLK	5	8	_	_	ns	
t <sub>CH</sub>	DCLK high time	3.2	6.4	—	—	ns	
t <sub>CL</sub>	DCLK low time	3.2	6.4	_	_	ns	
t <sub>CLK</sub>	DCLK period	7.5	15		_	ns	
f <sub>MAX</sub>	DCLK frequency (6)			133	66	MHz	

Table 8–12. PS Configuration Timing Parameters For Cyclone IV Devices (Part 2
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#### Notes to Table 8-12:

(1) Applicable for Cyclone IV GX and Cyclone IV E devices with 1.2-V core voltage.

(2) Applicable for Cyclone IV E devices with 1.0-V core voltage.

(3) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(4) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(5) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for starting the device.

(6) Cyclone IV E devices with 1.0-V core voltage have slower F<sub>MAX</sub> when compared with Cyclone IV GX devices with 1.2-V core voltage.

### **PS Configuration Using a Download Cable**

In this section, the generic term "download cable" includes the Altera USB-Blaster USB port download cable, MasterBlaster<sup>™</sup> serial and USB communications cable, ByteBlaster II parallel port download cable, the ByteBlasterMV<sup>™</sup> parallel port download cable, and the EthernetBlaster communications cable.

In the PS configuration with a download cable, an intelligent host (such as a PC) transfers data from a storage device to the Cyclone IV device through the download cable.

JTAG instructions have precedence over any other configuration modes. Therefore, JTAG configuration can take place without waiting for other configuration modes to complete. For example, if you attempt JTAG configuration in Cyclone IV devices during PS configuration, PS configuration terminates and JTAG configuration begins. If the MSEL pins are set to AS mode, the Cyclone IV device does not output a DCLK signal when JTAG configuration takes place.

The four required pins for a device operating in JTAG mode are TDI, TDO, TMS, and TCK. All the JTAG input pins are powered by the  $V_{CCIO}$  pin and support the LVTTL I/O standard only. All user I/O pins are tri-stated during JTAG configuration. Table 8-14 explains the function of each JTAG pin.

**Pin Name Pin Type** Description Serial input pin for instructions as well as test and programming data. Data shifts in on the Test data rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry is TDI disabled by connecting this pin to  $V_{CC}$ . TDI pin has weak internal pull-up resistors (typically 25 input kΩ). Serial data output pin for instructions as well as test and programming data. Data shifts out on Test data the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the TDO output JTAG interface is not required on the board, the JTAG circuitry is disabled by leaving this pin unconnected. Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions in the state machine occur on the rising edge of TCK. Therefore, Test mode TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. TMS select If the JTAG interface is not required on the board, the JTAG circuitry is disabled by connecting this pin to  $V_{CC}$ . TMS pin has weak internal pull-up resistors (typically 25 k $\Omega$ ). The clock input to the BST circuitry. Some operations occur at the rising edge, while others Test clock occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry TCK input

Table 8–14. Dedicated JTAG Pins

You can download data to the device through the USB-Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV download cable, or the EthernetBlaster communications cable during JTAG configuration. Configuring devices with a cable is similar to programming devices in-system. Figure 8-23 and Figure 8-24 show the JTAG configuration of a single Cyclone IV device.

is disabled by connecting this pin to GND. The TCK pin has an internal weak pull-down resistor.

synchronization state machine mode. In bit-slip mode, you can dynamically enable the receiver bit reversal using the rx\_revbitorderwa port. When enabled, the 8-bit or 10-bit data D[7..0] or D[9..0] at the output of the word aligner is rewired to D[0..7] or D[0..9] respectively. Figure 1–20 shows the receiver bit reversal feature.





#### Note to Figure 1-20:

(1) The rx\_revbitordwa port is dynamic and is only available when the word aligner is configured in bit-slip mode.

- When using the receiver bit reversal feature to receive MSB-to-LSB transmission, reversal of the word alignment pattern is required.
- Receiver bit-slip indicator—provides the number of bits slipped in the word aligner for synchronization with rx\_bitslipboundaryselectout signal. For usage details, refer to "Receive Bit-Slip Indication" on page 1–76.

### **Deskew FIF0**

This module is only available when used for the XAUI protocol and is used to align all four channels to meet the maximum skew requirement of 40 UI (12.8 ns) as seen at the receiver of the four lanes. The deskew operation is compliant to the PCS deskew state machine diagram specified in clause 48 of the IEEE P802.3ae specification.

The deskew circuitry consists of a 16-word deep deskew FIFO in each of the four channels, and control logics in the central control unit of the transceiver block that controls the deskew FIFO write and read operations in each channel.

For details about the deskew FIFO operations for channel deskewing, refer to "XAUI Mode" on page 1–67.

Figure 1–69 shows the transceiver configuration in SDI mode.



Figure 1–69. Transceiver Configuration in SDI Mode

Altera recommends driving rx\_bitslip port low in configuration where low-latency PCS is not enabled. In SDI systems, the word alignment and framing occurs after descrambling, which is implemented in the user logic. The word alignment therefore is not useful, and keeping rx\_bitslip port low avoids the word aligner from inserting bits in the received data stream.

# Loopback

Cyclone IV GX devices provide three loopback options that allow you to verify the operation of different functional blocks in the transceiver channel. The following loopback modes are available:

- reverse parallel loopback (available only for PIPE mode)
- serial loopback (available for all modes except PIPE mode)
- reverse serial loopback (available for all modes except XAUI mode)

In each loopback mode, all transmitter buffer and receiver buffer settings are available if the buffers are active, unless stated otherwise.

Figure 3–9 shows the connection for PMA reconfiguration mode.



(1) This block can be reconfigured in PMA reconfiguration mode.

## **Transceiver Channel Reconfiguration Mode**

You can dynamically reconfigure the transceiver channel from an existing functional mode to a different functional mode by selecting the **Channel Reconfiguration** option in ALTGX and ALTGX\_RECONFIG MegaWizards. The blocks that are reconfigured by channel reconfiguration mode are the PCS and RX PMA blocks of a transceiver channel.

For more information about reconfiguring the RX PMA blocks of the transceiver channel using channel reconfiguration mode, you can refer to "Data Rate Reconfiguration Mode Using RX Local Divider" on page 3–26.

In channel reconfiguration, only a write transaction can occur; no read transactions are allowed. You can optionally choose to trigger write\_all once by selecting the continuous write operation in the ALTGX\_RECONFIG MegaWizard Plug-In Manager. The Quartus II software then continuously writes all the words required for reconfiguration.

For channel reconfiguration, **.mif** files are required to dynamically reconfigure the transceivers channels in channel reconfiguration modes. The **.mif** carries the reconfiguration information that will be used to reconfigure the transceivers channel dynamically on-the-fly. The **.mif** contents is generated automatically when you select the **Generate GXB Reconfig MIF** option in the Quartus II software setting. For different **.mif** settings, you need to later reconfigure and recompile the ALTGX MegaWizard to generate the **.mif** based on the required reconfiguration settings.

The dynamic reconfiguration controller can optionally perform a continuos write operation or a regular write operation of the **.mif** contents in terms of word size (16-bit data) to the transceivers channel that is selected for reconfiguration.

### Figure 3–9. ALTGX and ALTGX\_RECONFIG Connection for PMA Reconfiguration Mode

### **Option 1: Share a Single Transmitter Core Clock Between Receivers**

- Enable this option if you want tx\_clkout of the first channel (channel 0) of the transceiver block to provide the read clock to the Receive Phase Compensation FIFOs of the remaining receiver channels in the transceiver block.
- This option is typically enabled when all the channels of a transceiver block are in a Basic or Protocol configuration with rate matching enabled and are reconfigured to another Basic or Protocol configuration with rate matching enabled.

Figure 3–13 shows the sharing of channel 0's tx\_clkout between all four channels of a transceiver block.





A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
		V <sub>1</sub> = 4.20	100	%
		V <sub>1</sub> = 4.25	98	%
V <sub>i</sub> AC Input Voltage	V <sub>1</sub> = 4.30	65	%	
	V <sub>1</sub> = 4.35	43	%	
	V <sub>1</sub> = 4.40	29	%	
	V <sub>1</sub> = 4.45	20	%	
		$V_1 = 4.50$	13	%
		V <sub>1</sub> = 4.55	9	%
		$V_1 = 4.60$	6	%

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.





# **Transceiver Performance Specifications**

Table 1–21 lists the Cyclone IV GX transceiver specifications.

Table 1-21.	Transceiver Specification	for Cyclone IV GX Devices	(Part 1 of 4)
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Symbol/ Description	Conditions	C6		C7, I7			C8			<b>U</b> 14		
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	
Reference Clock												
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL											
Input frequency from REFCLK input pins		50	_	156.25	50	_	156.25	50	_	156.25	MHz	
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	_	33	30	_	33	30	_	33	kHz	
Spread-spectrum downspread	PIPE mode	_	0 to 0.5%	_	_	0 to 0.5%	_	_	0 to 0.5%	_	_	
Peak-to-peak differential input voltage	_	0.1	_	1.6	0.1	_	1.6	0.1	_	1.6	V	
V <sub>ICM</sub> (AC coupled)		1100 ± 5%		1100 ± 5%			1100 ± 5%		mV			
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	250	_	550	mV	
Transmitter REFCLK Phase Noise <sup>(1)</sup>	Frequency offset = 1 MHz – 8 MHZ	_	_	-123	_	_	-123	_	_	-123	dBc/Hz	
Transmitter REFCLK Total Jitter <sup>(1)</sup>		_	_	42.3	_	_	42.3	_	_	42.3	ps	
R <sub>ref</sub>	_	_	2000 ± 1%	_	_	2000 ± 1%	_	_	2000 ± 1%	_	Ω	
Transceiver Clock												
cal_blk_clk clock frequency	_	10	_	125	10	_	125	10	_	125	MHz	
fixedclk <b>clock</b> frequency	PCIe Receiver Detect	_	125	_	_	125	_	_	125	—	MHz	
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 <i>(2)</i>		50	2.5/ 37.5 <i>(2)</i>		50	2.5/ 37.5 <i>(2)</i>		50	MHz	
Delta time between reconfig_clk	_	_	_	2	_		2	_	_	2	ms	
Transceiver block minimum power-down pulse width	_	_	1		_	1	_	_	1	_	μs	