Intel - EP4CE75F23C8L Datasheet





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Details

Product Status	Active
Number of LABs/CLBs	4713
Number of Logic Elements/Cells	75408
Total RAM Bits	2810880
Number of I/O	292
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce75f23c8l

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Figure 3–7 shows a timing waveform for read and write operations in single-port mode with unregistered outputs. Registering the outputs of the RAM simply delays the q output by one clock cycle.



Figure 3–7. Cyclone IV Devices Single-Port Mode Timing Waveform

Simple Dual-Port Mode

Simple dual-port mode supports simultaneous read and write operations to different locations. Figure 3–8 shows the simple dual-port memory configuration.

Figure 3–8. Cyclone IV Devices Simple Dual-Port Memory (1)



Note to Figure 3-8:

(1) Simple dual-port RAM supports input or output clock mode in addition to the read or write clock mode shown.

Cyclone IV devices M9K memory blocks support mixed-width configurations, allowing different read and write port widths. Table 3–3 lists mixed-width configurations.

 Table 3–3.
 Cyclone IV Devices M9K Block Mixed-Width Configurations (Simple Dual-Port Mode)
 (Part 1 of 2)

Bood Bort					Write Port				
neau ruit	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	256 × 32	1024 × 9	512 × 18	256 × 36
8192 × 1	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	—	—	_
4096 × 2	\checkmark	\checkmark	~	\checkmark	\checkmark	\checkmark	—	—	—
2048 × 4	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	—	—	—
1024 × 8	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	—	—	—

20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. Choose the secondary clock frequency so the VCO operates in the recommended frequency range. Also, set the M, N, and C counters accordingly to keep the VCO operating frequency in the recommended range.

Figure 5–18 shows a waveform example of the switchover feature when using automatic loss of clock detection. Here, the inclk0 signal remains low. After the inclk0 signal remains low for approximately two clock cycles, the clock-sense circuitry drives the clkbad0 signal high. Also, because the reference clock signal is not toggling, the switchover state machine controls the multiplexer through the clksw signal to switch to inclk1.





Note to Figure 5–18:

(1) Switchover is enabled on the falling edge of inclk1 or inclk1, depending on which clock is available. In this figure, switchover is enabled on the falling edge of inclk1.

Manual Override

If you are using the automatic switchover, you must switch input clocks with the manual override feature with the clkswitch input.

Figure 5–19 shows an example of a waveform illustrating the switchover feature when controlled by clkswitch. In this case, both clock sources are functional and inclk0 is selected as the reference clock. A low-to-high transition of the clkswitch signal starts the switchover sequence. The clkswitch signal must be high for at least three clock cycles (at least three of the longer clock period if inclk0 and inclk1 have different frequencies). On the falling edge of inclk0, the reference clock of the counter, muxout, is gated off to prevent any clock glitching. On the falling edge of inclk1, the reference clock multiplexer switches from inclk0 to inclk1 as the PLL reference, and the activeclock signal changes to indicate which clock is currently feeding the PLL.

LFC[1]	LFC[0]	Setting (Decimal)
0	0	0
0	1	1
1	1	3

lable 5–10. Loop Filter Control of High Frequency Capac

Bypassing a PLL Counter

Bypassing a PLL counter results in a divide (N, C0 to C4 counters) factor of one.

Table 5–11 lists the settings for bypassing the counters in PLLs of Cyclone IV devices.

Table 5–11. PLL Counter Settings

PLL Scan Chain Bits [08] Settings							Description		
			LS	SB				MSB	Description
Х	Х	Х	Х	Х	Х	Х	Х	1 (1)	PLL counter bypassed
Х	Х	Х	Х	Х	Х	Х	Х	0 (1)	PLL counter not bypassed

Note to Table 5–11:

(1) Bypass bit.

To bypass any of the PLL counters, set the bypass bit to 1. The values on the other bits are then ignored.

Dynamic Phase Shifting

The dynamic phase shifting feature allows the output phase of individual PLL outputs to be dynamically adjusted relative to each other and the reference clock without sending serial data through the scan chain of the corresponding PLL. This feature simplifies the interface and allows you to quickly adjust t_{CO} delays by changing output clock phase shift in real time. This is achieved by incrementing or decrementing the VCO phase-tap selection to a given C counter or to the M counter. The phase is shifted by 1/8 the VCO frequency at a time. The output clocks are active during this phase reconfiguration process.

Table 5–12 lists the control signals that are used for dynamic phase shifting.

Table 5–12. Dynamic Phase Shifting Control Signals (Part 1 of 2)

Signal Name	Description	Source	Destination
phasecounterselect[20]	Counter Select. Three bits decoded to select either the M or one of the C counters for phase adjustment. One address map to select all C counters. This signal is registered in the PLL on the rising edge of scanclk.	Logic array or I/O pins	PLL reconfiguration circuit
phaseupdown	Selects dynamic phase shift direction; 1= UP, 0 = DOWN. Signal is registered in the PLL on the rising edge of scanclk.	Logic array or I/O pins	PLL reconfiguration circuit
phasestep	Logic high enables dynamic phase shifting.	Logic array or I/O pins	PLL reconfiguration circuit

Table 7–2 lists the number of DQS or DQ groups supported on each side of the Cyclone IV E device.

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
		Left	0	0	0	0	—	—
	144 pip EOED	Right	0	0	0	0	—	—
	144-pill EQFP	Bottom (1), (3)	1	0	0	0	—	—
		Top (1), (4)	1	0	0	0	—	—
		Left (1)	1	1	0	0	—	—
EP4CE6	256-pip LIBGA	Right ⁽²⁾	1	1	0	0	—	—
EP4CE10	250-piil 080A	Bottom	2	2	1	1	—	—
		Тор	2	2	1	1	—	—
		Left (1)	1	1	0	0	—	—
	256 pip EPCA	Right ⁽²⁾	1	1	0	0	—	—
	250-piii FBGA	Bottom	2	2	1	1	—	—
		Тор	2	2	1	1	—	—
		Left	0	0	0	0	—	—
	144 pip EOED	Right	0	0	0	0	—	—
		Bottom (1), (3)	1	0	0	0	—	—
		Top (1), (4)	1	0	0	0	—	—
	164-pin MBGA	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Bottom (1), (3)	1	0	0	0	—	—
		Top (1), (4)	1	0	0	0	—	—
	256-pin MBGA	Left	1	1	0	0	—	—
		Right	1	1	0	0	—	—
		Bottom (1), (3)	2	2	1	1	—	—
		Top (1), (4)	2	2	1	1	—	—
EF40E15		Left (1)	1	1	0	0	—	—
	256 pip LIPCA	Right (2)	1	1	0	0	—	—
	250-piil 080A	Bottom	2	2	1	1	—	—
		Тор	2	2	1	1	—	—
		Left (1)	1	1	0	0	—	—
	256 pip EPCA	Right ⁽²⁾	1	1	0	0	—	—
	250-piii FBGA	Bottom	2	2	1	1	—	—
		Тор	2	2	1	1	—	—
		Left	4	4	2	2	1	1
	484-nin EPCA	Right	4	4	2	2	1	1
	чоч-ріп град	Bottom	4	4	2	2	1	1
		Тор	4	4	2	2	1	1

The nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors, as shown in Figure 8–8 on page 8–26 and Figure 8–9 on page 8–27. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they receive their configuration data. When all target devices in the chain receive their configuration data and release CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

Guidelines for Connecting Parallel Flash to Cyclone IV E Devices for an AP Interface

For single- and multi-device AP configuration, the board trace length and loading between the supported parallel flash and Cyclone IV E devices must follow the recommendations listed in Table 8–11. These recommendations also apply to an AP configuration with multiple bus masters.

Cyclone IV E AP Pins	Maximum Board Trace Length from Cyclone IV E Device to Flash Device (inches)	Maximum Board Load (pF)
DCLK	6	15
DATA[150]	6	30
PADD[230]	6	30
nRESET	6	30
Flash_nCE	6	30
nOE	6	30
nAVD	6	30
nWE	6	30
I/O (1)	6	30

 Table 8–11. Maximum Trace Length and Loading for AP Configuration

Note to Table 8-11:

(1) The AP configuration ignores the WAIT signal from the flash during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Micron P30 or P33 flash.

Configuring With Multiple Bus Masters

Similar to the AS configuration scheme, the AP configuration scheme supports multiple bus masters for the parallel flash. For another master to take control of the AP configuration bus, the master must assert nCONFIG low for at least 500 ns to reset the master Cyclone IV E device and override the weak 10-k Ω pull-down resistor on the nCE pin. This resets the master Cyclone IV E device then takes control of the AP configuration bus. The other master device then takes control of the AP configuration bus, then releases the nCE pin, and finally pulses nCONFIG low to restart the configuration.

In the AP configuration scheme, multiple masters share the parallel flash. Similar to the AS configuration scheme, the bus control is negotiated by the nCE pin.

FPP Configuration Timing

Figure 8–22 shows the timing waveform for the FPP configuration when using an external host.





Notes to Figure 8-22:

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and $CONF_DONE$ are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power up, the Cyclone IV device holds ${\tt nSTATUS}$ low during POR delay.
- (3) After power up, before and during configuration, $CONF_DONE$ is low.
- (4) Do not leave DCLK floating after configuration. It must be driven high or low, whichever is more convenient.
- (5) DATA [7..0] is available as a user I/O pin after configuration; the state of the pin depends on the dual-purpose pin settings.

Table 8–13 lists the FPP configuration timing parameters for Cyclone IV devices.

Table 8–13. FPP Timing Parameters for Cyclone IV Devices (Part 1 of 2)

0hal	Deventer	Minii	num	Maxir	Unit	
Symbol	Parameter	Cyclone IV ⁽¹⁾	Cyclone IV E ⁽²⁾	Cyclone IV ⁽¹⁾ Cyclone IV E		
t _{cf2cd}	nCONFIG low to CONF_DONE low	_	_	50	ns	
t _{cf2st0}	nCONFIG low to nSTATUS low	_	_	50	ns	
t _{CFG}	nCONFIG low pulse width	50	0		ns	
t _{status}	nSTATUS low pulse width	4	5	230	(3)	μs
t _{cf2ST1}	nCONFIG high to nSTATUS high	_	_	230 (4)		μs
t _{cf2CK}	nCONFIG high to first rising edge on DCLK	230 ⁽³⁾		.30 (3)		μs

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system with JTAG BST circuitry. Figure 8–25 and Figure 8–26 show multi-device JTAG configuration.

For devices using 2.5-, 3.0-, and 3.3-V V_{CCIO} supply, you must refer to Figure 8–25. All I/O inputs must maintain a maximum AC voltage of 4.1 V because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using 2.5-, 3.0-, and 3.3- V V_{CCIO} supply. You must power up the V_{CC} of the download cable with a 2.5-V V_{CCA} supply. For device using V_{CCIO} of 1.2, 1.5 V, and 1.8 V, refer to Figure 8–26. You can power up the V_{CC} of the download cable with the supply from V_{CCIO}.

Figure 8–25. JTAG Configuration of Multiple Devices Using a Download Cable (2.5, 3.0, and 3.3-V V_{CCIO} Powering the JTAG Pins)



Notes to Figure 8-25:

- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Connect the nCONFIG and MSEL pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA [0] to either high or low, whichever is convenient on your board.
- (3) Pin 6 of the header is a V₁₀ reference voltage for the MasterBlaster output driver. V₁₀ must match the V_{CCA} of the device. For this value, refer to the MasterBlaster Serial/USB Communications Cable User Guide. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) You must connect the nCE pin to GND or driven low for successful JTAG configuration.
- (5) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.
- (6) Resistor value can vary from 1 k Ω to 10 k Ω .





Notes to Figure 8-28:

- (1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.
- (2) Power up the V_{CC} of the EthernetBlaster, ByteBlaster II, or USB-Blaster cable with the 3.3-V supply.
- (3) Pin 6 of the header is a V_{I0} reference voltage for the MasterBlaster output driver. The V_{I0} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. When using the ByteBlasterMV download cable, this pin is a no connect. When using the USB-Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
- (4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL for AS configuration schemes, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.
- (5) Power up the V_{CC} of the EthernetBlaster, ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5-V V_{CCA} supply. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.
- (6) You must place the diodes and capacitors as close as possible to the Cyclone IV device. Altera recommends using the Schottky diode, which has a relatively lower forward diode voltage (VF) than the switching and Zener diodes, for effective voltage clamping.
- (7) These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as DATA[1] pin in AP and FPP modes.
- (8) Resistor value can vary from 1 k Ω to 10 k Ω .
- (9) Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK.

Reconfiguration

After the configuration data is successfully written into the serial configuration device, the Cyclone IV device does not automatically start reconfiguration. The intelligent host issues the PULSE_NCONFIG JTAG instruction to initialize the reconfiguration process. During reconfiguration, the master device is reset and the SFL design no longer exists in the Cyclone IV device and the serial configuration device configures all the devices in the chain with the user design.



• For more information about the SFL, refer to *AN* 370: Using the Serial FlashLoader with *Quartus II Software*.

JTAG Instructions



For more information about the JTAG binary instruction code, refer to the *JTAG Boundary-Scan Testing for Cyclone IV Devices* chapter.

I/O Reconfiguration

Use the CONFIG_IO instruction to reconfigure the I/O configuration shift register (IOCSR) chain. This instruction allows you to perform board-level testing prior to configuring the Cyclone IV device or waiting for a configuration device to complete configuration. After the configuration is interrupted and JTAG testing is complete, you must reconfigure the part through the PULSE_NCONFIG JTAG instruction or by pulsing the nCONFIG pin low.

You can issue the CONFIG_IO instruction any time during user mode.

You must meet the following timing restrictions when using the CONFIG_IO instruction:

- The CONFIG_IO instruction cannot be issued when the nCONFIG pin is low
- You must observe a 230 μs minimum wait time after any of the following conditions:
 - nCONFIG pin goes high
 - Issuing the PULSE_NCONFIG instruction
 - Issuing the ACTIVE_ENGAGE instruction, before issuing the CONFIG_IO instruction
- You must wait 230 µs after power up, with the nCONFIG pin high before issuing the CONFIG_IO instruction (or wait for the nSTATUS pin to go high)

Device	Boundary-Scan Register Length
EP4CGX75	1006
EP4CGX110	1495
EP4CGX150	1495

Table 10–1. B	Boundarv-Scan Re	aister Lenath for (Cyclone IV Devices	(Part 2 of 2)
		giotoi mongtii ioi t	· · · · · · · · · · · · · · · · · · ·	(

Note to Table 10-1:

(1) For the F484 package of the EP4CGX30 device, the boundary-scan register length is 1006.

Table 10–2 lists the IDCODE information for Cyclone IV devices.

Table 10-2.	IDCODE Information for 32-Bit (Cyclone IV Devices
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	IDCODE (32 Bits) ⁽¹⁾					
Device	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) ⁽²⁾		
EP4CE6	0000	0010 0000 1111 0001	000 0110 1110	1		
EP4CE10	0000	0010 0000 1111 0001	000 0110 1110	1		
EP4CE15	0000	0010 0000 1111 0010	000 0110 1110	1		
EP4CE22	0000	0010 0000 1111 0011	000 0110 1110	1		
EP4CE30	0000	0010 0000 1111 0100	000 0110 1110	1		
EP4CE40	0000	0010 0000 1111 0100	000 0110 1110	1		
EP4CE55	0000	0010 0000 1111 0101	000 0110 1110	1		
EP4CE75	0000	0010 0000 1111 0110	000 0110 1110	1		
EP4CE115	0000	0010 0000 1111 0111	000 0110 1110	1		
EP4CGX15	0000	0010 1000 0000 0001	000 0110 1110	1		
EP4CGX22	0000	0010 1000 0001 0010	000 0110 1110	1		
EP4CGX30 (3)	0000	0010 1000 0000 0010	000 0110 1110	1		
EP4CGX30 (4)	0000	0010 1000 0010 0011	000 0110 1110	1		
EP4CGX50	0000	0010 1000 0001 0011	000 0110 1110	1		
EP4CGX75	0000	0010 1000 0000 0011	000 0110 1110	1		
EP4CGX110	0000	0010 1000 0001 0100	000 0110 1110	1		
EP4CGX150	0000	0010 1000 0000 0100	000 0110 1110	1		

Notes to Table 10-2:

(1) The MSB is on the left.

(2) The IDCODE LSB is always 1.

(3) The IDCODE is applicable for all packages except for the F484 package.

(4) The IDCODE is applicable for the F484 package only.

IEEE Std.1149.6 mandates the addition of two new instructions: EXTEST_PULSE and EXTEST_TRAIN. These two instructions enable edge-detecting behavior on the signal path containing the AC pins.

Document Revision History

Table 10–3 lists the revision history for this chapter.

Table 10–3. Document Revision History

Date	Version	Changes
December 2013	1.3	 Updated the "EXTEST_PULSE" section.
November 2011	1.2	 Updated the "BST Operation Control" section.
		■ Updated Table 10–2.
February 2010	1.1	 Added Cyclone IV E devices in Table 10–1 and Table 10–2 for the Quartus II software version 9.1 SP1 release.
		■ Updated Figure 10–1 and Figure 10–2.
		 Minor text edits.
November 2009	1.0	Initial release.



Figure 1–37. Clock Distribution in Bonded (×2 and ×4) Channel Configuration for Transceivers in F484 and Larger Packages

Notes to Figure 1-37:

- (1) High-speed clock.
- (2) Low-speed clock.
- (3) Bonded common low-speed clock path.
- (4) These PLLs have restricted clock driving capability and may not reach all connected channels. For details, refer to Table 1–10.

The channel datapath clocking is similar between bonded channels in ×2 and ×4 configurations.

Figure 1–38 shows the datapath clocking in Transmitter Only operation for ×2 and ×4 bonded configurations. In these configurations, each bonded channel selects the high-speed clock from one the supported PLLs. The high-speed clock in each bonded channel feeds the respective serializer for parallel to serial operation. The common bonded low-speed clock feeds to each bonded channel that is used for the following blocks in each transmitter PCS channel:

- 8B/10B encoder
- read clock of byte serializer
- read clock of TX phase compensation FIFO

Reverse Parallel Loopback

The reverse parallel loopback option is only available for PIPE mode. In this mode, the received serial data passes through the receiver CDR, deserializer, word aligner, and rate match FIFO before looping back to the transmitter serializer and transmitted out through the TX buffer, as shown in Figure 1–70. The received data is also available to the FPGA fabric. This loopback mode is compliant with version 2.00 of the *PHY Interface for the PCI Express Architecture* specification.

To enable the reverse parallel loopback mode, assert the tx_detectrxloopback port in P0 power state.

Figure 1–70. PIPE Reverse Parallel Loopback Path (1)



Note to Figure 1–70: (1) Grayed-Out Blocks are Not Active in this mode.

Serial Loopback

The serial loopback option is available for all functional modes except PIPE mode. In this mode, the data from the FPGA fabric passes through the transmitter channel and looped back to the receiver channel, bypassing the receiver buffer, as shown in Figure 1–71. The received data is available to the FPGA logic for verification. The receiver input buffer is not active in this mode. With this option, you can check the operation of all enabled PCS and PMA functional blocks in the transmitter and receiver channels.

The transmitter channel sends the data to both the serial output port and the receiver channel. The differential output voltage on the serial ports is based on the selected V_{OD} settings. The data is looped back to the receiver CDR and is retimed through different clock domains. You must provide an alignment pattern for the word aligner to enable the receiver channel to retrieve the byte boundary.

PRBS

Figure 1–74 shows the datapath for the PRBS, high and low frequency pattern test modes. The pattern generator is located in TX PCS before the serializer, and PRBS pattern verifier located in RX PCS after the word aligner.

Figure 1–74. PRBS Pattern Test Mode Datapath



Note to Figure 1-74:

(1) Serial loopback path is optional and can be enabled for the PRBS verifier to check the PRBS pattern

Table 1–25 lists the supported PRBS, high and low frequency patterns, and corresponding channel settings. The PRBS pattern repeats after completing an iteration. The number of bits a PRBS X pattern sends before repeating the pattern is $2^{(X-1)}$ bits.

Table 1–25. PRBS, High and Low Frequency Patterns, and Channel Settings (Part 1 of 2)

	Polynomial	8-bit Channel Width			10-bit Channel Width				
Patterns		Channel Width of 8 bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages	Channel Width of 10-bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages
PRBS 7	X ⁷ + X ⁶ + 1	Y	16'h3040	2.0	2.5	Ν	—	_	_
PRBS 8	X ⁸ + X ⁷ + 1	Y	16'hFF5A	2.0	2.5	Ν	—	—	—
PRBS 10	$X^{10} + X^7 + 1$	Ν	—	—	—	Y	10'h3FF	2.5	3.125
PRBS 23	$X^{23} + X^{18} + 1$	Y	16'hFFFF	2.0	2.5	Ν	—		_
High frequency ⁽²⁾	1010101010	Y	_	2.0	2.5	Y	_	2.5	3.125