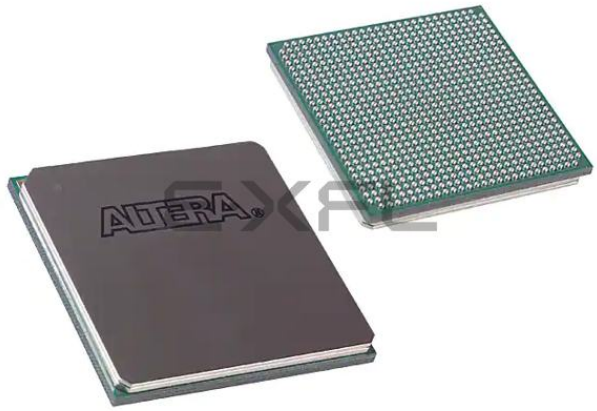

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4713
Number of Logic Elements/Cells	75408
Total RAM Bits	2810880
Number of I/O	426
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce75f29c8l

Table 5 3. GCLK Network Connections for Cyclone IV E Devices (1) (Part 3 of 3)

GCLK Network Clock Sources	GCLK Networks																			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
DPCLK2 (4)																				
CDPCLK1 or CDPCLK2 (2), (5)				v	v															
DPCLK5 (4)						v														
DPCLK7 (2)																				
DPCLK4 (4)							v													
DPCLK6 (2)																				
DPCLK6 (4)								v												
CDPCLK5 or CDPCLK6 (2), (5)																				
DPCLK3 (4)									v	v										
CDPCLK4 or CDPCLK3 (2), (5)																				
DPCLK8											v									
DPCLK11												v								
DPCLK9													v							
DPCLK10														v	v					
DPCLK5															v					
DPCLK2																v				
DPCLK4																	v			
DPCLK3																		v	v	

Notes to Table 5 3:

(1) EP4CE6 and EP4CE10 devices only have GCLK networks 0 to 9.
(2) These pins apply to all Cyclone IV E devices except EP4CE6 and EP4CE10 devices.
(3) EP4CE6 and EP4CE10 devices only have PLL_1 and PLL_2.
(4) This pin applies only to EP4CE6 and EP4CE10 devices.
(5) Only one of the two CDPCLK pins can feed the clock control block. You can use the other pin as a regular I/O pin.

Each Cyclone IV I/O bank has a VREFbus to accommodate voltage-referenced I/O standards. Each VREF pin is the reference source for its V_{REF} group. If you use a V_{REF} group for voltage-referenced I/O standards, connect the VREF pin for that group to the appropriate voltage level. If you do not use all the V_{REF} groups in the I/O bank for voltage-referenced I/O standards, you can use the VREF pin in the unused voltage-referenced groups as regular I/O pins. For example, if you have SSTL-2 Class I input pins in I/O bank 1 and they are all placed in the VREFB1N[0] group, VREFB1N[0] must be powered with 1.25 V, and the remaining VREFB1N[1..3] pins (if available) are used as I/O pins. If multiple V_{REF} groups are used in the same I/O bank, the VREF pins must all be powered by the same voltage level because the VREF pins are shorted together within the same I/O bank.

When VREF pins are used as regular I/Os, they have higher pin capacitance than regular user I/O pins. This has an impact on the timing if the pins are used as inputs and outputs.

For more information about VREF pin capacitance, refer to the pin capacitance section in the *Cyclone IV Device Datasheet* chapter.

For information about how to identify V_{REF} groups, refer to the Cyclone IV Device Pin-Out files or the Quartus II Pin Planner tool.

Table 6–4 and Table 6–5 summarize the number of VREF pins in each I/O bank for the Cyclone IV device family.

Table 6–4. Number of VREF Pins Per I/O Bank for Cyclone IV E Devices (Part 1 of 2)

Device	EP4CE6			EP4CE10			EP4CE15						EP4CE22			EP4CE30			EP4CE40				EP4CE55			EP4CE75			EP4CE115	
I/O Bank (1)	144-EQPF	256-UBGA	256-FBGA	144-EQPF	256-UBGA	256-FBGA	144-EQPF	164-MBGA	256-MBGA	256-UBGA	256-FBGA	484-FBGA	144-EQPF	256-UBGA	256-FBGA	324-FBGA	484-FBGA	780-FBGA	324-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-FBGA	780-FBGA
1	1	1	1	1	1	1	2	2	2	2	2	2	1	1	1	4	4	4	4	4	4	4	2	2	2	3	3	3	3	3
2	1	1	1	1	1	1	2	2	2	2	2	2	1	1	1	4	4	4	4	4	4	4	2	2	2	3	3	3	3	3
3	1	1	1	1	1	1	2	2	2	2	2	2	1	1	1	4	4	4	4	4	4	4	2	2	2	3	3	3	3	3
4	1	1	1	1	1	1	2	2	2	2	2	2	1	1	1	4	4	4	4	4	4	4	2	2	2	3	3	3	3	3
5	1	1	1	1	1	1	2	2	2	2	2	2	1	1	1	4	4	4	4	4	4	4	2	2	2	3	3	3	3	3
6	1	1	1	1	1	1	2	2	2	2	2	2	1	1	1	4	4	4	4	4	4	4	2	2	2	3	3	3	3	3
7	1	1	1	1	1	1	2	2	2	2	2	2	1	1	1	4	4	4	4	4	4	4	2	2	2	3	3	3	3	3

Use the ACTIVE_DISENGAGE instruction with the CONFIG_IO instruction to interrupt configuration. Table 8–16 lists the sequence of instructions to use for various CONFIG_IO usage scenarios.

Table 8–16. JTAG CONFIG_IO (without JTAG_PROGRAM) Instruction Flows (1)

JTAG Instruction	Configuration Scheme and Current State of the Cyclone IV Device											
	Prior to User Mode (Interrupting Configuration)				User Mode				Power Up			
	PS	FPP	AS	AP	PS	FPP	AS	AP	PS	FPP	AS	AP
ACTIVE_DISENGAGE	O	O	O	O	O	O	O	O	—	—	—	—
CONFIG_IO	R	R	R	R	R	R	R	R	NA	NA	NA	NA
JTAG Boundary Scan Instructions (no JTAG_PROGRAM)	O	O	O	O	O	O	O	O	—	—	—	—
ACTIVE_ENGAGE	A	A	R (2)	R (2)	A	A	R (2)	R (2)	—	—	—	—
PULSE_NCONFIG			A (3)	A (3)			O	O	—	—	—	—
Pulse nCONFIG pin			A (3)	A (3)			O	O	—	—	—	—
JTAG TAP Reset	R	R	R	R	R	R	R	R	—	—	—	—

Notes to Table 8–16:

(1) You must execute "R" indicates that the instruction before the next instruction, "O" indicates the optional instruction, "A" indicates that the instruction must be executed, and "NA" indicates that the instruction is not allowed in this mode.

(2) Required if you use ACTIVE_DISENGAGE.

(3) Neither of the instruction is required if you use ACTIVE_ENGAGE.

The CONFIG_IO instruction does not hold nSTATUS low until reconfiguration. You must disengage the AS or AP configuration controller by issuing the ACTIVE_DISENGAGE and ACTIVE_ENGAGE instructions when active configuration is interrupted. You must issue the ACTIVE_DISENGAGE instruction alone or prior to the CONFIG_IO instruction if the JTAG_PROGRAM instruction is to be issued later (Table 8–17). This puts the active configuration controllers into the idle state. The active configuration controller is re-engaged after user mode is reached through JTAG programming (Table 8–17).

☞ While executing the CONFIG_IO instruction, all user I/Os are tri-stated.

If reconfiguration after interruption is performed using configuration modes (rather than using JTAG_PROGRAM), it is not necessary to issue the ACTIVE_DISENGAGE instruction prior to CONFIG_IO. You can start reconfiguration by either pulling nCONFIG low for at least 500 ns or issuing the PULSE_NCONFIG instruction. If the ACTIVE_DISENGAGE instruction was issued and the JTAG_PROGRAM instruction fails to enter user mode, you must issue the ACTIVE_ENGAGE instruction to reactivate the active configuration controller. Issuing the ACTIVE_ENGAGE instruction also triggers reconfiguration in configuration modes; therefore, it is not necessary to pull nCONFIG low or issue the PULSE_NCONFIG instruction.

Figure 8–34 shows the control register bit positions. Table 8–23 defines the control register bit contents. The numbers in Figure 8–34 show the bit position of a setting in a register. For example, bit number 35 is the enable bit for the watchdog timer.

Figure 8–34. Remote System Upgrade Control Register

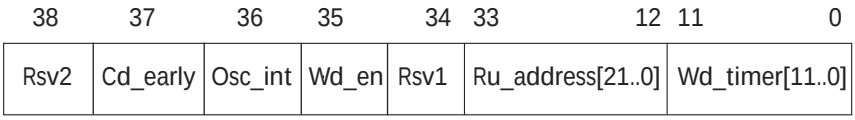


Table 8–23. Remote System Upgrade Control Register Contents

Control Register Bit	Value	Definition
Wd_timer[11..0]	12'b000000000000	User watchdog time-out value (most significant 12 bits of 29-bit count value: {Wd_timer[11..0],17'b1000})
Ru_address[21..0]	22'b0000000000000000000000	Configuration address (most significant 22 bits of 24-bit boot address value: boot_address[23:0] = {Ru_address[21..0],2'b0})
Rsv1	1'b0	Reserved bit
Wd_en	1'b1	User watchdog timer enable bit
Osc_int (1)	1'b1	Internal oscillator as startup state machine clock enable bit
Cd_early (1)	1'b1	Early CONF_DONE check
Rsv2	1'b1	Reserved bit

Note to Table 8–23:

(1) Option bit for the application configuration.

When enabled, the early CONF_DONE check (Cd_early) option bit ensures that there is a valid configuration at the boot address specified by the factory configuration and that it is of the proper size. If an invalid configuration is detected or the CONF_DONE pin is asserted too early, the device resets and then reconfigures the factory configuration image. The internal oscillator (as the startup state machine clock [Osc_int] option bit) ensures a functional startup clock to eliminate the hanging of startup. When all option bits are turned on, they provide complete coverage for the programming and startup portions of the application configuration. Altera recommends turning on both the Cd_early and Osc_int option bits.

☞ The Cd_early and Osc_int option bits for the application configuration must be turned on by the factory configuration.

Remote System Upgrade Status Register

The remote system upgrade status register specifies the reconfiguration trigger condition. The various trigger and error conditions include:

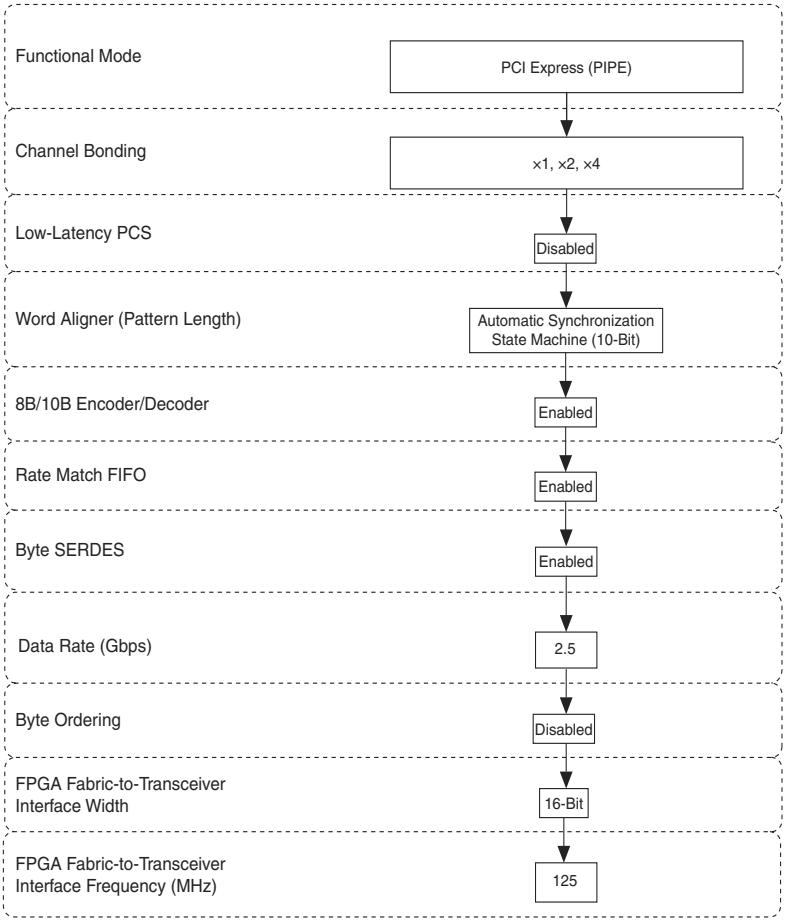
- Cyclical redundancy check (CRC) error during application configuration
- nSTATUS assertion by an external device due to an error
- Cyclone IV device logic array triggers a reconfiguration cycle, possibly after downloading a new application configuration image

Configuring the hard IP module requires using the PCI Express Compiler. When configuring the transceiver for PCIe implementation with hard IP module, the byte serializer and deserializer are not enabled, providing an 8-bit transceiver-PIPE-hard IP data interface width running at 250 MHz clock frequency.

For more information about PCIe implementation with hard IP module, refer to the *PCI Express Compiler User Guide*.

Figure 1–49 shows the transceiver configuration in PIPE mode.

Figure 1–49. Transceiver Configuration in PIPE Mode



When configuring the transceiver into PIPE mode using ALTGX megafunction for PCIe implementation, the PHY-MAC, data link and transaction layers must be implemented in user logics. The PCIe hard IP block is bypassed in this configuration.

Table 1–21. XGMII Character to PCS Code Groups Mapping (Part 2 of 2)

XGMII TXC (1)	XGMII TXD (2), (3)	PCS Code Group	Description
1	Any other value	K30.7	Invalid XGMII character

Notes to Table 1–21:

(1) Equivalent to `tx_ctrlenable` port.
(2) Equivalent to 8-bit input data to 8B/10B encoder.
(3) The values in XGMII TXD column are in hexadecimal.

8B/10B decoder in the receiver datapath maps received PCS code groups into specific 8-bit XGMII codes as listed in Table 1–22.

Table 1–22. PCS Code Groups to XGMII Character Mapping

XGMII RXC (1)	XGMII RXD (2), (3)	PCS Code Group	Description
0	00 through FF	Dxx,y	Normal data transmission
1	07	K28.0, K28.3, or K28.5	Idle in ||I||
1	07	K28.5	Idle in ||T||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	FE	Invalid code group	Received code group

Notes to Table 1–22:

(1) Equivalent to `rx_ctrlenable` port.
(2) Equivalent to 8-bit input data to 8B/10B encoder.
(3) The values in XGMII RXD column are in hexadecimal.

Channel Deskewing

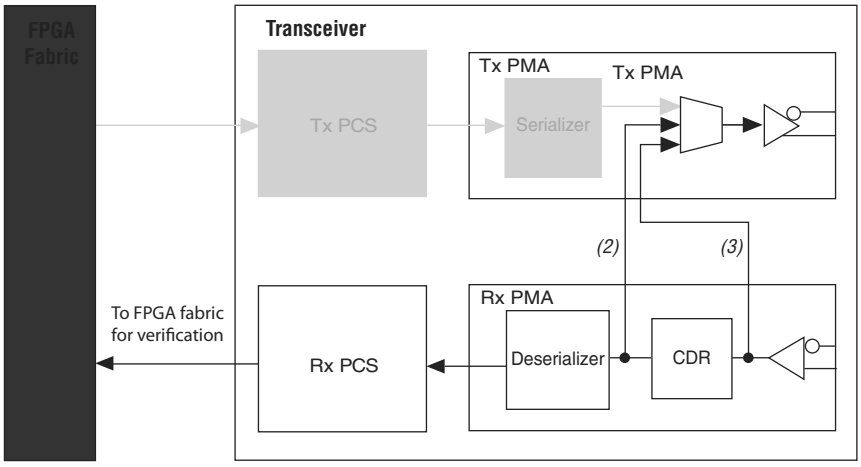
The deskew FIFO in each of the four lanes expects to receive /A/ code group simultaneously on all four channels during the inter-packet gap, as required by XAUI protocol. The skew introduced in the physical medium and the receiver channels might cause the /A/ code group to be received misaligned with respect to each other.

The deskew FIFO works to align the /A/ code group across the four channels, which operation is compliant to the PCS deskew state machine diagram specified in clause 48 of the IEEE P802.3ae specification. The deskew operation begins after link synchronization is achieved on all four channels as indicated by the word aligner in each channel. The following are the deskew FIFO operations:

- Until the first /A/ code group is received, the deskew FIFO read and write pointers in each channel are not incremented.
- After the first /A/ code group is received, the write pointer starts incrementing for each word received but the read pointer is frozen.
- When all the four channels received the /A/ code group within 10 recovered clock cycles of each other, the read pointer of all four deskew FIFOs is released simultaneously, aligning the /A/ code group of all four channels in a column.

Figure 1–72 shows the two paths in reverse serial loopback mode.

Figure 1–72. Reverse Serial Loopback (1)



Notes to Figure 1–72:

(1) Grayed-Out Blocks are Not Active in this mode.
(2) Post-CDR reverse serial loopback path.
(3) Pre-CDR reverse serial loopback path.

Self Test Modes

Each transceiver channel in the Cyclone IV GX device contains modules for pattern generator and verifier. Using these built-in features, you can verify the functionality of the functional blocks in the transceiver channel without requiring user logic. The self test functionality is provided as an optional mechanism for debugging transceiver channels.

There are three types of supported pattern generators and verifiers:

- Built-in self test (BIST) incremental data generator and verifier—test the complete transmitter PCS and receiver PCS datapaths for bit errors with parallel loopback before the PMA blocks.
- Pseudo-random binary sequence (PRBS) generator and verifier—the PRBS generator and verifier interface with the serializer and deserializer in the PMA blocks. The advantage of using a PRBS data stream is that the randomness yields an environment that stresses the transmission medium. In the data stream, you can observe both random jitter and deterministic jitter using a time interval analyzer, bit error rate tester, or oscilloscope.
- High frequency and low frequency pattern generator—the high frequency patterns generate alternate ones and zeros and the low frequency patterns generate five ones and five zeroes. These patterns do not have a corresponding verifier.

The self-test features are only supported in Basic mode.

- In PCIe mode simulation, you must assert the `tx_forceelecidle` signal for at least one parallel clock cycle before transmitting normal data for correct simulation behavior.

Reference Information

For more information about some useful reference terms used in this chapter, refer to the links listed in Table 2–7.

Table 2–7. Reference Information

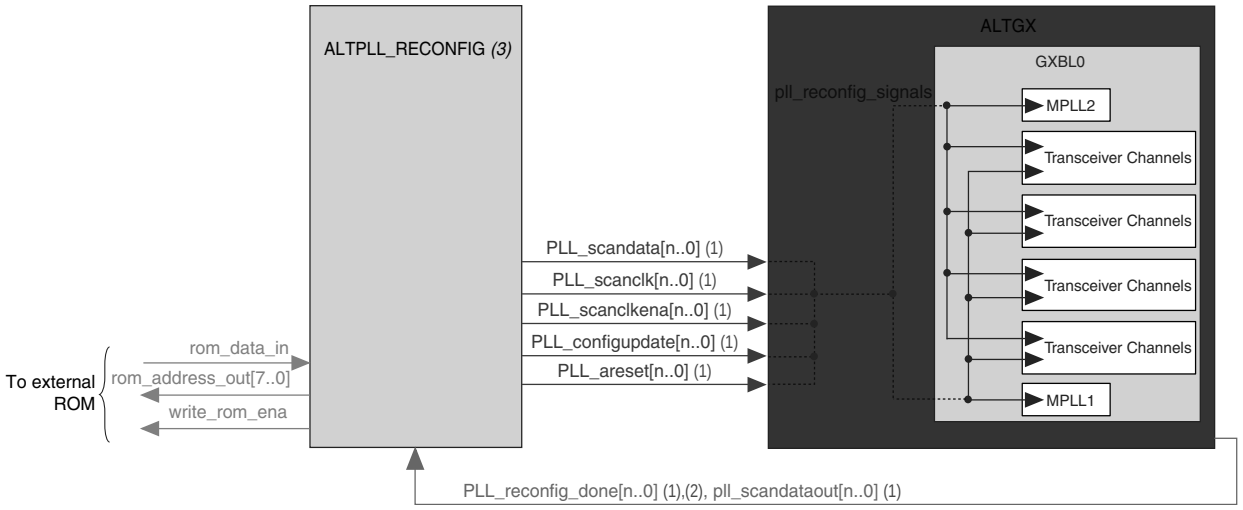
Terms Used in this Chapter	Useful Reference Points
Automatic Lock Mode	page 2–8
Bonded channel configuration	page 2–6
`busy`	page 2–3
Dynamic Reconfiguration Reset Sequences	page 2–19
`gxb_powerdown`	page 2–3
LTD	page 2–6
LTR	page 2–6
Manual Lock Mode	page 2–9
Non-Bonded channel configuration	page 2–10
PCIe	page 2–17
`pll_locked`	page 2–3
`pll_areset`	page 2–3
`rx_analogreset`	page 2–2
`rx_digitalreset`	page 2–2
`rx_freqlocked`	page 2–3
`tx_digitalreset`	page 2–2

The .mif files carries the reconfiguration information that will be used to reconfigure the multipurpose PLL or general purpose PLL dynamically. The .mif contents is generated automatically when you select the Enable PLL Reconfiguration option in the Reconfiguration Setting in ALTGX instances. The .mif files will be generated based on the data rate and input reference clock setting in the ALTGX MegaWizard. You must use the external ROM and feed its content to the ALTPLL_RECONFIG megafunction to reconfigure the multipurpose PLL setting.

For more information about instantiating the ALTPLL_Reconfig, refer to the *AN 609: Implementing Dynamic Reconfiguration in Cyclone IV GX Devices*.

Figure 3–16 shows the connection for PLL reconfiguration mode.

Figure 3–16. ALTGX and ALTPLL_RECONFIG Connection for PLL Reconfiguration Mode



Notes to Figure 3–16:

(1) <n> = (number of transceiver PLLs configured in the ALTGX MegaWizard) - 1.

(2) You must connect the `pll_reconfig_done` signal from the ALTGX to the `pll_scandone` port from ALTPLL_RECONFIG.

(3) You need two ALTPLL_RECONFIG controllers if you have two separate ALTGX instances with transceiver PLL instantiated in each ALTGX instance.

For more information about connecting the ALTPLL_RECONFIG and ALTGX instances, refer to the *AN 609: Implementing Dynamic Reconfiguration in Cyclone IV GX Devices*.

If you are reconfiguring the multipurpose PLL with a different M counter value, follow these steps:

1. During transceiver PLL reconfiguration, assert `tx_digitalreset`, `rx_digitalreset`, and `rx_analogreset` signals.
2. Perform PLL reconfiguration to update the multipurpose PLL with the PLL .mif files.
3. Perform channel reconfiguration and update the transceiver with the GXB reconfiguration .mif files. If you have multiple channel instantiations connected to the same multipurpose PLL, reconfigure each channel.
4. Deassert `tx_digitalreset` and `rx_analogreset` signals.
5. After the `rx_freqlocked` signal goes high, wait for at least 4 µs, and then deassert the `rx_digitalreset` signal.

Error Indication During Dynamic Reconfiguration

The ALTGX_RECONFIG MegaWizard Plug-In Manager provides an error status signal when you select the Enable illegal mode checking option or the Enable self recovery option in the Error checks/data rate switch screen. The conditions under which the error signal is asserted are:

- Enable illegal mode checking option—when you select this option, the dynamic reconfiguration controller checks whether an attempted operation falls under one of the conditions listed below. The dynamic reconfiguration controller detects these conditions within two `reconfig_clk` cycles, deasserts the `busy` signal, and asserts the error signal for two `reconfig_clk` cycles.
  - PMA controls, read operation—none of the output ports (`rx_eqctrl_out`, `rx_eqdcgain_out`, `tx_vodctrl_out`, and `tx_preemp_out`) are selected in the ALTGX_RECONFIG instance and the `read` signal is asserted.
  - PMA controls, write operation—none of the input ports (`rx_eqctrl`, `rx_eqdcgain`, `tx_vodctrl`, and `tx_preemp`) are selected in the ALTGX_RECONFIG instance and the `write_all` signal is asserted.
- Channel reconfiguration and PMA reconfiguration mode select - read operation option:
  - The `reconfig_mode_sel` input port is set to 3'b001 (Channel reconfiguration mode)
  - The `read` signal is asserted
- Enable self recovery option—when you select this option, the ALTGX_RECONFIG MegaWizard Plug-In Manager provides the error output port. The dynamic reconfiguration controller quits an operation if it did not complete within the expected number of clock cycles. After recovering from the illegal operation, the dynamic reconfiguration controller deasserts the `busy` signal and asserts the error output port for two `reconfig_clk` cycles.

☞ The error signal is not asserted when an illegal value is written to any of the PMA controls.

1. Cyclone IV Device Datasheet

CYIV-53001-2.1

This chapter describes the electrical and switching characteristics for Cyclone IV devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

This chapter includes the following sections:

Operating Conditions

When Cyclone IV devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone IV devices, you must consider the operating requirements described in this chapter.

Cyclone IV devices are offered in commercial, industrial, extended industrial and, automotive grades. Cyclone IV E devices offer –6 (fastest), –7, –8, –8L, and –9L speed grades for commercial devices, –8L speed grades for industrial devices, and –7 speed grade for extended industrial and automotive devices. Cyclone IV GX devices offer –6 (fastest), –7, and –8 speed grades for commercial devices and –7 speed grade for industrial devices.

For more information about the supported speed grades for respective Cyclone IV devices, refer to the Cyclone IV FPGA Device Family Overview chapter.

Cyclone IV E devices are offered in core voltages of 1.0 and 1.2 V. Cyclone IV E devices with a core voltage of 1.0 V have an 'L' prefix attached to the speed grade.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with a "C" prefix, industrial with an "I" prefix, and automotive with an "A" prefix. Therefore, commercial devices are indicated as C6, C7, C8, C8L, or C9L per respective speed grade. Industrial devices are indicated as I7, I8, or I8L. Automotive devices are indicated as A7.