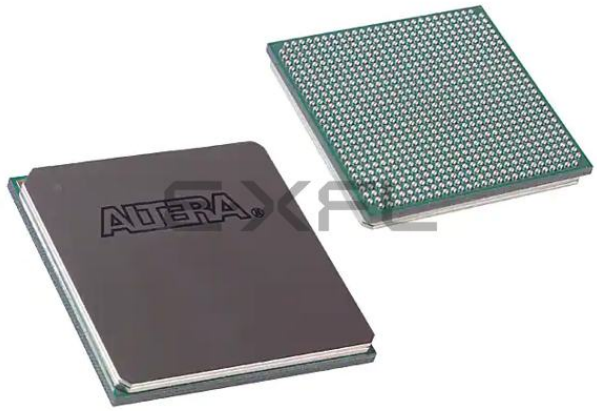

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

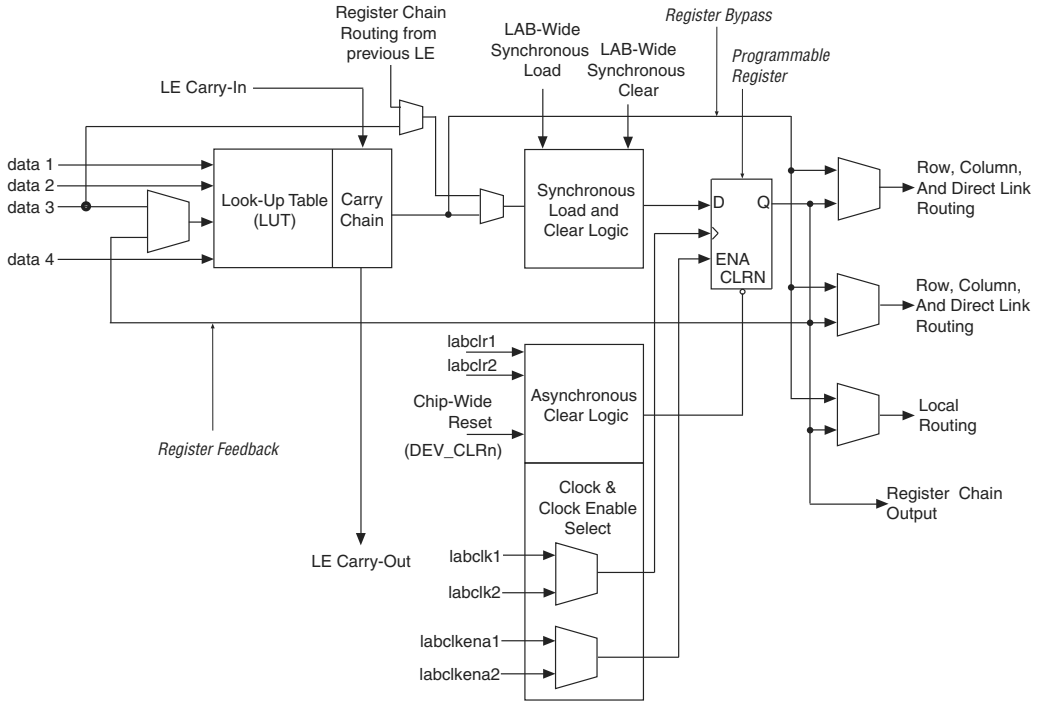
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4713
Number of Logic Elements/Cells	75408
Total RAM Bits	2810880
Number of I/O	426
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce75f29c8ln

Figure 2–1 shows the LEs for Cyclone IV devices.

Figure 2–1. Cyclone IV Device LEs



LE Features

You can configure the programmable register of each LE for D, T, JK, or SR flipflop operation. Each register has data, clock, clock enable, and clear inputs. Signals that use the global clock network, general-purpose I/O pins, or any internal logic can drive the clock and clear control signals of the register. Either general-purpose I/O pins or the internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output independently drives these three outputs. Two LE outputs drive the column or row and direct link routing connections, while one LE drives the local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. The LAB-wide synchronous load control signal is not available when using register packing. For more information about the synchronous load control signal, refer to "LAB Control Signals" on page 2–6.

The register feedback mode allows the register output to feed back into the LUT of the same LE to ensure that the register is packed with its own fan-out LUT, providing another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

Table 5–6. Cyclone IV E PLL Features (Part 2 of 2)

Hardware Features	Availability
Loss of lock detection	✓

Notes to Table 5–6:

(1) C counters range from 1 through 512 if the output clock uses a 50% duty cycle. For any output clocks using a non-50% duty cycle, the post-scale counters range from 1 through 256.

(2) Only applicable if the input clock jitter is in the input jitter tolerance specifications.

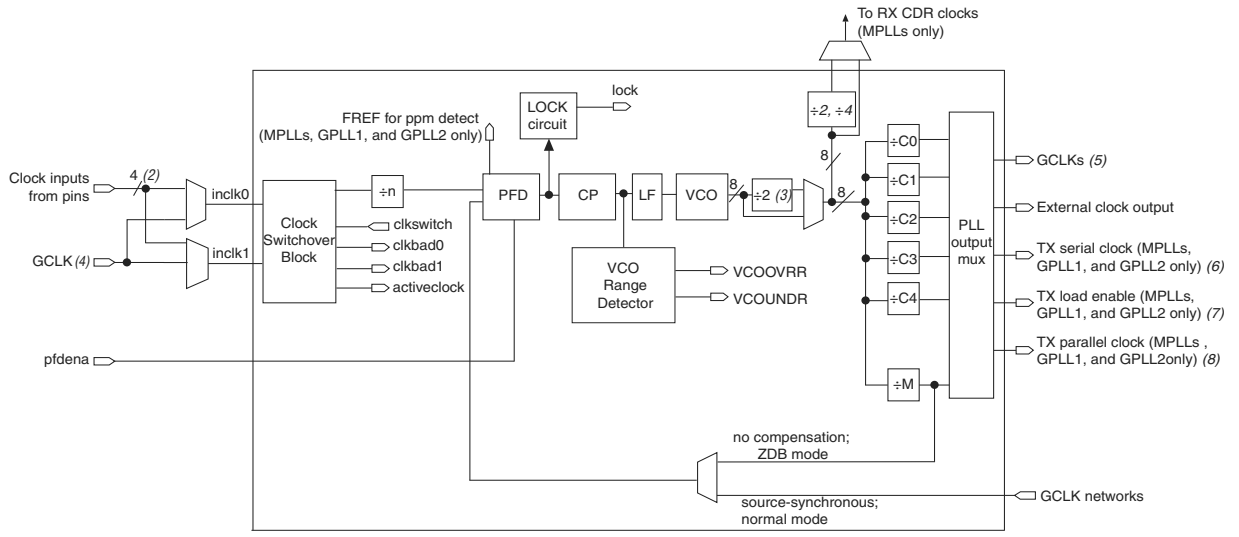
(3) The smallest phase shift is determined by the VCO period divided by eight. For degree increments, Cyclone IV E devices can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

Cyclone IV PLL Hardware Overview

This section gives a hardware overview of the Cyclone IV PLL.

Figure 5–9 shows a simplified block diagram of the major components of the PLL of Cyclone IV GX devices.

Figure 5–9. Cyclone IV GX PLL Block Diagram (1)



Notes to Figure 5–9:

(1) Each clock source can come from any of the four clock pins located on the same side of the device as the PLL.

(2) There are additional 4 pairs of dedicated differential clock inputs in EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices that can only drive general purpose PLLs and multipurpose PLLs on the left side of the device. `CLK[19..16]` can access `PLL_2`, `PLL_6`, `PLL_7`, and `PLL_8` while `CLK[23..20]` can access `PLL_1`, `PLL_5`, `PLL_6`, and `PLL_7`. For the location of these clock input pins, refer to Figure 5–3 on page 5–13.

(3) This is the VCO post-scale counter K.

(4) This input port is fed by a pin-driven dedicated GCLK, or through a clock control block if the clock control block is fed by an output from another PLL or a pin-driven dedicated GCLK. An internally generated global signal cannot drive the PLL.

(5) For the general purpose PLL and multipurpose PLL counter outputs connectivity to the GCLKs, refer to Table 5–1 on page 5–2 and Table 5–2 on page 5–4.

(6) Only the CI output counter can drive the TX serial clock.

(7) Only the C2 output counter can drive the TX load enable.

(8) Only the C3 output counter can drive the TX parallel clock.

Table 6–2 lists the I/O standards that support impedance matching and series termination.

Table 6–2. Cyclone IV Device I/O Features Support (Part 1 of 2)

I/O Standard	IOH/IOL Current Strength Setting (mA) (1), (9)		R_S OCT with Calibration Setting, Ohm (Ω)		R_S OCT Without Calibration Setting, Ohm (Ω)		Cyclone IV E I/O Banks Support	Cyclone IV GX I/O Banks Support	Slew Rate Option (6)	PCI-clamp Diode Support
	Column I/O	Row I/O	Column I/O	Row I/O (8)	Column I/O	Row I/O (8)				
3.3-V LVTTL	4,8	4,8	—	—	—	—	1,2,3,4,5,6,7,8	3,4,5,6,7,8,9	—	✓
3.3-V LVCMOS	2	2	—	—	—	—			—	✓
3.0-V LVTTL	4,8,12,16	4,8,12,16	50,25	50,25	50,25	50,25			0,1,**2**	✓
3.0-V LVCMOS	4,8,12,16	4,8,12,16	50,25	50,25	50,25	50,25				✓
3.0-V PCI/PCI-X	—	—	—	—	—	—			—	✓
2.5-V LVTTL/LVCMOS	4,8,12,16	4,8,12,16	50,25	50,25	50,25	50,25			0,1,**2**	✓
1.8-V LVTTL/LVCMOS	2,4,6,8,10,12,16	2,4,6,8,10,12,16	50,25	50,25	50,25	50,25				—
1.5-V LVCMOS	2,4,6,8,10,12,16	2,4,6,8,10,12,16	50,25	50,25	50,25	50,25				—
1.2-V LVCMOS	2,4,6,8,10,12	2,4,6,8,10	50,25	50	50,25	50		4,5,6,7,8		—
SSTL-2 Class I	8,12	8,12	50	50	50	50		3,4,5,6,7,8,9		—
SSTL-2 Class II	16	16	25	25	25	25				—
SSTL-18 Class I	8,10,12	8,10,12	50	50	50	50				—
SSTL-18 Class II	12,16	12,16	25	25	25	25				—
HSTL-18 Class I	8,10,12	8,10,12	50	50	50	50				—
HSTL-18 Class II	16	16	25	25	25	25				—
HSTL-15 Class I	8,10,12	8,10,12	50	50	50	50				—
HSTL-15 Class II	16	16	25	25	25	25				—
HSTL-12 Class I	8,10,12	8,10	50	50	50	50		4,5,6,7,8		—
HSTL-12 Class II	14	—	25	—	25	—	3,4,7,8	4,7,8		—
Differential SSTL-2 Class I (2), (7)	8,12	8,12	50	50	50	50	1,2,3,4,5,6,7,8	3,4,5,6,7,8	0,1,**2**	—
Differential SSTL-2 Class II (2), (7)	16	16	25	25	25	25				—
Differential SSTL-18 (2), (7)	8,10,12	—	50	—	50	—				—
Differential HSTL-18 (2), (7)	8,10,12	—	50	—	50	—				—
Differential HSTL-15 (2), (7)	8,10,12	—	50	—	50	—				—
Differential HSTL-12 (2), (7)	8,10,12	—	50	—	50	—	3,4,7,8	4,7,8		—

High-Speed I/O Interface

Cyclone IV E I/Os are separated into eight I/O banks, as shown in Figure 6–9 on page 6–17. Cyclone IV GX I/Os are separated into six user I/O banks with the left side of the device as the transceiver block, as shown in Figure 6–10 on page 6–18. Each bank has an independent power supply. True output drivers for LVDS, RSDS, mini-LVDS, and PPDS are on the right I/O banks. On the Cyclone IV E row I/O banks and the Cyclone IV GX right I/O banks, some of the differential pin pairs (`p` and `n` pins) of the true output drivers are not located on adjacent pins. In these cases, a power pin is located between the `p` and `n` pins. These I/O standards are also supported on all I/O banks using two single-ended output with the second output programmed as inverted, and an external resistor network. True input buffers for these I/O standards are supported on the top, bottom, and right I/O banks except for I/O bank 9.

Table 6–9. Cyclone IV GX I/O, Differential, and XCVRs Channel Count

Device	4CGX15	4CGX22		4CGX30			4CGX50		4CGX75		4CGX110			4CGX150		
Numbers of Differential Channels (1), (2)	169-FBGA	169-FBGA	324-FBGA	169-FBGA	324-FBGA	484-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	896-FBGA	484-FBGA	672-FBGA	896-FBGA
User I/O (3)	72	72	150	72	150	290	290	310	290	310	270	393	475	270	393	475
User I/O banks	9 (4)	9 (4)	9 (4)	9 (4)	9 (4)	11 (5)	11 (5), (6)	11 (5), (6)	11 (5), (6)	11 (5), (6)	11 (5), (6)	11 (5), (6)	11 (5), (6)	11 (5), (6)	11 (5), (6)	11 (5), (6)
LVDS (7), (9)	9	9	16	9	16	45	45	51	45	51	38	52	63	38	52	63
Emulated LVDS (8), (9)	16	16	48	16	48	85	85	89	85	89	82	129	157	82	129	157
XCVRs	2	2	4	2	4	4	4	8	4	8	4	8	8	4	8	8

Notes to Table 6–9:

(1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as outputs only.

(2) For differential pad placement guidelines, refer to "Pad Placement" on page 6–23.

(3) The I/O pin count includes all GPIOs, dedicated clock pins, and dual-purpose configuration pins. Transceivers pins and dedicated configuration pins are not included in the pin count.

(4) Includes one configuration I/O bank and two dedicated clock input I/O banks for HSSI input reference clock.

(5) Includes one configuration I/O bank and four dedicated clock input I/O banks for HSSI input reference clock.

(6) Single-ended clock input support is available for dedicated clock input I/O banks 3B (pins CLKIO20 and CLKIO22) and 8B (pins CLKIO17 and CLKIO19).

(7) The true LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in right I/O banks 5 and 6.

(8) The emulated LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in column I/O banks 3, 4, 7, and 8.

(9) LVDS input and output buffers are sharing the same p and n pins. One LVDS I/O channel can only be either transmitter or receiver at a time.

High-Speed I/O Standards Support

This section provides information about the high-speed I/O standards and the HSSI input reference clock supported in Cyclone IV devices.

High Speed Serial Interface (HSSI) Input Reference Clock Support

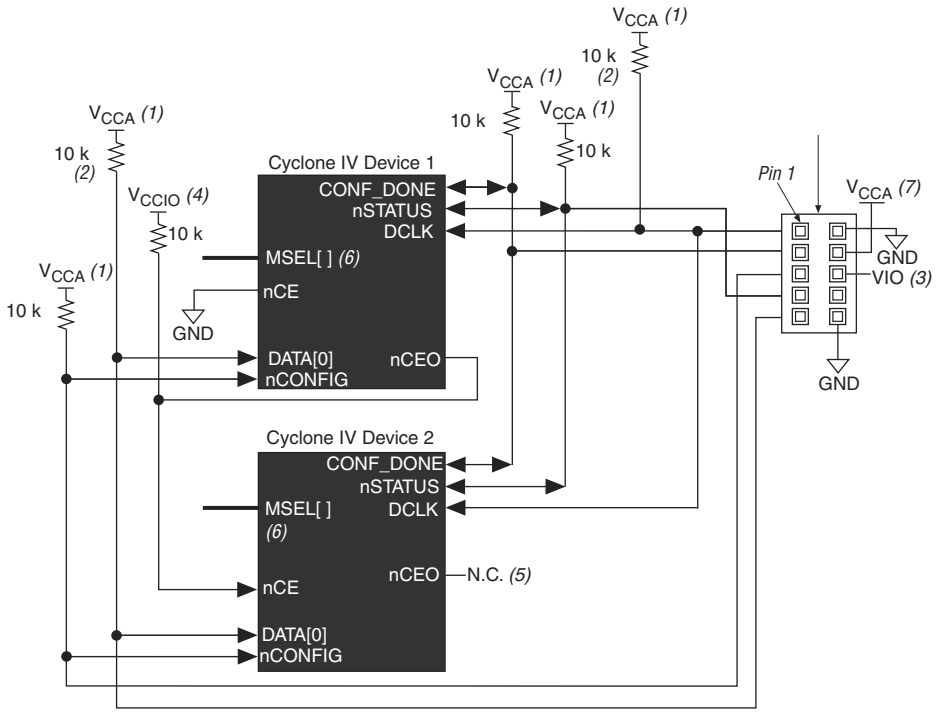
Cyclone IV GX devices support the same I/O features for GPIOs with additional new features where current I/O banks 3A and 8A consist of dual-purpose clock input pins (CLKIN) and 3B and 8B consist of dedicated CLKIN that can be used to support the high-speed transceiver input reference clock (REFCLK) features on top of the general-purpose clock input function.

The EP4CGX15, EP4CGX22, and EP4CGX30 devices contain two pairs of CLKIN/REFCLK pins located in I/O banks 3A and 8A. I/O banks 3B and 8B are not available in EP4CGX15, EP4CGX22, and EP4CGX30 devices. The EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have a total of four pairs of CLKIN/REFCLK pins located in I/O banks 3A, 3B, 8A, and 8B. I/O banks 3B and 8B can also support single-ended clock inputs. For more information about the CLKIN/REFCLK pin location, refer to Figure 6–10 on page 6–18 and Figure 6–11 on page 6–19.

You can use a download cable to configure multiple Cyclone IV device configuration pins. nCONFIG, nSTATUS, DCLK, DATA[0], and CONF_DONE are connected to every device in the chain. All devices in the chain utilize and enter user mode at the same time because all CONF_DONE pins are tied together.

In addition, the entire chain halts configuration if any device detects an error because the nSTATUS pins are tied together. Figure 8–18 shows the PS configuration for multiple Cyclone IV devices using a MasterBlaster, USB-Blaster, ByteBlaster II, or ByteBlasterMV cable.

Figure 8–18. Multi-Device PS Configuration Using a Download Cable



Notes to Figure 8–18:

(1) You must connect the pull-up resistor to the same supply voltage as the V_{CCA} supply.

(2) The pull-up resistors on DATA[0] and DCLK are only required if the download cable is the only configuration scheme used on your board. This ensures that DATA[0] and DCLK are not left floating after configuration. For example, if you also use a configuration device, the pull-up resistors on DATA[0] and DCLK are not required.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} must match the V_{CCA} of the device. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. When using the ByteBlasterMV download cable, this pin is a no connect. When using USB-Blaster, ByteBlaster II, and EthernetBlaster cables, this pin is connected to nCE when it is used for AS programming. Otherwise, it is a no connect.

(4) Connect the pull-up resistor to the V_{CCIO} supply voltage of the I/O bank in which the nCE pin resides.

(5) The nCEO pin of the last device in the chain is left unconnected or used as a user I/O pin.

(6) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL for PS configuration schemes, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to V_{CCA} or GND.

(7) Power up the V_{CC} of the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5 V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

When Cyclone IV devices successfully load the application configuration, they enter user mode. In user mode, the soft logic (the Nios II processor or state machine and the remote communication interface) assists the Cyclone IV device in determining when a remote system update is arriving. When a remote system update arrives, the soft logic receives the incoming data, writes it to the configuration memory device and triggers the device to load the factory configuration. The factory configuration reads the remote system upgrade status register, determines the valid application configuration to load, writes the remote system upgrade control register accordingly, and starts system reconfiguration.

☞ WYSIWYG is an optimization technique that performs optimization on a VQM (Verilog Quartus Mapping) netlist in the Quartus II software.

Error Detection Block

Table 9–3 lists the types of CRC detection to check the configuration bits.

Table 9–3. Types of CRC Detection to Check the Configuration Bits

First Type of CRC Detection	Second Type of CRC Detection
■ CRAM error checking ability (32-bit CRC) during user mode, for use by the CRC_ERROR pin. ■ There is only one 32-bit CRC value. This value covers all the CRAM data.	■ 16-bit CRC embedded in every configuration data frame. ■ During configuration, after a frame of data is loaded into the device, the pre-computed CRC is shifted into the CRC circuitry. ■ Simultaneously, the CRC value for the data frame shifted-in is calculated. If the pre-computed CRC and calculated CRC values do not match, nSTATUS is set low. ■ Every data frame has a 16-bit CRC. Therefore, there are many 16-bit CRC values for the whole configuration bit stream. ■ Every device has a different length of configuration data frame.

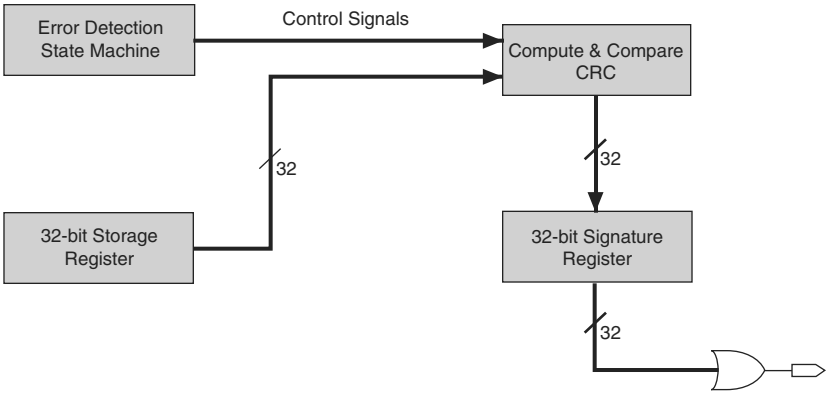
This section focuses on the first type—the 32-bit CRC when the device is in user mode.

Error Detection Registers

There are two sets of 32-bit registers in the error detection circuitry that store the computed CRC signature and pre-calculated CRC value. A non-zero value on the signature register causes the CRC_ERROR pin to set high.

Figure 9–1 shows the block diagram of the error detection block and the two related 32-bit registers: the signature register and the storage register.

Figure 9–1. Error Detection Block Diagram



Document Revision History

Table 10–3 lists the revision history for this chapter.

Table 10–3. Document Revision History

Date	Version	Changes
December 2013	1.3	■ Updated the “EXTEST_PULSE” section.
November 2011	1.2	■ Updated the “BST Operation Control” section. ■ Updated Table 10–2.
February 2010	1.1	■ Added Cyclone IV E devices in Table 10–1 and Table 10–2 for the Quartus II software version 9.1 SP1 release. ■ Updated Figure 10–1 and Figure 10–2. ■ Minor text edits.
November 2009	1.0	Initial release.

- Programmable equalization—boosts the high-frequency gain of the incoming signal up to 7 dB. This compensates for the low-pass filter effects of the transmission media. The amount of high-frequency gain required depends on the loss characteristics of the physical medium.
- Programmable DC gain—provides equal boost to incoming signal across the frequency spectrum with DC gain settings up to 6 dB.
- Programmable differential OCT—provides calibrated OCT at 100 Ω or 150 Ω with on-chip receiver common mode voltage at 0.82 V. The common mode voltage is tri-stated when you disable the OCT to use external termination.
- Offset cancellation—corrects the analog offset voltages that might exist from process variations between the positive and negative differential signals in the equalizer stage and CDR circuit.
- Signal detection—detects if the signal level present at the receiver input buffer is higher than the threshold with a built-in signal threshold detection circuitry. The circuitry has a hysteresis response that filters out any high-frequency ringing caused by ISI effects or high-frequency losses in the transmission medium. Detection is indicated by the assertion of the `rx_signaldetect` signal. Signal detection is only supported when 8B/10B encoder/decoder block is enabled. When not supported, the `rx_signaldetect` signal is forced high, bypassing the signal detection function.

Disable OCT to use external termination if the link requires a 85 Ω termination, such as when you are interfacing with certain PCIe Gen1 or Gen2 capable devices.

For specifications on programmable equalization and DC gain settings, refer to the *Cyclone IV Device Data Sheet*.

Table 1–25. PRBS, High and Low Frequency Patterns, and Channel Settings (Part 2 of 2)

Patterns	Polynomial	8-bit Channel Width				10-bit Channel Width			
		Channel Width of 8 bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages	Channel Width of 10-bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages
Low Frequency (2)	1111100000	N	—	—	—	Y	—	2.5	3.125

Notes to Table 1–25:

(1) Channel width refers to the **What is the channel width?** option in the **General** screen of the ALTGX MegaWizard Plug-In Manager. Based on the selection, an 8 or 10 bits wide pattern is generated as indicated by a **Yes (Y)** or **No (N)**.

(2) A verifier and associated `rx_bistdone` and `rx_bisterr` signals are not available for the specified patterns.

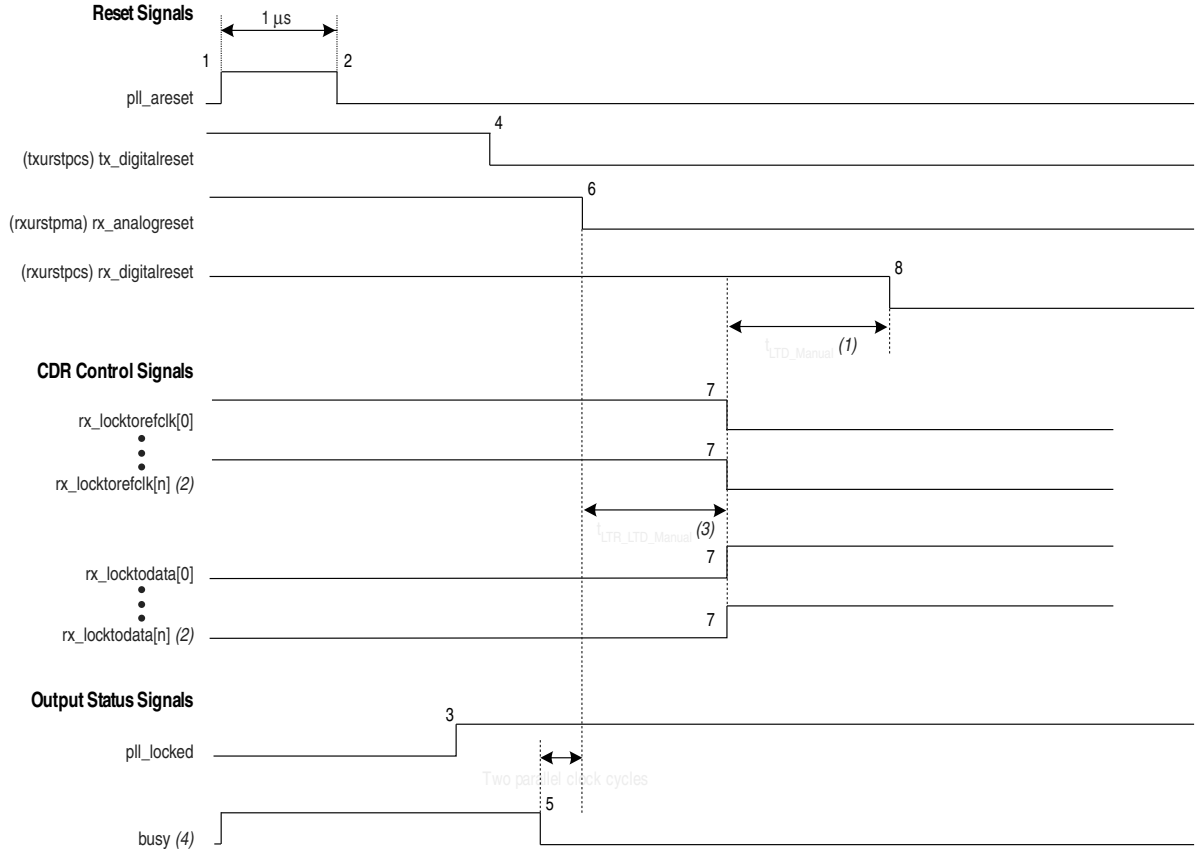
You can enable the serial loopback option to loop the generated PRBS patterns to the receiver channel for verifier to check the PRBS patterns. When the PRBS pattern is received, the `rx_bisterr` and `rx_bistdone` signals indicate the status of the verifier. After the word aligner restores the word boundary, the `rx_bistdone` signal is driven high when the verifier receives a complete pattern cycle and remains asserted until it is reset using the `rx_digitalreset` port. After the assertion of `rx_bistdone`, the `rx_bisterr` signal is asserted for a minimum of three `rx_clkout` cycles when errors are detected in the data and deasserts if the following PRBS sequence contains no error. You can reset the PRBS pattern generator and verifier by asserting the `tx_digitalreset` and `rx_digitalreset` ports, respectively.

4. For the receiver operation, after deassertion of `busy` signal, wait for two parallel clock cycles to deassert the `rx_analogreset` signal.
5. Wait for the `rx_freqlocked` signal from each channel to go high. The `rx_freqlocked` signal of each channel may go high at different times (indicated by the slashed pattern at marker 7).
6. In a bonded channel group, when the `rx_freqlocked` signals of all the channels has gone high, from that point onwards, wait for at least t_{LTD_Auto} time for the receiver parallel clock to be stable, then deassert the `rx_digitalreset` signal (marker 8). At this point, all the receivers are ready for data traffic.

Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode

This configuration contains both a transmitter and receiver channel. When the receiver CDR is in manual lock mode, use the reset sequence shown in Figure 2–5.

Figure 2–5. Sample Reset Sequence for Bonded Configuration Receiver and Transmitter Channels—Receiver CDR in Manual Lock Mode



Notes to Figure 2–5:

(1) For t_{LTD_Manual} duration, refer to the *Cyclone IV Device Datasheet* chapter.
(2) The number of `rx_locktorefclk[n]` and `rx_locktodata[n]` signals depend on the number of channels configured. `n`=number of channels.
(3) For $t_{LTR\_LTD\_Manual}$ duration, refer to the *Cyclone IV Device Datasheet* chapter.
(4) The `busy` signal is asserted and deasserted only during initial power up when offset cancellation occurs. In subsequent reset sequences, the `busy` signal is asserted and deasserted only if there is a read or write operation to the ALTGX_RECONFIG megafunction.

Document Revision History

Table 2–8 lists the revision history for this chapter.

Table 2–8. Document Revision History

Date	Version	Changes
September 2014	1.4	■ Removed the `rx_pll_locked` signal from the "Sample Reset Sequence of Receiver Only Channel—Receiver CDR in Manual Lock Mode" and the "Sample Reset Sequence of Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode" figures.
May 2013	1.3	■ Added rx_pll_locked to Figure 2–7 and Figure 2–9. ■ Added information on rx_pll_locked to "Receiver Only Channel—Receiver CDR in Manual Lock Mode" and "Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode".
November 2011	1.2	Updated the "All Supported Functional Modes Except the PCIe Functional Mode" section.
December 2010	1.1	■ Updated for the Quartus II software version 10.1 release. ■ Updated all `pll_powerdown` to `pll_areset`. ■ Added information about the `busy` signal in Figure 2–4, Figure 2–5, Figure 2–6, Figure 2–7, Figure 2–8, Figure 2–9, Figure 2–10, Figure 2–12, and Figure 2–13. ■ Added information for clarity ("Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode", "Receiver Only Channel—Receiver CDR in Automatic Lock Mode", "Receiver Only Channel—Receiver CDR in Manual Lock Mode", "Receiver and Transmitter Channel—Receiver CDR in Manual Lock Mode", and "Reset Sequence in Channel Reconfiguration Mode"). ■ Minor text edits.
July 2010	1.0	Initial release.

There are three methods that you can use to dynamically reconfigure the PMA controls of a transceiver channel:

- "Method 1: Using logical_channel_address to Reconfigure Specific Transceiver Channels" on page 3–14
- "Method 2: Writing the Same Control Signals to Control All the Transceiver Channels" on page 3–16
- "Method 3: Writing Different Control Signals for all the Transceiver Channels at the Same Time" on page 3–19

Method 1: Using logical_channel_address to Reconfigure Specific Transceiver Channels

Enable the `logical_channel_address` port by selecting the **Use 'logical_channel_address' port** option on the **Analog controls** tab. This method is applicable only for a design where the dynamic reconfiguration controller controls more than one channel.

You can additionally reconfigure either the receiver portion, transmitter portion, or both the receiver and transmitter portions of the transceiver channel by setting the corresponding value on the `rx_tx_duplex_sel` input port. For more information, refer to Table 3–2 on page 3–4.

Connecting the PMA Control Ports

The selected PMA control ports remain fixed in width, regardless of the number of channels controlled by the ALTGX_RECONFIG instance:

- `tx_vodctrl` and `tx_vodctrl_out` are fixed to 3 bits
- `tx_preemp` and `tx_preemp_out` are fixed to 5 bits
- `rx_eqdcgain` and `rx_eqdcgain_out` are fixed to 2 bits
- `rx_eqctrl` and `rx_eqctrl_out` are fixed to 4 bits

Write Transaction

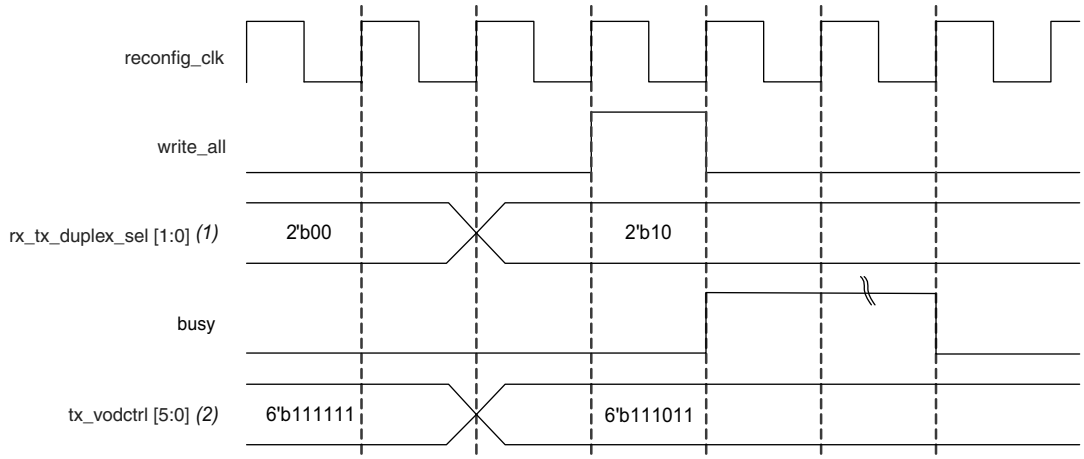
To complete a write transaction, perform the following steps:

1. Set the selected PMA control ports to the desired settings (for example, `tx_vodctrl` = **3'b001**).
2. Set the `logical_channel_address` input port to the logical channel address of the transceiver channel whose PMA controls you want to reconfigure.
3. Set the `rx_tx_duplex_sel` port to **2'b10** so that only the transmit PMA controls are written to the transceiver channel.
4. Ensure that the `busy` signal is low before you start a write transaction.
5. Assert the `write_all` signal for one `reconfig_clk` clock cycle.

The `busy` output status signal is asserted high to indicate that the dynamic reconfiguration controller is busy writing the PMA control values. When the write transaction has completed, the `busy` signal goes low.

Figure 3–8 shows a write transaction waveform with the **Use the same control signal for all the channels** option disabled.

Figure 3–8. Write Transaction Waveform—Use the same control signal for all the channels Option Disabled



Notes to Figure 3–8:

(1) In this waveform example, you want to write to only the transmitter portion of the channel.

(2) In this waveform example, the number of channels controlled by the dynamic reconfiguration controller (the ALTGX_RECONFIG instance) is two and that the `tx_vodctrl` control port is enabled.

☞ Simultaneous write and read transactions are not allowed.

Read Transaction

The read transaction in Method 3 is identical to that in Method 2. Refer to "Read Transaction" on page 3–18.

☞ This is the slowest method. You have to write all the PMA settings for all channels even if you may only be changing one parameter on the channel. Altera recommends using the `logical_channel_address` method for time-critical applications.

For each method, you can additionally reconfigure the PMA setting of both transmitter and receiver portion, transmitter portion only, or receiver portion only of the transceiver channel. For more information, refer to "Dynamic Reconfiguration Controller Port List" on page 3–4. You can enable the `rx_tx_duplex_sel` port by selecting the **Use 'rx_tx_duplex_sel' port to enable RX only, TX only or duplex reconfiguration** option on the **Error checks** tab of the ALTGX_RECONFIG MegaWizard Plug-In Manager.

Figure 3–9 shows the ALTGX_RECONFIG connection to the ALTGX instances when set in analog reconfiguration mode. For the port information, refer to the "Dynamic Reconfiguration Controller Port List" on page 3–4.

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Volume 3

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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This chapter provides additional information about the document and Altera.

About this Handbook

This handbook provides comprehensive information about the Altera® Cyclone® IV family of devices.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices (1), (2) (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT} (3)	Supply voltage for internal logic, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply voltage for internal logic, 1.0-V operation	—	0.97	1.0	1.03	V
V_{CCIO} (3), (4)	Supply voltage for output buffers, 3.3-V operation	—	3.135	3.3	3.465	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
V_{CCA} (3)	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
V_{CCD_PLL} (3)	Supply (digital) voltage for PLL, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply (digital) voltage for PLL, 1.0-V operation	—	0.97	1.0	1.03	V
V_I	Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
		For extended temperature	–40	—	125	°C
		For automotive use	–40	—	125	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) (5)	50 µs	—	50 ms	—
		Fast POR (6)	50 µs	—	3 ms	—

Document Revision History

Table 1–47 lists the revision history for this chapter.

Table 1–47. Document Revision History

Date	Version	Changes
December 2016	2.1	Added note to Table 1–9 and Table 1–10.
March 2016	2.0	Updated note (5) in Table 1–21 to remove support for the N148 package.
October 2014	1.9	Updated maximum value for V_{CCD_PLL} in Table 1–1. Removed extended temperature note in Table 1–3.
December 2013	1.8	Updated Table 1–21 by adding Note (15).
May 2013	1.7	Updated Table 1–15 by adding Note (4).
October 2012	1.6	■ Updated the maximum value for V_I, V_{CCD_PLL}, V_{CCIO}, V_{CC_CLKIN}, V_{CCH_GXB}, and V_{CCA_GXB} Table 1–1. ■ Updated Table 1–11 and Table 1–22. ■ Updated Table 1–21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock. ■ Updated Table 1–29 to include the typical DCLK value. ■ Updated the minimum f_{HSCLK} value in Table 1–31, Table 1–32, Table 1–33, Table 1–34, and Table 1–35.
November 2011	1.5	■ Updated “Maximum Allowed Overshoot or Undershoot Voltage”, “Operating Conditions”, and “PLL Specifications” sections. ■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21. ■ Updated Figure 1–1.
December 2010	1.4	■ Updated for the Quartus II software version 10.1 release. ■ Updated Table 1–21 and Table 1–25. ■ Minor text edits.
July 2010	1.3	Updated for the Quartus II software version 10.0 release: ■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45. ■ Updated Figure 1–2 and Figure 1–3. ■ Removed SW Requirement and TCCS for Cyclone IV Devices tables. ■ Minor text edits.
March 2010	1.2	Updated to include automotive devices: ■ Updated the “Operating Conditions” and “PLL Specifications” sections. ■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43. ■ Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os. ■ Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices. ■ Minor text edits.