Intel - EP4CE75U19I7N Datasheet





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Details

Product Status	Active
Number of LABs/CLBs	4713
Number of Logic Elements/Cells	75408
Total RAM Bits	2810880
Number of I/O	292
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep4ce75u19i7n

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Hardware Features	Availability
Loss of lock detection	\checkmark

Notes to Table 5-6:

- (1) C counters range from 1 through 512 if the output clock uses a 50% duty cycle. For any output clocks using a non-50% duty cycle, the post-scale counters range from 1 through 256.
- (2) Only applicable if the input clock jitter is in the input jitter tolerance specifications.
- (3) The smallest phase shift is determined by the VCO period divided by eight. For degree increments, Cyclone IV E devices can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

Cyclone IV PLL Hardware Overview

This section gives a hardware overview of the Cyclone IV PLL.

Figure 5–9 shows a simplified block diagram of the major components of the PLL of Cyclone IV GX devices.





Notes to Figure 5-9:

- (1) Each clock source can come from any of the four clock pins located on the same side of the device as the PLL.
- (2) There are additional 4 pairs of dedicated differential clock inputs in EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices that can only drive general purpose PLLs and multipurpose PLLs on the left side of the device. CLK [19..16] can access PLL_2, PLL_6, PLL_7, and PLL_8 while CLK [23..20] can access PLL_1, PLL_5, PLL_6, and PLL_7. For the location of these clock input pins, refer to Figure 5–3 on page 5–13.
- (3) This is the VCO post-scale counter K.
- (4) This input port is fed by a pin-driven dedicated GCLK, or through a clock control block if the clock control block is fed by an output from another PLL or a pin-driven dedicated GCLK. An internally generated global signal cannot drive the PLL.
- (5) For the general purpose PLL and multipurpose PLL counter outputs connectivity to the GCLKs, refer to Table 5–1 on page 5–2 and Table 5–2 on page 5–4.
- (6) Only the CI output counter can drive the TX serial clock.
- (7) Only the C2 output counter can drive the TX load enable.
- (8) Only the C3 output counter can drive the TX parallel clock.

Clock Feedback Modes

Cyclone IV PLLs support up to five different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. For the supported feedback modes, refer to Table 5–5 on page 5–18 for Cyclone IV GX PLLs and Table 5–6 on page 5–19 for Cyclone IV E PLLs.



² Input and output delays are fully compensated by the PLL only if you are using the dedicated clock input pins associated with a given PLL as the clock sources.

When driving the PLL using the GCLK network, the input and output delays may not be fully compensated in the Quartus II software.

Source-Synchronous Mode

If the data and clock arrive at the same time at the input pins, the phase relationship between the data and clock remains the same at the data and clock ports of any I/O element input register.

Figure 5–12 shows an example waveform of the data and clock in this mode. Use this mode for source-synchronous data transfers. Data and clock signals at the I/O element experience similar buffer delays as long as the same I/O standard is used.





Source-synchronous mode compensates for delay of the clock network used, including any difference in the delay between the following two paths:

- Data pin to I/O element register input
- Clock input pin to the PLL phase frequency detector (PFD) input

Set the input pin to the register delay chain in the I/O element to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL. Also, all data pins must use the **PLL COMPENSATED logic** option in the Quartus II software.

Differential I/O Standards	I/O Bank Location	External Resistor Network at Transmitter	Transmitter (TX)	Receiver (RX)	
	5,6	Not Required			
	3,4,5,6,7,8	Three Resistors	`	v	
	5,6	Not Required			
RSDS	3,4,7,8	Three Resistors	✓	—	
	3,4,5,6,7,8	Single Resistor			
	5,6	Not Required			
111111-LVD3	3,4,5,6,7,8	Three Resistors	`		
סחמס	5,6	Not Required			
FFD3	3,4,5,6,7,8 Three Resistors		`		
BLVDS (1)	3,4,5,6,7,8	Single Resistor	\checkmark	\checkmark	
LVPECL (2)	3,4,5,6,7,8	—	—	\checkmark	
Differential SSTL-2 ⁽³⁾	3,4,5,6,7,8	—	\checkmark	\checkmark	
Differential SSTL-18 (3)	3,4,5,6,7,8	—	\checkmark	\checkmark	
Differential HSTL-18 (3)	3,4,5,6,7,8	—	\checkmark	\checkmark	
Differential HSTL-15 (3)	3,4,5,6,7,8	—	\checkmark	\checkmark	
Differential HSTL-12 ⁽³⁾	4,5,6,7,8	—	~	\checkmark	

Table 6–7. Differential I/O Standards Supported in Cyclone IV GX I/O Banks

Notes to Table 6-7:

(1) Transmitter and Receiver f_{MAX} depend on system topology and performance requirement.

(2) The LVPECL I/O standard is only supported on dedicated clock input pins.

(3) The differential SSTL-2, SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards are only supported on clock input pins and PLL output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

You can use I/O pins and internal logic to implement a high-speed differential interface in Cyclone IV devices. Cyclone IV devices do not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal phase-locked loops (PLLs), and I/O cells are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data. The differential interface data serializers and deserializers (SERDES) are automatically constructed in the core logic elements (LEs) with the Quartus II software ALTLVDS megafunction.

In Cyclone IV devices, the DM pins are preassigned in the device pinouts. The Quartus II Fitter treats the DQ and DM pins in a DQS group equally for placement purposes. The preassigned DQ and DM pins are the preferred pins to use.

Some DDR2 SDRAM and DDR SDRAM devices support error correction coding (ECC), a method of detecting and automatically correcting errors in data transmission. In 72-bit DDR2 or DDR SDRAM, there are eight ECC pins and 64 data pins. Connect the DDR2 and DDR SDRAM ECC pins to a separate DQS or DQ group in Cyclone IV devices. The memory controller needs additional logic to encode and decode the ECC data.

Address and Control/Command Pins

The address signals and the control or command signals are typically sent at a single data rate. You can use any of the user I/O pins on all I/O banks of Cyclone IV devices to generate the address and control or command signals to the memory device.

Cyclone IV devices do not support QDR II SRAM in the burst length of two.

Memory Clock Pins

In DDR2 and DDR SDRAM memory interfaces, the memory clock signals (CK and CK#) are used to capture the address signals and the control or command signals. Similarly, QDR II SRAM devices use the write clocks (K and K#) to capture the address and command signals. The CK/CK# and K/K# signals are generated to resemble the write-data strobe using the DDIO registers in Cyclone IV devices.

CK/CK# pins must be placed on differential I/O pins (DIFFIO in Pin Planner) and in the same bank or on the same side as the data pins. You can use either side of the device for wraparound interfaces. As seen in the Pin Planner Pad View, CK0 cannot be located in the same row and column pad group as any of the interfacing DQ pins.



Cyclone IV Devices Memory Interfaces Features

This section discusses Cyclone IV memory interfaces, including DDR input registers, DDR output registers, OCT, and phase-lock loops (PLLs).

DDR Input Registers

The DDR input registers are implemented with three internal logic element (LE) registers for every DQ pin. These LE registers are located in the logic array block (LAB) adjacent to the DDR input pin.

DDR Output Registers

A dedicated write DDIO block is implemented in the DDR output and output enable paths.

Figure 7–8 shows how a Cyclone IV dedicated write DDIO block is implemented in the I/O element (IOE) registers.

Figure 7–8. Cyclone IV Dedicated Write DDIO



The two DDR output registers are located in the I/O element (IOE) block. Two serial data streams routed through datain_l and datain_h, are fed into two registers, output register Ao and output register Bo, respectively, on the same clock edge. The output from output register Ao is captured on the falling edge of the clock, while the output from output register Bo is captured on the rising edge of the clock. The registered outputs are multiplexed by the common clock to drive the DDR output pin at twice the data rate.

The DDR output enable path has a similar structure to the DDR output path in the IOE block. The second output enable register provides the write preamble for the DQS strobe in DDR external memory interfaces. This active-low output enable register extends the high-impedance state of the pin by half a clock cycle to provide the external memory's DQS write preamble time specification.

To For more information about Cyclone IV IOE registers, refer to the *Cyclone IV Device I/O Features* chapter.

Figure 7–9 illustrates how the second output enable register extends the DQS high-impedance state by half a clock cycle during a write operation.



Figure 7–9. Extending the OE Disable by Half a Clock Cycle for a Write Transaction ⁽¹⁾

Note to Figure 7-9:

(1) The waveform reflects the software simulation result. The OE signal is an active low on the device. However, the Quartus II software implements the signal as an active high and automatically adds an inverter before the A_{OE} register D input.

OCT with Calibration

Cyclone IV devices support calibrated on-chip series termination (R_S OCT) in both vertical and horizontal I/O banks. To use the calibrated OCT, you must use the RUP and RDN pins for each R_S OCT control block (one for each side). You can use each OCT calibration block to calibrate one type of termination with the same V_{CCIO} for that given side.

 For more information about the Cyclone IV devices OCT calibration block, refer to the Cyclone IV Device I/O Features chapter.

PLL

When interfacing with external memory, the PLL is used to generate the memory system clock, the write clock, the capture clock and the logic-core clock. The system clock generates the DQS write signals, commands, and addresses. The write-clock is shifted by -90° from the system clock and generates the DQ signals during writes. You can use the PLL reconfiguration feature to calibrate the read-capture phase shift to balance the setup and hold margins.

- The PLL is instantiated in the ALTMEMPHY megafunction. All outputs of the PLL are used when the ALTMEMPHY megafunction is instantiated to interface with external memories. PLL reconfiguration is used in the ALTMEMPHY megafunction to calibrate and track the read-capture phase to maintain the optimum margin.
- **For more information about usage of PLL outputs by the ALTMEMPHY** megafunction, refer to the *External Memory Interface Handbook*.

Remote System Upgrade

Cyclone IV devices support remote system upgrade in AS and AP configuration schemes. You can also implement remote system upgrade with advanced Cyclone IV features such as real-time decompression of configuration data in the AS configuration scheme.

Remote system upgrade is not supported in a multi-device configuration chain for any configuration scheme.

Functional Description

The dedicated remote system upgrade circuitry in Cyclone IV devices manages remote configuration and provides error detection, recovery, and status information. A Nios[®] II processor or a user logic implemented in the Cyclone IV device logic array provides access to the remote configuration data source and an interface to the configuration memory.

Configuration memory refers to serial configuration devices (EPCS) or supported parallel flash memory, depending on the configuration scheme that is used.

The remote system upgrade process of the Cyclone IV device consists of the following steps:

- 1. A Nios II processor (or user logic) implemented in the Cyclone IV device logic array receives new configuration data from a remote location. The connection to the remote source is a communication protocol, such as the transmission control protocol/Internet protocol (TCP/IP), peripheral component interconnect (PCI), user datagram protocol (UDP), universal asynchronous receiver/transmitter (UART), or a proprietary interface.
- 2. The Nios II processor (or user logic) writes this new configuration data into a configuration memory.
- 3. The Nios II processor (or user logic) starts a reconfiguration cycle with the new or updated configuration data.
- 4. The dedicated remote system upgrade circuitry detects and recovers from any error that might occur during or after the reconfiguration cycle and provides error status information to the user design.

Figure 8–30 shows the steps required for performing remote configuration updates (the numbers in Figure 8–30 coincide with steps 1–3).

Figure 8–30. Functional Diagram of Cyclone IV Device Remote System Upgrade



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Remote System Upgrade Mode

In remote update mode, Cyclone IV devices load the factory configuration image after power up. The user-defined factory configuration determines the application configuration to be loaded and triggers a reconfiguration cycle. The factory configuration can also contain application logic.

When used with configuration memory, the remote update mode allows an application configuration to start at any flash sector boundary. Additionally, the remote update mode features a user watchdog timer that can detect functional errors in an application configuration.

Remote Update Mode

In AS configuration scheme, when a Cyclone IV device is first powered up in remote update, it loads the factory configuration located at address <code>boot_address[23:0] = 24b'0</code>. Altera recommends storing the factory configuration image for your system at boot address 24b'0, which corresponds to the start address location 0×000000 in the serial configuration device. A factory configuration image is a bitstream for the Cyclone IV device in your system that is programmed during production and is the fall-back image when an error occurs. This image is stored in non-volatile memory and is never updated or modified using remote access.

When you use the AP configuration in Cyclone IV E devices, the Cyclone IV E device loads the default factory configuration located at the following address after device power-up in remote update mode:

boot_address[23:0] = 24'h010000 = 24'b1 0000 0000 0000.

You can change the default factory configuration address to any desired address using the APFC_BOOT_ADDR JTAG instruction. The factory configuration image is stored in non-volatile memory and is never updated or modified using remote access. This corresponds to the default start address location 0×010000 represented in 16-bit word addressing (or the updated address if the default address is changed) in the supported parallel flash memory. For more information about the application of the APFC_BOOT_ADDR JTAG instruction in AP configuration scheme, refer to the "JTAG Instructions" on page 8–57.

The factory configuration image is user-designed and contains soft logic (Nios II processor or state machine and the remote communication interface) to:

- Process any errors based on status information from the dedicated remote system upgrade circuitry
- Communicate with the remote host and receive new application configurations and store the new configuration data in the local non-volatile memory device
- Determine the application configuration to be loaded into the Cyclone IV device
- Enable or disable the user watchdog timer and load its time-out value (optional)
- Instruct the dedicated remote system upgrade circuitry to start a reconfiguration cycle

Figure 8–32 shows the transitions between the factory configuration and application configuration in remote update mode.





After power up or a configuration error, the factory configuration logic writes the remote system upgrade control register to specify the address of the application configuration to be loaded. The factory configuration also specifies whether or not to enable the user watchdog timer for the application configuration and, if enabled, specifies the timer setting.

Only valid application configurations designed for remote update mode include the logic to reset the timer in user mode. For more information about the user watchdog timer, refer to the "User Watchdog Timer" on page 8–79.

If there is an error while loading the application configuration, the remote system upgrade status register is written by the dedicated remote system upgrade circuitry of the Cyclone IV device to specify the cause of the reconfiguration.

The following actions cause the remote system upgrade status register to be written:

- nSTATUS driven low externally
- Internal cyclical redundancy check (CRC) error
- User watchdog timer time-out
- A configuration reset (logic array nCONFIG signal or external nCONFIG pin assertion)

The Cyclone IV device automatically loads the factory configuration when an error occurs. This user-designed factory configuration reads the remote system upgrade status register to determine the reason for reconfiguration. Then the factory configuration takes the appropriate error recovery steps and writes to the remote system upgrade control register to determine the next application configuration to be loaded.

Dedicated Remote System Upgrade Circuitry

This section describes the implementation of the Cyclone IV device remote system upgrade dedicated circuitry. The remote system upgrade circuitry is implemented in hard logic. This dedicated circuitry interfaces with the user-defined factory application configurations implemented in the Cyclone IV device logic array to provide the complete remote configuration solution. The remote system upgrade circuitry contains the remote system upgrade registers, a watchdog timer, and state machines that control those components. Figure 8–33 shows the data path of the remote system upgrade block.

Figure 8–33. Remote System Upgrade Circuit Data Path (1)



Notes to Figure 8-33:

- (1) The RU_DOUT, RU_SHIFTnLD, RU_CAPTNUPDT, RU_CLK, RU_DIN, RU_nCONFIG, and RU_nRSTIMER signals are internally controlled by the ALTREMOTE_UPDATE megafunction.
- (2) The RU_CLK refers to the ALTREMOTE_UPDATE megafunction block "clock" input. For more information, refer to the *Remote Update Circuitry* (ALTREMOTE_UPDATE) Megafunction User Guide.

Remote System Upgrade Registers

The remote system upgrade block contains a series of registers that stores the configuration addresses, watchdog timer settings, and status information. Table 8–22 lists these registers.

 Table 8–22.
 Remote System Upgrade Registers

Register	Description
Shift register	This register is accessible by the logic array and allows the update, status, and control registers to be written and sampled by user logic. Write access is enabled in remote update mode for factory configurations to allow writing to the update register. Write access is disabled for all application configurations in remote update mode.
Control register	This register contains the current configuration address, the user watchdog timer settings, one option bit for checking early CONF_DONE, and one option bit for selecting the internal oscillator as the startup state machine clock. During a read operation in an application configuration, this register is read into the shift register. When a reconfiguration cycle is started, the contents of the update register are written into the control register.
Update register	This register contains data similar to that in the control register. However, it can only be updated by the factory configuration by shifting data into the shift register and issuing an update operation. When a reconfiguration cycle is triggered by the factory configuration, the control register is updated with the contents of the update register. During a read in a factory configuration, this register is read into the shift register.
Status register	This register is written by the remote system upgrade circuitry on every reconfiguration to record the cause of the reconfiguration. This information is used by the factory configuration to determine the appropriate action following a reconfiguration. During a capture cycle, this register is read into the shift register.

The control and status registers of the remote system upgrade are clocked by the 10-MHz internal oscillator (the same oscillator that controls the user watchdog timer) or the CLKUSR. However, the shift and update registers of the remote system upgrade are clocked by the maximum frequency of 40-MHz user clock input (RU_CLK). There is no minimum frequency for RU_CLK.

Remote System Upgrade Control Register

The remote system upgrade control register stores the application configuration address, the user watchdog timer settings, and option bits for a application configuration. In remote update mode for the AS configuration scheme, the control register address bits are set to all zeros (24'b0) at power up to load the AS factory configuration. In remote update mode for the AP configuration scheme, the control register address bits are set to 24'h010000 (24'b1 0000 0000 0000) at power up to load the AP default factory configuration. However, for the AP configuration scheme, you can change the default factory configuration address to any desired address using the APFC_BOOT_ADDR JTAG instruction. Additionally, a factory configuration in remote update mode has write access to this register.

Visual Cue	Meaning
	Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. The suffix n denotes an active-low signal. For example, resetn.
Courier type	Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf.
	Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI).
4	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets indicate a list of items when the sequence of the items is not important.
LP	The hand points to information that requires special attention.
0	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
▋┯∎	The multimedia icon directs you to a related multimedia presentation.
CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
VIARNING	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.

The following describes the 8B/10B encoder behavior in reset condition (as shown in Figure 1–7):

- During reset, the 8B/10B encoder ignores the inputs (tx_datain and tx_ctrlenable ports) from the FPGA fabric and outputs the K28.5 pattern from the RD- column continuously until the tx_digitalreset port is deasserted.
- Upon deassertion of the tx_digitalreset port, the 8B/10B encoder starts with a negative disparity and transmits three K28.5 code groups for synchronization before it starts encoding and transmitting data on its output.
- Due to some pipelining of the transmitter PCS, some "don't cares" (10'hxxx) are sent before the three synchronizing K28.5 code groups.

clock tx_digitalreset dataout[9..0] K28.5 K28.5-K28.5 K28.5-. K28.5+ K28.5-Dx.y+ ххх ххх Normal During reset Don't cares after reset Synchronization operation

Figure 1–7. 8B/10B Encoder Behavior in Reset Condition

The encoder supports forcing the running disparity to either positive or negative disparity with tx_forcedisp and tx_dispval ports. Figure 1–8 shows an example of tx_forcedisp and tx_dispval port use, where data is shown in hexadecimal radix.



Figure 1–8. Force Running Disparity Operation

In this example, a series of K28.5 code groups are continuously sent. The stream alternates between a positive disparity K28.5 (RD+) and a negative disparity K28.5 (RD-) to maintain a neutral overall disparity. The current running disparity at time n + 1 indicates that the K28.5 in time n + 2 should be encoded with a negative disparity. Because tx_forcedisp is high at time n + 2, and tx_dispval is low, the K28.5

- Programmable equalization—boosts the high-frequency gain of the incoming signal up to 7 dB. This compensates for the low-pass filter effects of the transmission media. The amount of high-frequency gain required depends on the loss characteristics of the physical medium.
- Programmable DC gain—provides equal boost to incoming signal across the frequency spectrum with DC gain settings up to 6 dB.
- Programmable differential OCT—provides calibrated OCT at 100 Ω or 150 Ω with on-chip receiver common mode voltage at 0.82 V. The common mode voltage is tristated when you disable the OCT to use external termination.
- Offset cancellation—corrects the analog offset voltages that might exist from process variations between the positive and negative differential signals in the equalizer stage and CDR circuit.
- Signal detection—detects if the signal level present at the receiver input buffer is higher than the threshold with a built-in signal threshold detection circuitry. The circuitry has a hysteresis response that filters out any high-frequency ringing caused by ISI effects or high-frequency losses in the transmission medium. Detection is indicated by the assertion of the rx_signaldetect signal. Signal detection is only supported when 8B/10B encoder/decoder block is enabled. When not supported, the rx_signaldetect signal is forced high, bypassing the signal detection function.
- Disable OCT to use external termination if the link requires a 85 Ω termination, such as when you are interfacing with certain PCIe Gen1 or Gen2 capable devices.
 - For specifications on programmable equalization and DC gain settings, refer to the *Cyclone IV Device Data Sheet*.

Receiver polarity inversion—corrects accidental swapped positive and negative signals from the serial differential link during board layout. This feature works by inverting the polarity of every bit of the input data word to the word aligner, which has the same effect as swapping the positive and negative signals of the differential link. Inversion is dynamically controlled using rx_invpolarity port. Figure 1–19 shows the receiver polarity inversion feature.

Figure 1–19. Receiver Polarity Inversion



The generic receiver polarity inversion feature is different from the PCI Express (PIPE) 8B/10B polarity inversion feature. The generic receiver polarity inversion feature inverts the polarity of the data bits at the input of the word aligner and is not available in PCI Express (PIPE) mode. The PCI Express (PIPE) 8B/10B polarity inversion feature inverts the polarity of the data bits at the input of the 8B/10B decoder and is available only in PCI Express (PIPE) mode.

The rx_invpolarity signal is dynamic and might cause initial disparity errors in an 8B/10B encoded link. The downstream system must be able to tolerate these disparity errors.

Receiver bit reversal—by default, the Cyclone IV GX receiver assumes LSB to MSB transmission. If the link transmission order is MSB to LSB, the receiver forwards the incorrect reverse bit-ordered version of the parallel data to the FPGA fabric on the rx_dataout port. The receiver bit reversal feature is available to correct this situation. This feature is static in manual alignment and automatic

Figure 1–27 shows an example of the termination scheme for AC-coupled connections for REFCLK pins.





Note to Figure 1-27:

(1) For more information about the V_{ICM} value, refer to the *Cyclone IV Device Datasheet* chapter.

Figure 1–28 shows an example termination scheme for the REFCLK pin when configured as a **HCSL** input.

Figure 1–28. Termination Scheme for a Reference Clock When Configured as HCSL⁽¹⁾



Notes to Figure 1-28:

- (1) No biasing is required if the reference clock signals are generated from a clock source that conforms to the PCIe specification.
- (2) Select values as recommended by the PCIe clock source vendor.

Transceiver Channel Datapath Clocking

Channel datapath clocking varies with channel configuration options and PCS configurations. This section describes the clock distribution from the left PLLs for transceiver channels and the datapath clocking in various supported configurations.

Table 1–7 lists the clocks generated by the PLLs for transceiver datapath.

 Table 1–7.
 PLL Clocks for Transceiver Datapath

Clock	Usage
CDR clocks	Receiver CDR unit
High-speed clock	Transmitter serializer block in PMA
Low-speed clock	Transmitter PCS blocks
	Receiver PCS blocks when rate match FIFO enabled

Serial loopback mode can only be dynamically enabled or disabled during user mode by performing a dynamic channel reconfiguration.

Figure 1–71. Serial Loopback Path⁽¹⁾



Note to Figure 1–71:

(1) Grayed-Out Blocks are Not Active in this mode.

Reverse Serial Loopback

The reverse serial loopback mode is available for all functional modes except for XAUI mode. The two reverse serial loopback options from the receiver to the transmitter are:

- Pre-CDR mode where data received through the RX input buffer is looped back to the TX output buffer using the **Reverse serial loopback (pre-CDR)** option
- Post-CDR mode where retimed data through the receiver CDR from the RX input buffer is looped back to the TX output buffer using the Reverse serial loopback option

The received data is also available to the FPGA logic. In the transmitter channel, only the transmitter buffer is active.

- The transmitter pre-emphasis feature is not available in reverse serial loopback (pre-CDR) mode.
- Reverse serial loopback modes can only be dynamically enabled or disabled during user mode by performing a dynamic channel reconfiguration.

	Polynomial		8-bit Cha	nnel Width		10-bit Channel Width				
Patterns		Channel Width of 8 bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages	Channel Width of 10-bits (1)	Word Alignment Pattern	Maximum Data Rate (Gbps) for F324 and Smaller Packages	Maximum Data Rate (Gbps) for F484 and Larger Packages	
Low Frequency ⁽²⁾	1111100000	Ν		_	_	Y		2.5	3.125	

Table 1-25	. PRBS, High and Lo	w Frequency Patterns	, and Channel Settings	(Part 2 of 2)
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Notes to Table 1-25:

(1) Channel width refers to the **What is the channel width?** option in the **General** screen of the ALTGX MegaWizard Plug-In Manager. Based on the selection, an 8 or 10 bits wide pattern is generated as indicated by a **Yes (Y)** or **No (N)**.

(2) A verifier and associated rx bistdone and rx bisterr signals are not available for the specified patterns.

You can enable the serial loopback option to loop the generated PRBS patterns to the receiver channel for verifier to check the PRBS patterns. When the PRBS pattern is received, the rx_bisterr and rx_bistdone signals indicate the status of the verifier. After the word aligner restores the word boundary, the rx_bistdone signal is driven high when the verifier receives a complete pattern cycle and remains asserted until it is reset using the rx_digitalreset port. After the assertion of rx_bistdone, the rx_bisterr signal is asserted for a minimum of three rx_clkout cycles when errors are detected in the data and deasserts if the following PRBS sequence contains no error. You can reset the PRBS pattern generator and verifier by asserting the tx_digitalreset and rx_digitalreset ports, respectively.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1–12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

Table 1–12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices (1)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R_PU		$V_{CC10} = 3.3 \text{ V} \pm 5\%$ (2), (3)	7	25	41	kΩ
	Value of the I/O nin pull-up resistor	$V_{CC10} = 3.0 \text{ V} \pm 5\%$ (2), (3)	7	28	47	kΩ
	before and during configuration, as well as user mode if you enable the programmable pull-up resistor option	$V_{CCIO} = 2.5 \text{ V} \pm 5\%$ (2), (3)	8	35	61	kΩ
		$V_{CCIO} = 1.8 \text{ V} \pm 5\%$ (2), (3)	10	57	108	kΩ
		$V_{CCIO} = 1.5 \text{ V} \pm 5\%$ (2), (3)	13	82	163	kΩ
		$V_{CCIO} = 1.2 \text{ V} \pm 5\%$ (2), (3)	19	143	351	kΩ
R_pd		$V_{CCIO} = 3.3 \text{ V} \pm 5\%$ (4)	6	19	30	kΩ
	Value of the I/O pin pull-down resistor	$V_{CCIO} = 3.0 \text{ V} \pm 5\%$ (4)	6	22	36	kΩ
		$V_{CCIO} = 2.5 \text{ V} \pm 5\%$ (4)	6	25	43	kΩ
	soloro and daming borngulation	$V_{CCIO} = 1.8 \text{ V} \pm 5\%$ (4)	7	35	71	kΩ
		$V_{CCIO} = 1.5 \text{ V} \pm 5\%$ (4)	8	50	112	kΩ

Notes to Table 1-12:

- (1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .
- (3) $R_{PU} = (V_{CCIO} V_I)/I_{R_PU}$ Minimum condition: -40°C; $V_{CCIO} = V_{CC} + 5\%$, $V_I = V_{CC} + 5\% - 50$ mV; Typical condition: 25°C; $V_{CCIO} = V_{CC}$, $V_I = 0$ V; Maximum condition: 100°C; $V_{CCIO} = V_{CC} - 5\%$, $V_I = 0$ V; in which V_I refers to the input voltage at the I/O pin.
- $\begin{array}{ll} (4) & R_{_PD} = V_I/I_{R_PD} \\ & \text{Minimum condition:} -40^{\circ}\text{C}; \ V_{CCIO} = V_{CC} + 5\%, \ V_I = 50 \ \text{mV}; \\ & \text{Typical condition:} \ 25^{\circ}\text{C}; \ V_{CCIO} = V_{CC}, \ V_I = V_{CC} 5\%; \\ & \text{Maximum condition:} \ 100^{\circ}\text{C}; \ V_{CCIO} = V_{CC} 5\%, \ V_I = V_{CC} 5\%; \ \text{in which } V_I \ \text{refers to the input voltage at the I/O pin.} \end{array}$

Hot-Socketing

Table 1–13 lists the hot-socketing specifications for Cyclone IV devices.

Table 1–13. Hot-Socketing Specifications for Cyclone IV Devices

Symbol	Parameter	Maximum
I _{IOPIN(DC)}	DC current per I/O pin	300 μA
I _{IOPIN(AC)}	AC current per I/O pin	8 mA <i>(1)</i>
I _{XCVRTX(DC)}	DC current per transceiver TX pin	100 mA
I _{XCVRRX(DC)}	DC current per transceiver RX pin	50 mA

Note to Table 1-13:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

I/N Standard	V _{CCIO} (V)			V _{ID} (mV) V _{IC}			V _{IcM} (V) ⁽²⁾	(V) ⁽²⁾ V ₀₀		V _{0D} (mV) ⁽³⁾		V _{0S} (V) ⁽³⁾		
i/U Stanuaru	Min	Тур	Max	Min	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
						0.05	$D_{MAX} \leq ~500~Mbps$	1.80						
(Column	2.375	2.5	2.625	100	_	0.55	$\begin{array}{l} 500 \text{ Mbps} \leq \text{D}_{\text{MAX}} \\ \leq \ 700 \text{ Mbps} \end{array}$	1.80	247	_	600	1.125	1.25	1.375
1,00)						1.05	D _{MAX} > 700 Mbps	1.55						
BLVDS (Row I/Os) ⁽⁴⁾	2.375	2.5	2.625	100	_	_	_	_	_	_	_	_	_	_
BLVDS (Column I/Os) <i>(4)</i>	2.375	2.5	2.625	100			_			_		_		
mini-LVDS (Row I/Os) <i>(5)</i>	2.375	2.5	2.625		_	_	_		300	_	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) ⁽⁵⁾	2.375	2.5	2.625				_		300		600	1.0	1.2	1.4
RSDS®(Row I/Os) ⁽⁵⁾	2.375	2.5	2.625	_	_			_	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) ⁽⁵⁾	2.375	2.5	2.625				_		100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) <i>(5</i>)	2.375	2.5	2.625	_	_			_	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) ⁽⁵⁾	2.375	2.5	2.625	_	_		_		100	200	600	0.5	1.2	1.4

	Table 1-20.	Differential I/O Standard S	pecifications for C	yclone IV Devices ⁽¹⁾	(Part 2 of 2
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Notes to Table 1-20:

(1) For an explanation of terms used in Table 1–20, refer to "Glossary" on page 1–37.

(2) $~V_{IN}$ range: 0 V $\leq V_{IN} \leq$ 1.85 V.

(3) $R_L \mbox{ range: } 90 \leq \ R_L \leq \ 110 \ \Omega$.

(4) There are no fixed $V_{\rm IN},\,V_{\rm OD},$ and $V_{\rm OS}$ specifications for BLVDS. They depend on the system topology.

(5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.

(6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.