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## What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "**Embedded - Microcontrollers**"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 12x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN-S (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep16gs502t-e-mm |

**FIGURE 2-5:** PHASE-SHIFTED FULL-BRIDGE CONVERTER
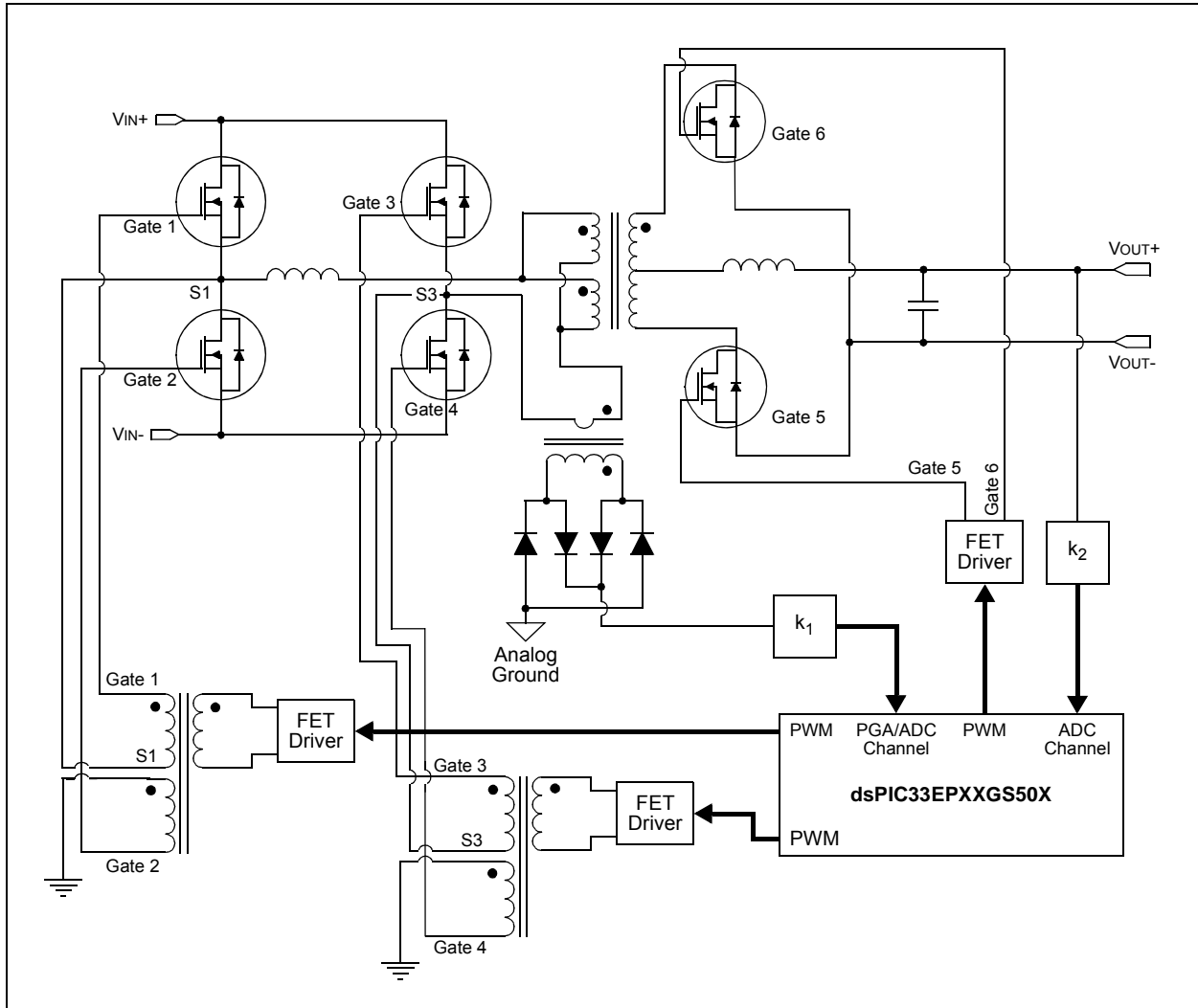
**REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)**

bit 2　　　　**SFA:** Stack Frame Active Status bit

　　　　　　1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG
　　　　　　0 = Stack frame is not active; W14 and W15 address the base Data Space

bit 1　　　　**RND:** Rounding Mode Select bit

　　　　　　1 = Biased (conventional) rounding is enabled
　　　　　　0 = Unbiased (convergent) rounding is enabled

bit 0　　　　**IF:** Integer or Fractional Multiplier Mode Select bit

　　　　　　1 = Integer mode is enabled for DSP multiply
　　　　　　0 = Fractional mode is enabled for DSP multiply

**Note 1:** This bit is always read as '0'.
　　　**2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

**REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| — | — | — | — | — | CCTXI2 | CCTXI1 | CCTXI0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| — | — | — | — | — | MCTXI2 | MCTXI1 | MCTXI0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared　　　x = Bit is unknown |

bit 15-11　　**Unimplemented:** Read as '0'

bit 10-8　　**CCTXI<2:0>:** Current (W Register) Context Identifier bits

　　　　　　111 = Reserved
　　　　　　•
　　　　　　•
　　　　　　•
　　　　　　011 = Reserved
　　　　　　010 = Alternate Working Register Set 2 is currently in use
　　　　　　001 = Alternate Working Register Set 1 is currently in use
　　　　　　000 = Default register set is currently in use

bit 7-3　　　**Unimplemented:** Read as '0'

bit 2-0　　　**MCTXI<2:0>:** Manual (W Register) Context Identifier bits

　　　　　　111 = Reserved
　　　　　　•
　　　　　　•
　　　　　　•
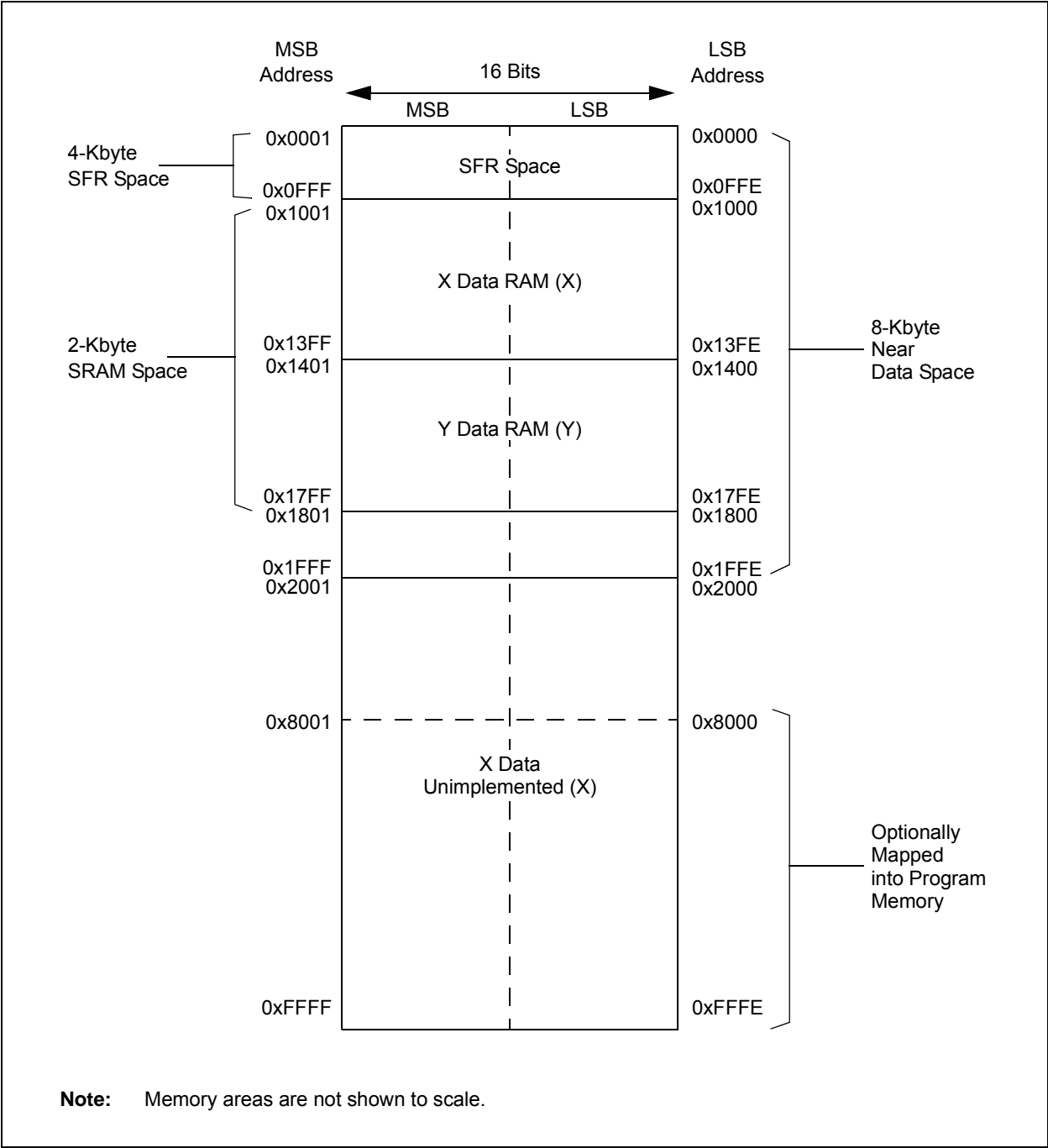　　　　　　011 = Reserved
　　　　　　010 = Alternate Working Register Set 2 was most recently manually selected
　　　　　　001 = Alternate Working Register Set 1 was most recently manually selected
　　　　　　000 = Default register set was most recently manually selected

**FIGURE 4-6:     DATA MEMORY MAP FOR dsPIC33EP16GS50X DEVICES**



Note:     Memory areas are not shown to scale.

When a PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses the PSV page
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSRPAG register is incremented and the EA<15> bit is set to keep the base address within the PSV window. When an underflow is detected, the DSRPAG register is decremented and the EA<15> bit is set to keep the base

address within the PSV window. This creates a linear PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0 and PSV spaces. Table 4-37 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSRPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

**TABLE 4-37: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0 AND PSV SPACE BOUNDARIES[2,3,4]**

| O/U, R/W | Operation | Before | | | After | | |
|---|---|---|---|---|---|---|---|
| | | DSxPAG | DS EA<15> | Page Description | DSxPAG | DS EA<15> | Page Description |
| O, Read | `[++Wn]` or `[Wn++]` | DSRPAG = 0x2FF | 1 | PSV: Last lsw page | DSRPAG = 0x300 | 1 | PSV: First MSB page |
| O, Read | | DSRPAG = 0x3FF | 1 | PSV: Last MSB page | DSRPAG = 0x3FF | 0 | See **Note 1** |
| U, Read | `[--Wn]` or `[Wn--]` | DSRPAG = 0x001 | 1 | PSV page | DSRPAG = 0x001 | 0 | See **Note 1** |
| U, Read | | DSRPAG = 0x200 | 1 | PSV: First lsw page | DSRPAG = 0x200 | 0 | See **Note 1** |
| U, Read | | DSRPAG = 0x300 | 1 | PSV: First MSB page | DSRPAG = 0x2FF | 1 | PSV: Last lsw page |

**Legend:** O = Overflow, U = Underflow, R = Read, W = Write

**Note 1:** The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x7FFF).

**2:** An EDS access, with DSRPAG = 0x000, will generate an address error trap.

**3:** Only reads from PS are supported using DSRPAG.

**4:** Pseudolinear Addressing is not supported for large offsets.

## 5.6 Control Registers

Five SFRs are used to write and erase the program Flash memory: NVMCON, NVMKEY, NVMADR, NVMADRU and NVMSRCADR/H.

The NVMCON register (Register 5-1) selects the operation to be performed (page erase, word/row program, Inactive Partition erase), initiates the program or erase cycle and is used to determine the Active Partition in Dual Partition modes.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word/row for programming operations, or the selected page for erase operations. The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

For row programming operation, data to be written to program Flash memory is written into data memory space (RAM) at an address defined by the NVMSRCADR register (location of first element in row programming data).

**REGISTER 7-2: CORCON: CORE CONTROL REGISTER[1]**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
|-------|-----|-------|-------|-------|-----|-----|-----|
| VAR | — | US1 | US0 | EDT | DL2 | DL1 | DL0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-----|-------|-------|
| SATA | SATB | SATDW | ACCSAT | IPL3[2] | SFA | RND | IF |
| bit 7 | | | | | | | bit 0 |

| Legend: | | C = Clearable bit | |
|---------|---|----|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1'= Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15     **VAR:** Variable Exception Processing Latency Control bit

        1 = Variable exception processing is enabled
        0 = Fixed exception processing is enabled

bit 3     **IPL3:** CPU Interrupt Priority Level Status bit 3[2]

        1 = CPU Interrupt Priority Level is greater than 7
        0 = CPU Interrupt Priority Level is 7 or less

**Note 1:** For complete register details, see Register 3-2.

    **2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

## 15.0   HIGH-SPEED PWM

> **Note:** This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Speed PWM Module"** (DS70000323) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The high-speed PWM module on dsPIC33EPXXGS50X devices supports a wide variety of PWM modes and output formats. This PWM module is ideal for power conversion applications, such as:

- AC/DC Converters
- DC/DC Converters
- Power Factor Correction
- Uninterruptible Power Supply (UPS)
- Inverters
- Battery Chargers
- Digital Lighting

### 15.1   Features Overview

The high-speed PWM module incorporates the following features:

- Five PWMx Generators with Two Outputs per Generator
- Two Master Time Base Modules
- Individual Time Base and Duty Cycle for Each PWM Output
- Duty Cycle, Dead Time, Phase Shift and a Frequency Resolution of 1.04 ns
- Independent Fault and Current-Limit Inputs
- Redundant Output
- True Independent Output
- Center-Aligned PWM mode
- Output Override Control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Dual Trigger from PWMx to Analog-to-Digital Converter (ADC)
- PWMxL and PWMxH Output Pin Swapping
- Independent PWMx Frequency, Duty Cycle and Phase-Shift Changes
- Enhanced Leading-Edge Blanking (LEB) Functionality
- PWM Capture Functionality

> **Note:** Duty cycle, dead time, phase shift and frequency resolution is 8.32 ns in Center-Aligned PWM mode.

Figure 15-1 conceptualizes the PWM module in a simplified block diagram. Figure 15-2 illustrates how the module hardware is partitioned for each PWMx output pair for the Complementary PWM mode.

The PWM module contains five PWM generators. The module has up to 10 PWMx output pins: PWM1H/PWM1L through PWM5H/PWM5L. For complementary outputs, these 10 I/O pins are grouped into high/low pairs.

### 15.2   Feature Description

The PWM module is designed for applications that require:

- High resolution at high PWM frequencies
- The ability to drive Standard, Edge-Aligned, Center-Aligned Complementary mode and Push-Pull mode outputs
- The ability to create multiphase PWM outputs

Two common, medium power converter topologies are push-pull and half-bridge. These designs require the PWM output signal to be switched between alternate pins, as provided by the Push-Pull PWM mode.

Phase-shifted PWM describes the situation where each PWM generator provides outputs, but the phase relationship between the generator outputs is specifiable and changeable.

Multiphase PWM is often used to improve DC/DC converter load transient response, and reduce the size of output filter capacitors and inductors. Multiple DC/DC converters are often operated in parallel, but phase shifted in time. A single PWM output, operating at 250 kHz, has a period of 4 μs but an array of four PWM channels, staggered by 1 μs each, yields an effective switching frequency of 1 MHz. Multiphase PWM applications typically use a fixed-phase relationship.

Variable phase PWM is useful in Zero Voltage Transition (ZVT) power converters. Here, the PWM duty cycle is always 50% and the power flow is controlled by varying the relative phase shift between the two PWM generators.

**REGISTER 15-17: DTRx: PWMx DEAD-TIME REGISTER (x = 1 to 5)**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-------|-------|-------|-------|-------|-------|
| — | — | DTRx<13:8> | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DTRx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

**REGISTER 15-18: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER (x = 1 to 5)**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-------|-------|-------|-------|-------|-------|
| — | — | ALTDTRx<13:8> | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ALTDTRx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

### REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-----|-------|-------|-------|-------|-------|
| — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE[1] |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SSEN[2] | CKP | MSTEN | SPRE2[3] | SPRE1[3] | SPRE0[3] | PPRE1[3] | PPRE0[3] |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCKx Pin bit (SPIx Master modes only)

1 = Internal SPIx clock is disabled, pin functions as I/O
0 = Internal SPIx clock is enabled

bit 11 **DISSDO:** Disable SDOx Pin bit

1 = SDOx pin is not used by the module; pin functions as I/O
0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit

1 = Communication is word-wide (16 bits)
0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit

Master Mode:
1 = Input data is sampled at the end of data output time
0 = Input data is sampled at the middle of data output time

Slave Mode:
SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** SPIx Clock Edge Select bit[1]

1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)
0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)[2]

1 = $\overline{SS}$x pin is used for Slave mode
0 = $\overline{SS}$x pin is not used by the module; pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit

1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit

1 = Master mode
0 = Slave mode

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
2: This bit must be cleared when FRMEN = 1.
3: Do not set both primary and secondary prescalers to the value of 1:1.

**REGISTER 19-29: ADCAL0H: ADC CALIBRATION REGISTER 0 HIGH**

| R-0, HSC | U-0 | U-0 | U-0 | r-0 | R/W-0 | R/W-0 | R/W-0 |
|----------|-----|-----|-----|-----|-------|-------|-------|
| CAL3RDY | — | — | — | — | CAL3DIFF | CAL3EN | CAL3RUN |
| bit 15 | | | | | | | bit 8 |

| R-0, HSC | U-0 | U-0 | U-0 | r-0 | R/W-0 | R/W-0 | R/W-0 |
|----------|-----|-----|-----|-----|-------|-------|-------|
| CAL2RDY | — | — | — | — | CAL2DIFF | CAL2EN | CAL2RUN |
| bit 7 | | | | | | | bit 0 |

| Legend: | | r = Reserved bit | U = Unimplemented bit, read as '0' | |
|---------|---|------------------|-----------------------------------|---|
| R = Readable bit | | W = Writable bit | HSC = Hardware Settable/Clearable bit | |
| -n = Value at POR | | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CAL3RDY:** Dedicated ADC Core 3 Calibration Status Flag bit
1 = Dedicated ADC Core 3 calibration is finished
0 = Dedicated ADC Core 3 calibration is in progress

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **Reserved:** Must be written as '0'

bit 10 **CAL3DIFF:** Dedicated ADC Core 3 Differential-Mode Calibration bit
1 = Dedicated ADC Core 3 will be calibrated in Differential Input mode
0 = Dedicated ADC Core 3 will be calibrated in Single-Ended Input mode

bit 9 **CAL3EN:** Dedicated ADC Core 3 Calibration Enable bit
1 = Dedicated ADC Core 3 calibration bits (CALxRDY, CALxDIFF and CALxRUN) can be accessed by software
0 = Dedicated ADC Core 3 calibration bits are disabled

bit 8 **CAL3RUN:** Dedicated ADC Core 3 Calibration Start bit
1 = If this bit is set by software, the dedicated ADC Core 3 calibration cycle is started; this bit is automatically cleared by hardware
0 = Software can start the next calibration cycle

bit 7 **CAL2RDY:** Dedicated ADC Core 2 Calibration Status Flag bit
1 = Dedicated ADC Core 2 calibration is finished
0 = Dedicated ADC Core 2 calibration is in progress

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **Reserved:** Must be written as '0'

bit 2 **CAL2DIFF:** Dedicated ADC Core 2 Differential-Mode Calibration bit
1 = Dedicated ADC Core 2 will be calibrated in Differential Input mode
0 = Dedicated ADC Core 2 will be calibrated in Single-Ended Input mode

bit 1 **CAL2EN:** Dedicated ADC Core 2 Calibration Enable bit
1 = Dedicated ADC Core 2 calibration bits (CALxRDY, CALxDIFF and CALxRUN) can be accessed by software
0 = Dedicated ADC Core 2 calibration bits are disabled

bit 0 **CAL2RUN:** Dedicated ADC Core 2 Calibration Start bit
1 = If this bit is set by software, the dedicated ADC Core 2 calibration cycle is started; this bit is automatically cleared by hardware
0 = Software can start the next calibration cycle

## REGISTER 19-34: ADFLxCON: ADC DIGITAL FILTER x CONTROL REGISTER (x = 0 or 1)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0, HSC |
|-------|-------|-------|-------|-------|-------|-------|----------|
| FLEN | MODE1 | MODE0 | OVRSAM2 | OVRSAM1 | OVRSAM0 | IE | RDY |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-----|-------|-------|-------|-------|-------|
| — | — | — | FLCHSEL4 | FLCHSEL3 | FLCHSEL2 | FLCHSEL1 | FLCHSEL0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| | U = Unimplemented bit, read as '0' | | |
| R = Readable bit | W = Writable bit | HSC = Hardware Settable/Clearable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLEN:** Filter Enable bit

1 = Filter is enabled
0 = Filter is disabled and the RDY bit is cleared

bit 14-13 **MODE<1:0>:** Filter Mode bits

11 = Averaging mode
10 = Reserved
01 = Reserved
00 = Oversampling mode

bit 12-10 **OVRSAM<2:0>:** Filter Averaging/Oversampling Ratio bits

If MODE<1:0> = 00:
111 = 128x (16-bit result in the ADFLxDAT register is in 12.4 format)
110 = 32x (15-bit result in the ADFLxDAT register is in 12.3 format)
101 = 8x (14-bit result in the ADFLxDAT register is in 12.2 format)
100 = 2x (13-bit result in the ADFLxDAT register is in 12.1 format)
011 = 256x (16-bit result in the ADFLxDAT register is in 12.4 format)
010 = 64x (15-bit result in the ADFLxDAT register is in 12.3 format)
001 = 16x (14-bit result in the ADFLxDAT register is in 12.2 format)
000 = 4x (13-bit result in the ADFLxDAT register is in 12.1 format)
If MODE<1:0> = 11 (12-bit result in the ADFLxDAT register in all instances):
111 = 256x
110 = 128x
101 = 64x
100 = 32x
011 = 16x
010 = 8x
001 = 4x
000 = 2x

bit 9 **IE:** Filter Common ADC Interrupt Enable bit

1 = Common ADC interrupt will be generated when the filter result will be ready
0 = Common ADC interrupt will not be generated for the filter

bit 8 **RDY:** Oversampling Filter Data Ready Flag bit

This bit is cleared by hardware when the result is read from the ADFLxDAT register.
1 = Data in the ADFLxDAT register is ready
0 = The ADFLxDAT register has been read and new data in the ADFLxDAT register is not ready

bit 7-5 **Unimplemented:** Read as '0'

# TABLE 23-1: CONFIGURATION REGISTER MAP[3]

| Name | Address | Device Memory Size (Kbytes) | Bits 23-16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FSEC | 002B80 | 16 | — | AIVTDIS | — | — | — | CSS<2:0> | | | CWRP | GSS<1:0> | | GWRP | — | BSEN | BSS<1:0> | | BWRP |
| | 005780 | 32 | | | | | | | | | | | | | | | | | |
| | 00AF80 | 64 | | | | | | | | | | | | | | | | | |
| FBSLIM | 002B90 | 16 | — | — | — | — | BSLIM<12:0> | | | | | | | | | | | | |
| | 005790 | 32 | | | | | | | | | | | | | | | | | |
| | 00AF90 | 64 | | | | | | | | | | | | | | | | | |
| FSIGN | 002B94 | 16 | — | Reserved[2] | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | 005794 | 32 | | | | | | | | | | | | | | | | | |
| | 00AF94 | 64 | | | | | | | | | | | | | | | | | |
| FOSCSEL | 002B98 | 16 | — | — | — | — | — | — | — | — | — | IESO | — | — | — | — | FNOSC<2:0> | | |
| | 005798 | 32 | | | | | | | | | | | | | | | | | |
| | 00AF98 | 64 | | | | | | | | | | | | | | | | | |
| FOSC | 002B9C | 16 | — | — | — | — | — | — | — | — | PLLKEN | FCKSM<1:0> | | IOL1WAY | — | — | OSCIOFNC | POSCMD<1:0> | |
| | 00579C | 32 | | | | | | | | | | | | | | | | | |
| | 00AF9C | 64 | | | | | | | | | | | | | | | | | |
| FWDT | 002BA0 | 16 | — | — | — | — | — | — | — | WDTWIN<1:0> | | WINDIS | WDTEN<1:0> | | WDTPRE | WDTPOST<3:0> | | | |
| | 0057A0 | 32 | | | | | | | | | | | | | | | | | |
| | 00AFA0 | 64 | | | | | | | | | | | | | | | | | |
| FPOR | 002BA4 | 16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | Reserved[1] |
| | 0057A4 | 32 | | | | | | | | | | | | | | | | | |
| | 00AFA4 | 64 | | | | | | | | | | | | | | | | | |
| FICD | 002BA8 | 16 | — | BTSWP | — | — | — | — | — | — | — | Reserved[1] | — | JTAGEN | — | — | — | ICS<1:0> | |
| | 0057A8 | 32 | | | | | | | | | | | | | | | | | |
| | 00AFA8 | 64 | | | | | | | | | | | | | | | | | |

**Note 1:** These bits are reserved and must be programmed as '1'.
    **2:** This bit is reserved and must be programmed as '0'.
    **3:** When operating in Dual Partition mode, each partition will have dedicated Configuration registers. On a device Reset, the configuration values of the Active Partition are read at start-up, but during a soft swap condition, the configuration settings of the newly Active Partition are ignored.
    **4:** FBOOT resides in configuration memory space.

## 23.2 Device Calibration and Identification

The PGAx and current source modules on the dsPIC33EPXXGS50X family devices require Calibration Data registers to improve performance of the module over a wide operating range. These Calibration registers are read-only and are stored in configuration memory space. Prior to enabling the module, the calibration data must be read (TBLPAG and Table Read instruction) and loaded into its respective SFR registers. The device calibration addresses are shown in Table 23-3.

The dsPIC33EPXXGS50X devices have two identification registers near the end of configuration memory space that store the Device ID (DEVID) and Device Revision (DEVREV). These registers are used to determine the mask, variant and manufacturing information about the device. These registers are read-only and are shown in Register 23-1 and Register 23-2.

**TABLE 23-3: DEVICE CALIBRATION ADDRESSES[1]**

| Calibration Name | Address | Bits 23-16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PGA1CAL | 800E48 | — | — | — | — | — | — | — | — | — | — | — | PGA1 Calibration Data | | | | | |
| PGA2CAL | 800E4C | — | — | — | — | — | — | — | — | — | — | — | PGA2 Calibration Data | | | | | |
| ISRCCAL | 800E78 | — | — | — | — | — | — | — | — | — | — | — | Current Source Calibration Data | | | | | |

**Note 1:** The calibration data must be copied into its respective registers prior to enabling the module.

## 23.3 User OTP Memory

dsPIC33EPXXGS50X family devices contain 64 words of User One-Time-Programmable (OTP) memory, located at addresses, 0x800F80 through 0x800FFE. The User OTP Words can be used for storing checksum, code revisions, product information, such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information. These words can only be written once at program time and not at run time; they can be read at run time.

## 23.4 On-Chip Voltage Regulator

All the dsPIC33EPXXGS50X family devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXGS50X family incorporate an on-chip regulator that allows the device to run its core logic from $V_{DD}$.

The regulator provides power to the core from the other $V_{DD}$ pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the $V_{CAP}$ pin (Figure 23-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 26-5, located in **Section 26.0 "Electrical Characteristics"**.

| Note: | It is important for the low-ESR capacitor to be placed as close as possible to the $V_{CAP}$ pin. |
|---|---|

**FIGURE 23-1:** **CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR[1,2,3]**



Note 1: These are typical operating voltages. Refer to Table 26-5 located in **Section 26.0 "Electrical Characteristics"** for the full operating ranges of $V_{DD}$ and $V_{CAP}$.

2: It is important for the low-ESR capacitor to be placed as close as possible to the $V_{CAP}$ pin.

3: Typical $V_{CAP}$ pin voltage = 1.8V when $V_{DD} \geq V_{DDMIN}$.

## 23.5 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, $V_{CAP}$. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse which resets the device. The BOR selects the clock source based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an Oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out ($T_{PWRT}$) is applied before the internal Reset is released. If $T_{PWRT} = 0$ and a crystal oscillator is being used, then a nominal delay of $T_{FSCM}$ is applied. The total delay in this case is $T_{FSCM}$. Refer to Parameter SY35 in Table 26-23 of **Section 26.0 "Electrical Characteristics"** for specific $T_{FSCM}$ values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should $V_{DD}$ fall below the BOR threshold voltage.
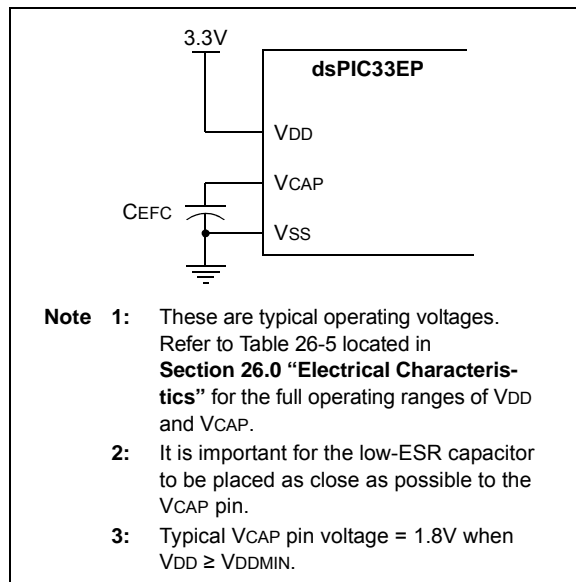
Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction, or a PSV or table read is performed. In these cases, the execution takes multiple instruction cycles,

with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

> **Note:** For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

### TABLE 24-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

| Field | Description |
|---|---|
| #text | Means literal defined by "text" |
| (text) | Means "content of text" |
| [text] | Means "the location addressed by text" |
| { } | Optional field or operation |
| a ∈ {b, c, d} | a is selected from the set of values b, c, d |
| <n:m> | Register bit field |
| .b | Byte mode selection |
| .d | Double-Word mode selection |
| .S | Shadow register select |
| .w | Word mode selection (default) |
| Acc | One of two accumulators {A, B} |
| AWB | Accumulator write-back destination address register ∈ {W13, [W13]+ = 2} |
| bit4 | 4-bit bit selection field (used in word addressed instructions) ∈ {0...15} |
| C, DC, N, OV, Z | MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero |
| Expr | Absolute address, label or expression (resolved by the linker) |
| f | File register address ∈ {0x0000...0x1FFF} |
| lit1 | 1-bit unsigned literal ∈ {0,1} |
| lit4 | 4-bit unsigned literal ∈ {0...15} |
| lit5 | 5-bit unsigned literal ∈ {0...31} |
| lit8 | 8-bit unsigned literal ∈ {0...255} |
| lit10 | 10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode |
| lit14 | 14-bit unsigned literal ∈ {0...16384} |
| lit16 | 16-bit unsigned literal ∈ {0...65535} |
| lit23 | 23-bit unsigned literal ∈ {0...8388608}; LSb must be '0' |
| None | Field does not require an entry, can be blank |
| OA, OB, SA, SB | DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate |
| PC | Program Counter |
| Slit10 | 10-bit signed literal ∈ {-512...511} |
| Slit16 | 16-bit signed literal ∈ {-32768...32767} |
| Slit6 | 6-bit signed literal ∈ {-16...16} |
| Wb | Base W register ∈ {W0...W15} |
| Wd | Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] } |
| Wdo | Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] } |
| Wm,Wn | Dividend, Divisor Working register pair (direct addressing) |

## 26.1 DC Characteristics

### TABLE 26-1: OPERATING MIPS vs. VOLTAGE

| Characteristic | VDD Range (in Volts) | Temperature Range (in °C) | Maximum MIPS |
|---|---|---|---|
| | | | dsPIC33EPXXGS50X Family |
| — | 3.0V to 3.6V[(1)] | -40°C to +85°C | 70 |
| — | 3.0V to 3.6V[(1)] | -40°C to +125°C | 60 |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, PGAs and comparators) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 26-13 for the minimum and maximum BOR values.

### TABLE 26-2: THERMAL OPERATING CONDITIONS

| Rating | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Industrial Temperature Devices | | | | | |
| Operating Junction Temperature Range | $T_J$ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | $T_A$ | -40 | — | +85 | °C |
| Extended Temperature Devices | | | | | |
| Operating Junction Temperature Range | $T_J$ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | $T_A$ | -40 | — | +125 | °C |
| Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$ | $P_D$ | $P_{INT} + P_{I/O}$ | | | W |
| Maximum Allowed Power Dissipation | $P_{DMAX}$ | $(T_J - T_A)/\theta_{JA}$ | | | W |

### TABLE 26-3: THERMAL PACKAGING CHARACTERISTICS

| Characteristic | Symbol | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 64-Pin TQFP 10x10x1 mm | $\theta_{JA}$ | 49.0 | — | °C/W | **1** |
| Package Thermal Resistance, 48-Pin TQFP 7x7x1.0 mm | $\theta_{JA}$ | 63.0 | — | °C/W | **1** |
| Package Thermal Resistance, 44-Pin QFN 8x8 mm | $\theta_{JA}$ | 29.0 | — | °C/W | **1** |
| Package Thermal Resistance, 44-Pin TQFP 10x10x1 mm | $\theta_{JA}$ | 50.0 | — | °C/W | **1** |
| Package Thermal Resistance, 28-Pin QFN-S 6x6x0.9 mm | $\theta_{JA}$ | 30.0 | — | °C/W | **1** |
| Package Thermal Resistance, 28-Pin UQFN 6x6x0.5 mm | $\theta_{JA}$ | 26.0 | — | °C/W | **1** |
| Package Thermal Resistance, 28-Pin SOIC 7.50 mm | $\theta_{JA}$ | 70.0 | — | °C/W | **1** |

**Note 1:** Junction to ambient thermal resistance, Theta-JA ($\theta_{JA}$) numbers are achieved by package simulations.

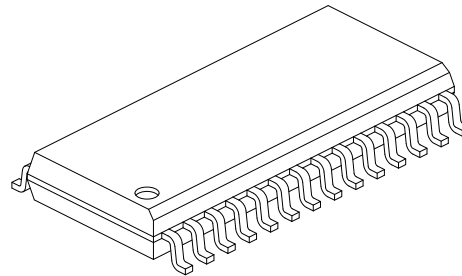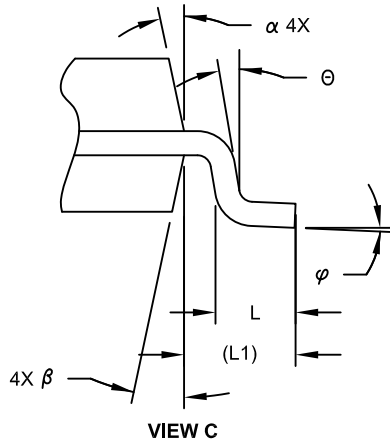**FIGURE 26-16: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**
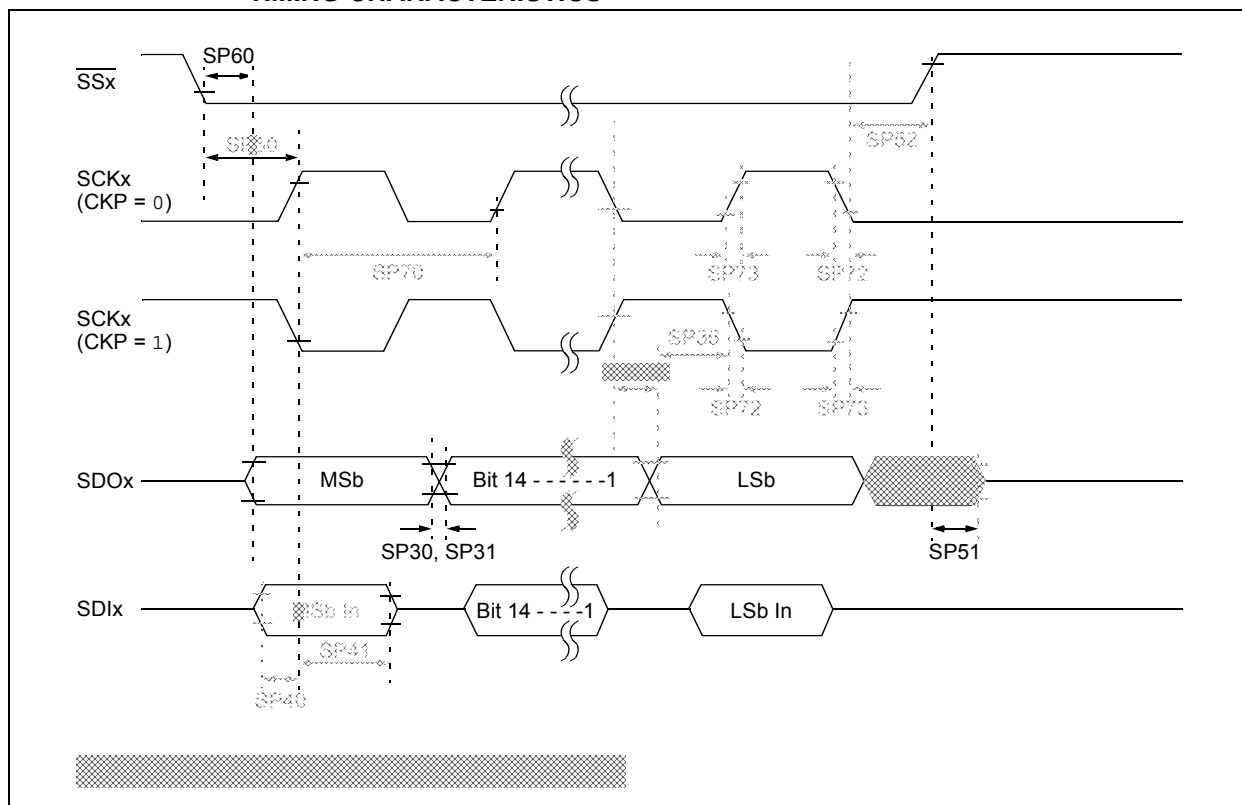
## 28-Lead Plastic Small Outline (SO) - Wide,  7.50 mm Body  [SOIC]

| Note: | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|

**VIEW C**

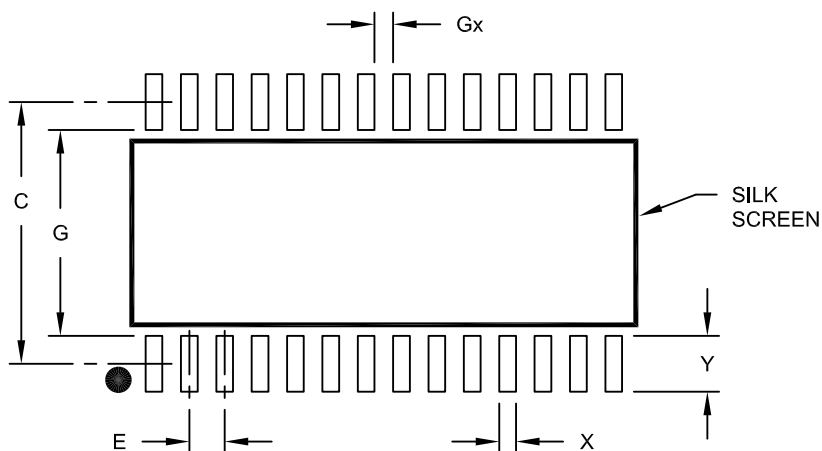|  | Units | | MILLIMETERS | | |
|---|---|---|---|---|---|
|  | Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | | 28 | |
| Pitch | e | | | 1.27 BSC | |
| Overall Height | A | | - | - | 2.65 |
| Molded Package Thickness | A2 | | 2.05 | - | - |
| Standoff § | A1 | | 0.10 | - | 0.30 |
| Overall Width | E | | | 10.30 BSC | |
| Molded Package Width | E1 | | | 7.50 BSC | |
| Overall Length | D | | | 17.90 BSC | |
| Chamfer (Optional) | h | | 0.25 | - | 0.75 |
| Foot Length | L | | 0.40 | - | 1.27 |
| Footprint | L1 | | | 1.40 REF | |
| Lead Angle | Θ | | 0° | - | - |
| Foot Angle | φ | | 0° | - | 8° |
| Lead Thickness | c | | 0.18 | - | 0.33 |
| Lead Width | b | | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | | 5° | - | 15° |
| Mold Draft Angle Bottom | β | | 5° | - | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end.  Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

    REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

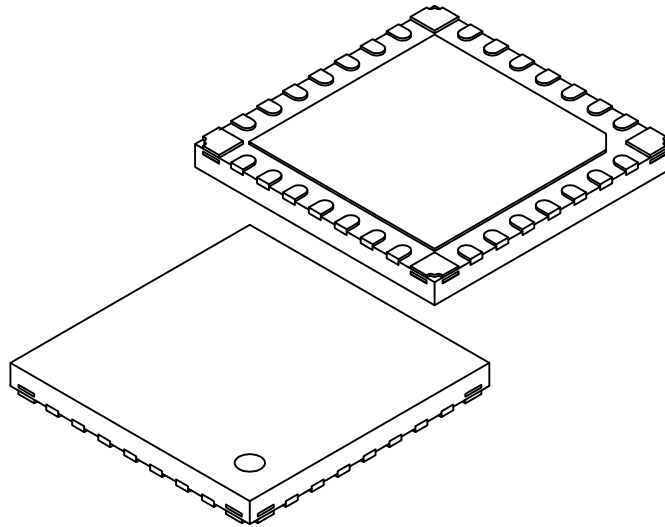| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 9.40 | |
| Contact Pad Width (X28) | X | | | 0.60 |
| Contact Pad Length (X28) | Y | | | 2.00 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 7.40 | | |

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

**28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (2N) - 6x6x0.55 mm Body [UQFN]
With 4.65x4.65 mm Exposed Pad and Corner Anchors**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|

| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.45 | 0.50 | 0.55 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.127 REF | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 4.55 | 4.65 | 4.75 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 4.55 | 4.65 | 4.75 |
| Exposed Pad Corner Chamfer | P | - | 0.35 | - |
| Terminal Width | b | 0.25 | 0.30 | 0.35 |
| Corner Anchor Pad | b1 | 0.35 | 0.40 | 0.43 |
| Corner Pad, Metal Free Zone | b2 | 0.15 | 0.20 | 0.25 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing  C04-385B Sheet 2 of 2