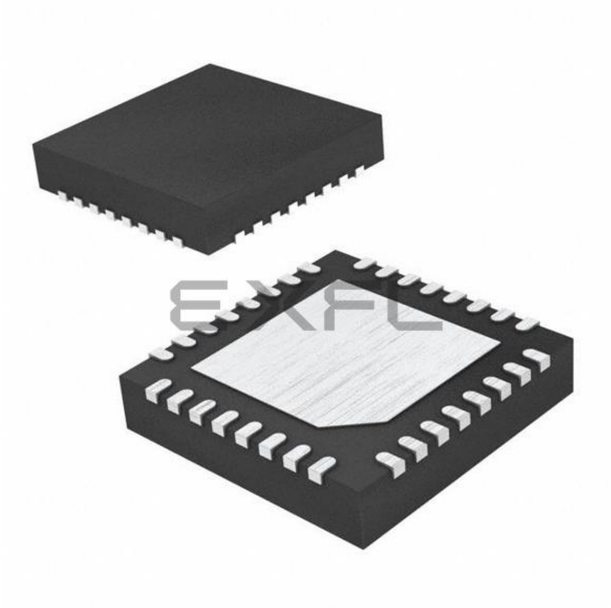

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UQFN Exposed Pad
Supplier Device Package	28-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep16gs502t-i-2n

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, MPLAB ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *“Using MPLAB® ICD 3”* (poster) DS51765
- *“Multi-Tool Design Advisory”* DS51764
- *“MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide”* DS51616
- *“Using MPLAB® REAL ICE™ In-Circuit Emulator”* (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For details, see **Section 8.0 “Oscillator Configuration”** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

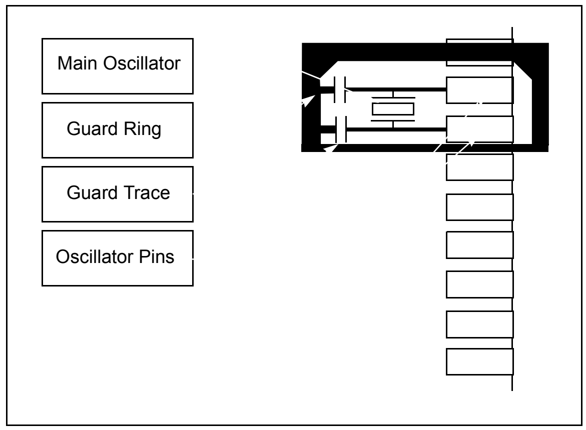
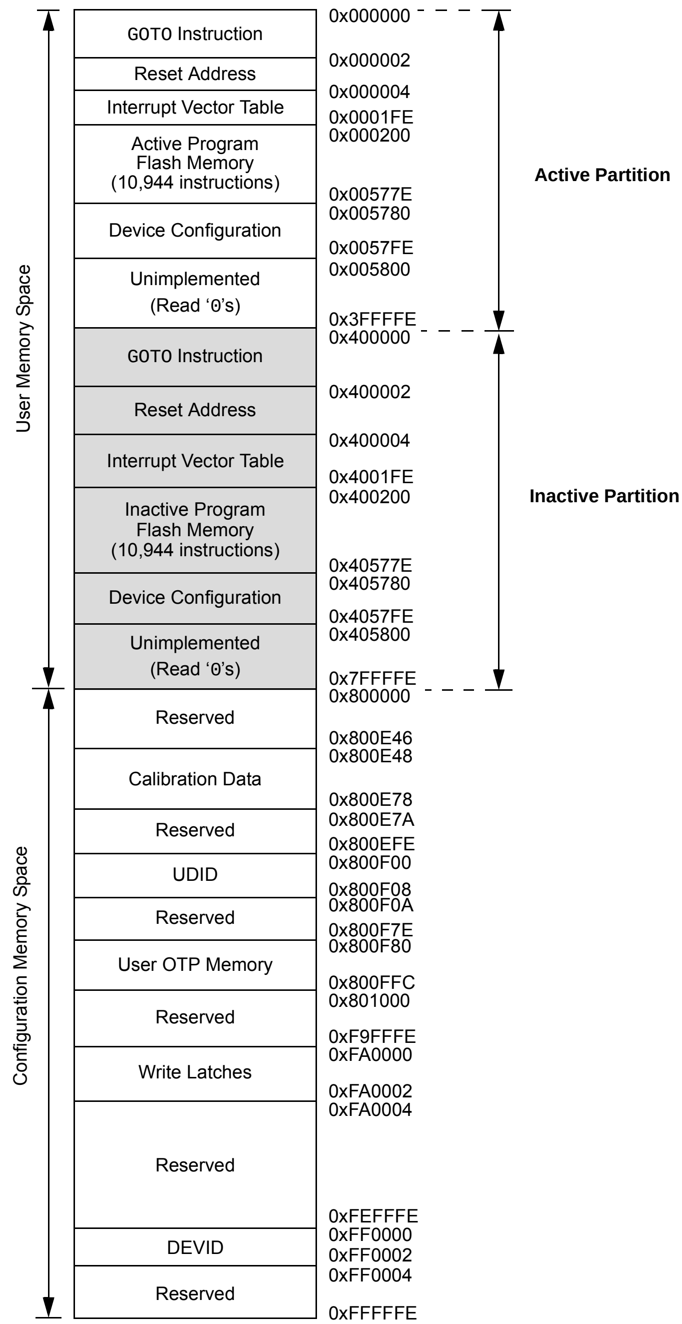


FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP64GS50X DEVICES (DUAL PARTITION)



Note: Memory areas are not shown to scale.

TABLE 4-16: ADC REGISTER MAP (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADLVLTRGL	03D0	LVLEN15[1]	LVLEN14	LVLEN13[1]	LVLEN12[2]	LVLEN11[2]	LVLEN10[2]	LVLEN9[2]	LVLEN8[2]	LVLEN7	LVLEN6	LVLEN5	LVLEN4	LVLEN3	LVLEN2	LVLEN1	LVLEN0	0000
ADLVLTRGH	03D2	—	—	—	—	—	—	—	—	—	—	LVLEN21	LVLEN20	LVLEN19	LVLEN18	LVLEN17[2]	LVLEN16[1]	0000
ADCORE0L	03D4	—	—	—	—	—	—	SAMC<9:0>										0000
ADCORE0H	03D6	—	—	—	EISEL2	EISEL1	EISEL0	RES1	RES0	—	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
ADCORE1L	03D8	—	—	—	—	—	—	SAMC<9:0>										0000
ADCORE1H	03DA	—	—	—	EISEL2	EISEL1	EISEL0	RES1	RES0	—	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
ADCORE2L	03DC	—	—	—	—	—	—	SAMC<9:0>										0000
ADCORE2H	03DE	—	—	—	EISEL2	EISEL1	EISEL0	RES1	RES0	—	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
ADCORE3L	03E0	—	—	—	—	—	—	SAMC<9:0>										0000
ADCORE3H	03E2	—	—	—	EISEL2	EISEL1	EISEL0	RES1	RES0	—	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
ADEIEL	03F0	EIEN15[1]	EIEN14[2]	EIEN13[1]	EIEN12[2]	EIEN11[2]	EIEN10[2]	EIEN9[2]	EIEN8[2]	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0	0000
ADEIEH	03F2	—	—	—	—	—	—	—	—	—	—	EIEN21	EIEN20	EIEN19	EIEN18	EIEN17[2]	EIEN16[1]	0000
ADEISTATL	03F8	EISTAT15[1]	EISTAT14[2]	EISTAT13[1]	EISTAT12[2]	EISTAT11[2]	EISTAT10[2]	EISTAT9[2]	EISTAT8[2]	EISTAT7	EISTAT6	EISTAT5	EISTAT4	EISTAT3	EISTAT2	EISTAT1	EISTAT0	0000
ADEISTATH	03FA	—	—	—	—	—	—	—	—	—	—	EISTAT21	EISTAT20	EISTAT19	EISTAT18	EISTAT17[2]	EISTAT16[1]	0000
ADCON5L	0400	SHRRDY	—	—	—	C3RDY	C2RDY	C1RDY	C0RDY	SHRPWR	—	—	—	C3PWR	C2PWR	C1PWR	C0PWR	0000
ADCON5H	0402	—	—	—	—	WARMTIME3	WARMTIME2	WARMTIME1	WARMTIME0	SHRCIE	—	—	—	C3CIE	C2CIE	C1CIE	C0CIE	0000
ADCAL0L	0404	CAL1RDY	—	—	—	—	CAL1DIFF	CAL1EN	CAL1RUN	CAL0RDY	—	—	—	—	CAL0DIFF	CAL0EN	CAL0RUN	0000
ADCAL0H	0406	CAL3RDY	—	—	—	—	CAL3DIFF	CAL3EN	CAL3RUN	CAL2RDY	—	—	—	—	CAL2DIFF	CAL2EN	CAL2RUN	0000
ADCAL1H	040A	CSHRRDY	—	—	—	—	CSHRDIFF	CSHREN	CSHRRUN	—	—	—	—	—	—	—	—	0000
ADCBUF0	040C	ADC Data Buffer 0																0000
ADCBUF1	040E	ADC Data Buffer 1																0000
ADCBUF2	0410	ADC Data Buffer 2																0000
ADCBUF3	0412	ADC Data Buffer 3																0000
ADCBUF4	0414	ADC Data Buffer 4																0000
ADCBUF5	0416	ADC Data Buffer 5																0000
ADCBUF6	041B	ADC Data Buffer 6																0000
ADCBUF7	041A	ADC Data Buffer 7																0000
ADCBUF8	041C	ADC Data Buffer 8																0000
ADCBUF9	041E	ADC Data Buffer 9																0000
ADCBUF10	0420	ADC Data Buffer 10																0000
ADCBUF11	0422	ADC Data Buffer 11																0000
ADCBUF12	0424	ADC Data Buffer 12																0000
ADCBUF13	0426	ADC Data Buffer 13																0000
ADCBUF14	0428	ADC Data Buffer 14																0000
ADCBUF15	042A	ADC Data Buffer 15																0000
ADCBUF16	042C	ADC Data Buffer 16																0000
ADCBUF17	042E	ADC Data Buffer 17																0000
ADCBUF18	0430	ADC Data Buffer 18																0000
ADCBUF19	0432	ADC Data Buffer 19																0000
ADCBUF20	0434	ADC Data Buffer 20																0000
ADCBUF21	0436	ADC Data Buffer 21																0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: Implemented on dsPIC33EPXXGS506 devices only.

2: Implemented on dsPIC33EPXXGS504/505 and dsPIC33EPXXGS506 devices only.

4.5.1 PAGED MEMORY SCHEME

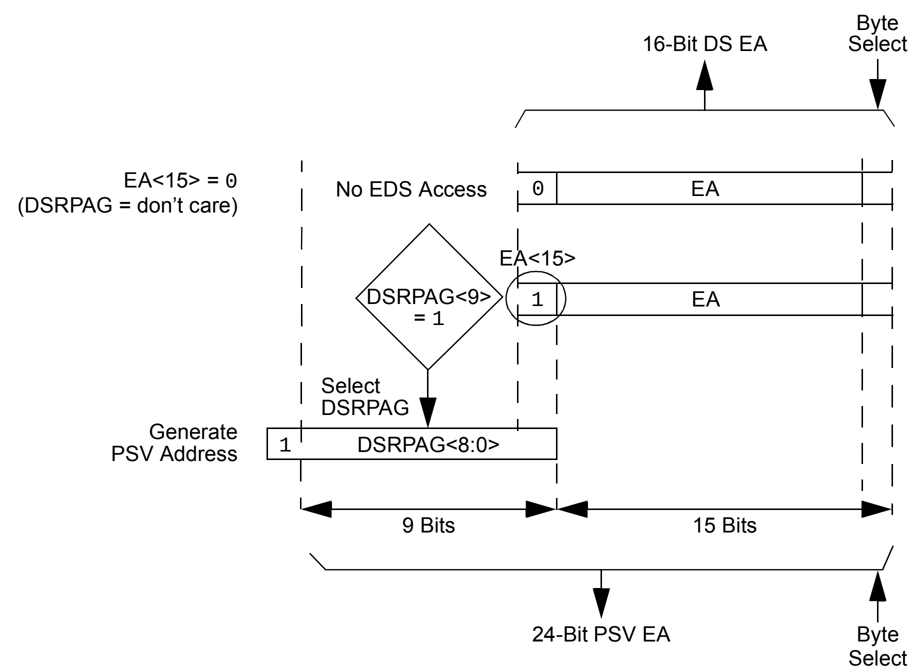
The dsPIC33EPXXGS50X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EAs). The upper half of the base Data Space address is used in conjunction with the Data Space Page (DSRPAG) register to form the Program Space Visibility (PSV) address.

The Data Space Page (DSRPAG) register is located in the SFR space. Construction of the PSV address is shown in Figure 4-9. When DSRPAG<9> = 1 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit PSV read address.

The paged memory scheme provides access to multiple 32-Kbyte windows in the PSV memory. The Data Space Page (DSRPAG) register, in combination with the upper half of the Data Space address, can provide up to 8 Mbytes of PSV address space. The paged data memory space is shown in Figure 4-10.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG.

FIGURE 4-9: PROGRAM SPACE VISIBILITY (PSV) READ ADDRESS GENERATION



Note: DS read access when DSRPAG = 0x000 will force an address error trap.

When a PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses the PSV page
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSRPAG register is incremented and the EA<15> bit is set to keep the base address within the PSV window. When an underflow is detected, the DSRPAG register is decremented and the EA<15> bit is set to keep the base address within the PSV window. This creates a linear PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0 and PSV spaces. Table 4-37 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSRPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

TABLE 4-37: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0 AND PSV SPACE BOUNDARIES(2,3,4)

O/U, R/W	Operation	Before			After		
		DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description
O, Read	`[++Wn]` or `[Wn++]`	DSRPAG = 0x2FF	`1`	PSV: Last lsw page	DSRPAG = 0x300	`1`	PSV: First MSB page
O, Read		DSRPAG = 0x3FF	`1`	PSV: Last MSB page	DSRPAG = 0x3FF	`0`	See **Note 1**
U, Read	`[--Wn]` or `[Wn--]`	DSRPAG = 0x001	`1`	PSV page	DSRPAG = 0x001	`0`	See **Note 1**
U, Read		DSRPAG = 0x200	`1`	PSV: First lsw page	DSRPAG = 0x200	`0`	See **Note 1**
U, Read		DSRPAG = 0x300	`1`	PSV: First MSB page	DSRPAG = 0x2FF	`1`	PSV: Last lsw page

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x7FFF).

2: An EDS access, with DSRPAG = 0x000, will generate an address error trap.

3: Only reads from PS are supported using DSRPAG.

4: Pseudolinear Addressing is not supported for large offsets.

4.5.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible, regardless of the contents of the Data Space Page register. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = `0`, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space in combination with DSRPAG = 0x00. Consequently, DSRPAG is initialized to 0x001 at Reset.

> **Note 1:** DSRPAG should not be used to access Page 0. An EDS access with DSRPAG set to 0x000 will generate an address error trap.
>
> **2:** Clearing the DSRPAG in software has no effect.

The remaining PSV pages are only accessible using the DSRPAG register in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = `1`.

4.5.3 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP), and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating the Stack Pointer (for example, creating stack frames).

> **Note:** To protect against misaligned stack accesses, W15<0> is fixed to ‘`0`’ by the hardware.

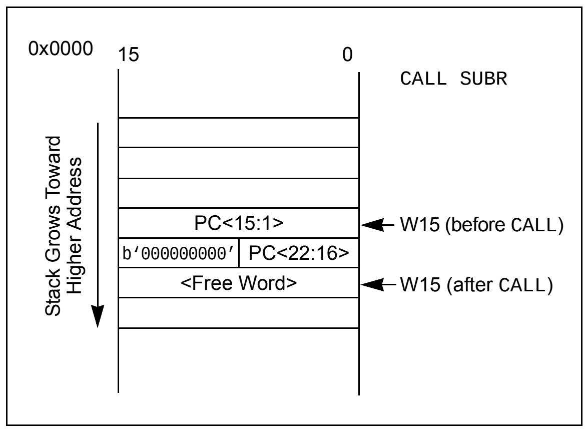
W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXGS50X devices and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack, working from lower toward higher addresses. Figure 4-11 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any `CALL` instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-11. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

> **Note 1:** To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore, restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = `1`).
>
> **2:** As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-11: CALL STACK FRAME



REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

R/SO-0(1)	R/W-0(1)	R/W-0(1)	R/W-0	R/C-0	R-0	R/W-0	R/C-0
WR	WREN	WRERR	NVMSIDL(2)	SFTSWP(6)	P2ACTIV(6)	RPDF	URERR
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
—	—	—	—	NVMOP3(3,4)	NVMOP2(3,4)	NVMOP1(3,4)	NVMOP0(3,4)
bit 7							bit 0

Legend:	C = Clearable bit	SO = Settable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit(1)
`1` = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
`0` = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
`1` = Enables Flash program/erase operations
`0` = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
`1` = An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
`0` = The program or erase operation completed normally

bit 12 **NVMSIDL:** NVM Stop in Idle Control bit(2)
`1` = Flash voltage regulator goes into Standby mode during Idle mode
`0` = Flash voltage regulator is active during Idle mode

bit 11 **SFTSWP:** Partition Soft Swap Status bit(6)
`1` = Partitions have been successfully swapped using the `BOOTSWP` instruction (soft swap)
`0` = Awaiting successful partition swap using the `BOOTSWP` instruction or a device Reset will determine the Active Partition based on FBTSEQ

bit 10 **P2ACTIV:** Partition 2 Active Status bit(6)
`1` = Partition 2 Flash is mapped into the active region
`0` = Partition 1 Flash is mapped into the active region

bit 9 **RPDF:** Row Programming Data Format bit
`1` = Row data to be stored in RAM in compressed format
`0` = Row data to be stored in RAM in uncompressed format

Note 1: These bits can only be reset on a POR.
2: If this bit is set, power consumption will be further reduced (I_{IDLE}) and upon exiting Idle mode, there is a delay (T_{VREG}) before Flash memory becomes operational.
3: All other combinations of NVMOP<3:0> are unimplemented.
4: Execution of the `PWRSAV` instruction is ignored while any of the NVM operations are in progress.
5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.
6: Only available on dsPIC33EP64GS50X devices operating in Dual Partition mode. For all other devices, this bit is reserved.
7: The specific Boot mode depends on bits<1:0> of the programmed data:
`11` = Single Partition Flash mode
`10` = Dual Partition Flash mode
`01` = Protected Dual Partition Flash mode
`00` = Reserved

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 2	**STKERR:** Stack Error Trap Status bit 1 = Stack error trap has occurred 0 = Stack error trap has not occurred
bit 1	**OSCFAIL:** Oscillator Failure Trap Status bit 1 = Oscillator failure trap has occurred 0 = Oscillator failure trap has not occurred
bit 0	**Unimplemented:** Read as '0'

8.5 Oscillator Control Registers

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2(2)	NOSC1(2)	NOSC0(2)
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF(3)	—	—	OSWEN
bit 7							bit 0

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
1 = If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and PLL configurations may be modified
0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit
1 = I/O lock is active
0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Note 1: Writes to this register require an unlock sequence.
2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.
3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and will trigger an oscillator failure trap.

NOTES:

REGISTER 14-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

`11111` = OCxRS compare event is used for synchronization
`11110` = INT2 pin synchronizes or triggers OCx
`11101` = INT1 pin synchronizes or triggers OCx
`11100` = Reserved
`11011` = CMP4 module synchronizes or triggers OCx
`11010` = CMP3 module synchronizes or triggers OCx
`11001` = CMP2 module synchronizes or triggers OCx
`11000` = CMP1 module synchronizes or triggers OCx
`10111` = Reserved
`10110` = Reserved
`10101` = Reserved
`10100` = Reserved
`10011` = IC4 input capture interrupt event synchronizes or triggers OCx
`10010` = IC3 input capture interrupt event synchronizes or triggers OCx
`10001` = IC2 input capture interrupt event synchronizes or triggers OCx
`10000` = IC1 input capture interrupt event synchronizes or triggers OCx
`01111` = Timer5 synchronizes or triggers OCx
`01110` = Timer4 synchronizes or triggers OCx
`01101` = Timer3 synchronizes or triggers OCx
`01100` = Timer2 synchronizes or triggers OCx **(default)**
`01011` = Timer1 synchronizes or triggers OCx
`01010` = Reserved
`01001` = Reserved
`01000` = IC4 input capture event synchronizes or triggers OCx
`00111` = IC3 input capture event synchronizes or triggers OCx
`00110` = IC2 input capture event synchronizes or triggers OCx
`00101` = IC1 input capture event synchronizes or triggers OCx
`00100` = OC4 module synchronizes or triggers OCx(1,2)
`00011` = OC3 module synchronizes or triggers OCx(1,2)
`00010` = OC2 module synchronizes or triggers OCx(1,2)
`00001` = OC1 module synchronizes or triggers OCx(1,2)
`00000` = No sync or trigger source for OCx

Note 1: Do not use the OCx module as its own synchronization or trigger source.
2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

REGISTER 15-5: STCON: PWMx SECONDARY MASTER TIME BASE CONTROL REGISTER

U-0	U-0	U-0	R-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	SESTAT	SEIEN	EIPU(1)	SYNCPOL	SYNCOEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Secondary special event interrupt is pending
0 = Secondary special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Secondary special event interrupt is enabled
0 = Secondary special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Secondary Period register is updated immediately
0 = Active Secondary Period register updates occur on PWMx cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit
1 = SYNCIx/SYNCO2 polarity is inverted (active-low)
0 = SYNCIx/SYNCO2 polarity is active-high

bit 8 **SYNCOEN:** Secondary Master Time Base Synchronization Enable bit
1 = SYNCO2 output is enabled
0 = SYNCO2 output is disabled

bit 7 **SYNCEN:** External Secondary Master Time Base Synchronization Enable bit
1 = External synchronization of secondary time base is enabled
0 = External synchronization of secondary time base is disabled

bit 6-4 **SYNCSRC<2:0>:** Secondary Time Base Sync Source Selection bits
111 = Reserved
101 = Reserved
100 = Reserved
011 = Reserved
010 = Reserved
001 = SYNCI2
000 = SYNCI1

bit 3-0 **SEVTPS<3:0>:** PWMx Secondary Special Event Trigger Output Postscaler Select bits
1111 = 1:16 Postscale
0001 = 1:2 Postscale
•
•
•
0000 = 1:1 Postscale

Note 1: This bit only applies to the secondary master time base period.

REGISTER 15-6: STCON2: PWMx SECONDARY CLOCK DIVIDER SELECT REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **PCLKDIV<2:0>:** PWMx Input Clock Prescaler (Divider) Select bits(1)
111 = Reserved
110 = Divide-by-64, maximum PWM timing resolution
101 = Divide-by-32, maximum PWM timing resolution
100 = Divide-by-16, maximum PWM timing resolution
011 = Divide-by-8, maximum PWM timing resolution
010 = Divide-by-4, maximum PWM timing resolution
001 = Divide-by-2, maximum PWM timing resolution
000 = Divide-by-1, maximum PWM timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 15-7: STPER: PWMx SECONDARY MASTER TIME BASE PERIOD REGISTER(1,2)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
STPER<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
STPER<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STPER<15:0>:** Secondary Master Time Base (SMTMR) Period Value bits

Note 1: The PWMx time base has a minimum value of 0x0010 and a maximum value of 0xFFF8.
2: Any period value that is less than 0x0028 must have the Least Significant 3 bits set to ‘0’, thus yielding a period resolution at 8.32 ns (at fastest auxiliary clock rate).

REGISTER 20-2: CMPxDAC: COMPARATOR x DAC CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CMREF<11:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMREF<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-0 **CMREF<11:0>:** Comparator Reference Voltage Select bits

111111111111
•
•
• = ([CMREF<11:0>] * (AV_{DD})/4096) volts (EXTREF = 0)
• or ([CMREF<11:0>] * (EXTREF)/4096) volts (EXTREF = 1)
•
•
000000000000

TABLE 23-1: CONFIGURATION REGISTER MAP(3) (CONTINUED)

Name	Address	Device Memory Size (Kbytes)	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FDEVOPT	002BAC	16	—	—	—	—	—	—	—	—	—	—	DBCC	—	ALTI2C2	ALTI2C1	Reserved(1)	—	PWMLOCK
	0057AC	32																	
	00AFAC	64																	
FALTREG	002BB0	16	—	—	—	—	—	—	—	—	—	—	CTXT2<2:0>			—	CTXT1<2:0>		
	0057B0	32																	
	00AFB0	64																	
FBTSEQ	002BFC	16	IBSEQ<11:0>					BSEQ<11:0>											
	0057FC	32																	
	00AFFC	64																	
FBOOT(4)	801000	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BTMODE<1:0>	

Note 1: These bits are reserved and must be programmed as '1'.
2: This bit is reserved and must be programmed as '0'.
3: When operating in Dual Partition mode, each partition will have dedicated Configuration registers. On a device Reset, the configuration values of the Active Partition are read at start-up, but during a soft swap condition, the configuration settings of the newly Active Partition are ignored.
4: FBOOT resides in configuration memory space.

TABLE 23-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
WDTEN<1:0>	Watchdog Timer Enable bits 11 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled; clearing the SWDTEN bit in the RCON register will have no effect) 10 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register) 01 = Watchdog Timer is enabled only while device is active and is disabled while in Sleep mode; software control is disabled in this mode 00 = Watchdog Timer and SWDTEN bit are disabled
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled
WDTPRE	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1

Note 1: The Boot Segment must be present to use the Alternate Interrupt Vector Table.

26.1 DC Characteristics

TABLE 26-1: OPERATING MIPS vs. VOLTAGE

Characteristic	V_{DD} Range (in Volts)	Temperature Range (in °C)	Maximum MIPS
			dsPIC33EPXXGS50X Family
—	3.0V to 3.6V(1)	-40°C to +85°C	70
—	3.0V to 3.6V(1)	-40°C to +125°C	60

Note 1: Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules (ADC, PGAs and comparators) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 26-13 for the minimum and maximum BOR values.

TABLE 26-2: THERMAL OPERATING CONDITIONS

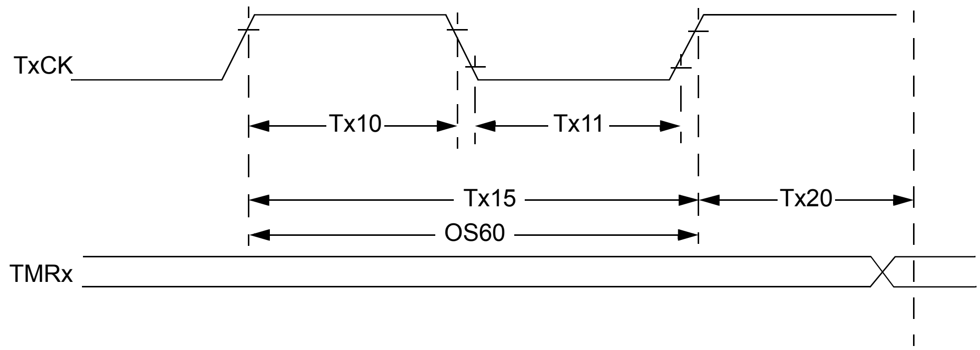
Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+140	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 26-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 64-Pin TQFP 10x10x1 mm	θ_{JA}	49.0	—	°C/W	1
Package Thermal Resistance, 48-Pin TQFP 7x7x1.0 mm	θ_{JA}	63.0	—	°C/W	1
Package Thermal Resistance, 44-Pin QFN 8x8 mm	θ_{JA}	29.0	—	°C/W	1
Package Thermal Resistance, 44-Pin TQFP 10x10x1 mm	θ_{JA}	50.0	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S 6x6x0.9 mm	θ_{JA}	30.0	—	°C/W	1
Package Thermal Resistance, 28-Pin UQFN 6x6x0.5 mm	θ_{JA}	26.0	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC 7.50 mm	θ_{JA}	70.0	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

FIGURE 26-5: TIMER1-TIMER5 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 26-1 for load conditions.

TABLE 26-24: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS[1]

AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic[2]**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	T_{TXH}	T1CK High Time	Synchronous mode	Greater of: 20 or (T_{CY} + 20)/N	—	—	ns	Must also meet Parameter TA15, N = Prescale Value (1, 8, 64, 256)
			Asynchronous	35	—	—	ns	
TA11	T_{TXL}	T1CK Low Time	Synchronous mode	Greater of: 20 or (T_{CY} + 20)/N	—	—	ns	Must also meet Parameter TA15, N = Prescale Value (1, 8, 64, 256)
			Asynchronous	10	—	—	ns	
TA15	T_{TXP}	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 T_{CY} + 40)/N	—	—	ns	N = Prescale Value (1, 8, 64, 256)
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC	—	50	kHz	
TA20	$T_{CKEXTMRL}$	Delay from External T1CK Clock Edge to Timer Increment		0.75 T_{CY} + 40	—	1.75 T_{CY} + 40	ns	

Note 1: Timer1 is a Type A timer.
2: These parameters are characterized but not tested in manufacturing.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

dsPIC 33 EP 64 GS5 04 T - I / PT XXX

Microchip Trademark
Architecture
Flash Memory Family
Program Memory Size (Kbyte)
Product Group
Pin Count
Tape and Reel Flag (if applicable)
Temperature Range
Package
Pattern

Architecture:	33	=	16-Bit Digital Signal Controller
Flash Memory Family:	EP	=	Enhanced Performance
Product Group:	GS	=	SMPS Family
Pin Count:	02	=	28-pin
	04	=	44-pin
	05	=	48-pin
	06	=	64-pin
Temperature Range:	I	=	-40°C to +85°C (Industrial)
	E	=	-40°C to +125°C (Extended)
Package:	2N	=	Ultra Thin Quad Flat, No Lead – (28-pin) 6x6 mm (UQFN)
	ML	=	Plastic Quad Flat, No Lead – (44-pin) 8x8 mm body (QFN)
	MM	=	Plastic Quad Flat, No Lead – (28-pin) 6x6 mm body (QFN-S)
	PT	=	Plastic Thin Quad Flatpack – (44-pin) 10x10 mm body (TQFP)
	PT	=	Plastic Thin Quad Flatpack – (64-pin) 10x10 mm body (TQFP)
	SO	=	Plastic Small Outline, Wide – (28-pin) 7.50 mm body (SOIC)
	Y8	=	Thin Quad Flatpack – (48-pin) 7x7 mm (TQFP)

Examples:

dsPIC33EP64GS504-I/PT:
dsPIC33, Enhanced Performance, 64-Kbyte Program Memory, SMPS, 44-Pin, Industrial Temperature, TQFP Package.