Microchip Technology - DSPIC33EP16GS505-I/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep16gs505-i-pt

3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

3.6.1 KEY RESOURCES

- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC12	0858	—	—	—	—	—	MI2C2IP2	MI2C2IP1	MI2C2IP0	—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	—	—	—	0440
IPC13	085A	—	—	—	—	—	INT4IP2	INT4IP1	INT4IP0	—	—	—	—	—	—	—	—	0400
IPC14	085C	—	—	—	—	—	—	—	—	—	PSEMIP2	PSEMIP1	PSEMIP0	—	—	—	—	0040
IPC16	0860	—	—	—	—	—	U2EIP2	U2EIP1	U2EIP0	—	U1EIP2	U1EIP1	U1EIP0	—	—	—	—	0440
IPC18	0864	—	—	—	—	—	—	—	—	—	PSESIP2	PSESIP1	PSESIP0	—	—	—	—	0040
IPC23	086E	—	PWM2IP2	PWM2IP1	PWM2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	4400
IPC24	0870	—	—	—	—	—	PWM5IP2	PWM5IP1	PWM5IP0	—	PWM4IP2	PWM4IP1	PWM4IP0	—	PWM3IP2	PWM3IP1	PWM3IP0	0444
IPC25	0872	—	AC2IP2	AC2IP1	AC2IP0	—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC26	0874	—	—	—	—	—	—	—	—	—	AC4IP2	AC4IP1	AC4IP0	—	AC3IP2	AC3IP1	AC3IP0	0044
IPC27	0876	—	ADCAN1IP2	ADCAN1IP1	ADCAN1IP0	—	ADCAN0IP2	ADCAN0IP1	ADCAN0IP0	—	—	—	—	—	—	—	—	4400
IPC28	0878	—	ADCAN5IP2	ADCAN5IP1	ADCAN5IP0	—	ADCAN4IP2	ADCAN4IP1	ADCAN4IP0	—	ADCAN3IP2	ADCAN3IP1	ADCAN3IP0	—	ADCAN2IP2	ADCAN2IP1	ADCAN2IP0	4444
IPC29	087A	—	—	—	—	—	—	—	—	—	ADCAN7IP2	ADCAN7IP1	ADCAN7IP0	—	ADCAN6IP2	ADCAN6IP1	ADCAN6IP0	0044
IPC35	0886	—	JTAGIP2	JTAGIP1	JTAGIP0	—	ICDIP2	ICDIP1	ICDIP0	—	—	—	—	—	—	—	—	4400
IPC37	088A	—	ADCAN8IP2(2)	ADCAN8IP1(2)	ADCAN8IP0(2)	—	—	—	—	—	—	—	—	—	—	—	—	4000
IPC38	088C	—	ADCAN12IP2(2)	ADCAN12IP1(2)	ADCAN12IP0(2)	—	ADCAN11IP2(2)	ADCAN11IP1(2)	ADCAN11IP0(2)	—	ADCAN10IP2(2)	ADCAN10IP1(2)	ADCAN10IP0(2)	—	ADCAN9IP2(2)	ADCAN9IP1(2)	ADCAN9IP0(2)	4444
IPC39	088E	—	ADCAN16IP2(1)	ADCAN16IP1(1)	ADCAN16IP0(1)	—	ADCAN15IP2(1)	ADCAN15IP1(1)	ADCAN15IP0(1)	—	ADCAN14IP2(2)	ADCAN14IP1(2)	ADCAN14IP0(2)	—	ADCAN13IP2(1)	ADCAN13IP1	ADCAN13IP0	4444
IPC40	0890	—	ADCAN20IP2	ADCAN20IP1	ADCAN20IP0	—	ADCAN19IP2	ADCAN19IP1	ADCAN19IP0	—	ADCAN18IP2	ADCAN18IP1	ADCAN18IP0	—	ADCAN17IP2(2)	ADCAN17IP1(2)	ADCAN17IP0(2)	4444
IPC41	0892	—	—	—	—	—	—	—	—	—	—	—	—	—	ADCAN21IP2	ADCAN21IP1	ADCAN21IP0	0004
IPC43	0896	—	—	—	—	—	I2C2BCIP2	I2C2BCIP1	I2C2BCIP0	—	I2C1BCIP2	I2C1BCIP1	I2C1BCIP0	—	—	—	—	0440
IPC44	0898	—	ADFLTR0IP2	ADFLTR0IP1	ADFLTR0IP0	—	ADCMP1IP2	ADCMP1IP1	ADCMP1IP0	—	ADCMP0IP2	ADCMP0IP1	ADCMP0IP0	—	—	—	—	4440
IPC45	089A	—	—	—	—	—	—	—	—	—	—	—	—	—	ADFLTR1IP2	ADFLTR1IP1	ADFLTR1IP0	0004
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	AIVTEN	—	—	—	INT4EP	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	NAE	—	—	—	DOOVR	—	—	—	APLL	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR3	ILR2	ILR1	ILR0	VECNUM7	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Only available on dsPIC33EPXXGS506 devices.

2: Only available on dsPIC33EPXXGS504/505 and dsPIC33EPXXGS506 devices.

TABLE 4-11: PWM GENERATOR 4 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON4	0C80	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	MTBS	CAM	XPRES	IUE	0000
IOCON4	0C82	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON4	0C84	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC4	0C86	PWM4 Generator Duty Cycle Register (PDC4<15:0>)																0000
PHASE4	0C88	PWM4 Primary Phase-Shift or Independent Time Base Period Register (PHASE4<15:0>)																0000
DTR4	0C8A	—	—	PWM4 Dead-Time Register (DTR4<13:0>)														0000
ALTDTR4	0C8C	—	—	PWM4 Alternate Dead-Time Register (ALTDTR4<13:0>)														0000
SDC4	0C8E	PWM4 Secondary Duty Cycle Register (SDC4<15:0>)																0000
SPHASE4	0C90	PWM4 Secondary Phase-Shift Register (SPHASE4<15:0>)																0000
TRIG4	0C92	PWM4 Primary Trigger Compare Value Register (TRGCMP<12:0>)													—	—	—	0000
TRGCON4	0C94	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG4	0C96	PWM4 Secondary Trigger Compare Value Register (STRGCMP<12:0>)													—	—	—	0000
PWMCAP4	0C98	PWM4 Primary Time Base Capture Register (PWMCAP<12:0>)													—	—	—	0000
LEBCON4	0C9A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY4	0C9C	—	—	—	—	PWM4 Leading-Edge Blanking Delay Register (LEB<8:0>)									—	—	—	0000
AUXCON4	0C9E	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: PWM GENERATOR 5 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON5	0CA0	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	MTBS	CAM	XPRES	IUE	0000
IOCON5	0CA2	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON5	0CA4	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC5	0CA6	PWM5 Generator Duty Cycle Register (PDC5<15:0>)																0000
PHASE5	0CA8	PWM5 Primary Phase-Shift or Independent Time Base Period Register (PHASE5<15:0>)																0000
DTR5	0CAA	—	—	PWM5 Dead-Time Register (DTR5<13:0>)														0000
ALTDTR5	0CAC	—	—	PWM5 Alternate Dead-Time Register (ALTDTR5<13:0>)														0000
SDC5	0CAE	PWM5 Secondary Duty Cycle Register (SDC5<15:0>)																0000
SPHASE5	0CB0	PWM5 Secondary Phase-Shift Register (SPHASE5<15:0>)																0000
TRIG5	0CB2	PWM5 Primary Trigger Compare Value Register (TRGCMP<12:0>)													—	—	—	0000
TRGCON5	0CB4	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG5	0CB6	PWM5 Secondary Trigger Compare Value Register (STRGCMP<12:0>)													—	—	—	0000
PWMCAP5	0CB8	PWM5 Primary Time Base Capture Register (PWMCAP<12:0>)													—	—	—	0000
LEBCON5	0CBA	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY5	0CBC	—	—	—	—	PWM5 Leading-Edge Blanking Delay Register (LEB<8:0>)									—	—	—	0000
AUXCON5	0CBE	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: PMD REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	ADCMD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	I2C2MD	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	076A	—	—	—	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	CMP4MD	CMP3MD	CMP2MD	CMP1MD	—	—	—	—	—	—	PGA1MD	—	0000
PMD8	076E	—	—	—	—	—	PGA2MD	ABGMD	—	—	—	—	—	—	—	CCSMD	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: CONSTANT-CURRENT SOURCE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ISRCCON	0500	ISRCEN	—	—	—	—	OUTSEL2	OUTSEL1	OUTSEL0	—	—	ISRCCAL5	ISRCCAL4	ISRCCAL3	ISRCCAL2	ISRCCAL1	ISRCCAL0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: PROGRAMMABLE GAIN AMPLIFIER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PGA1CON	0504	PGAEN	PGAOEN	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0	—	—	—	—	—	GAIN2	GAIN1	GAIN0	0000
PGA1CAL	0506	—	—	—	—	—	—	—	—	—	—	PGACAL<5:0>						0000
PGA2CON	0508	PGAEN	PGAOEN	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0	—	—	—	—	—	GAIN2	GAIN1	GAIN0	0000
PGA2CAL	050A	—	—	—	—	—	—	—	—	—	—	PGACAL<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: ANALOG COMPARATOR REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMP1CON	0540	CMPON	—	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE	INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE	0000
CMP1DAC	0542	—	—	—	—	CMREF<11:0>												0000
CMP2CON	0544	CMPON	—	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE	INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE	0000
CMP2DAC	0546	—	—	—	—	CMREF<11:0>												0000
CMP3CON	0548	CMPON	—	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE	INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE	0000
CMP3DAC	054A	—	—	—	—	CMREF<11:0>												0000
CMP4CON	054C	CMPON	—	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE	INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE	0000
CMP4DAC	054E	—	—	—	—	CMREF<11:0>												0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-27: JTAG INTERFACE REGISTER MAP

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	—	—	—	—	JDATAH<11:0>												xxxx
JDATAL	0FF2	JDATAL<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.5.1 PAGED MEMORY SCHEME

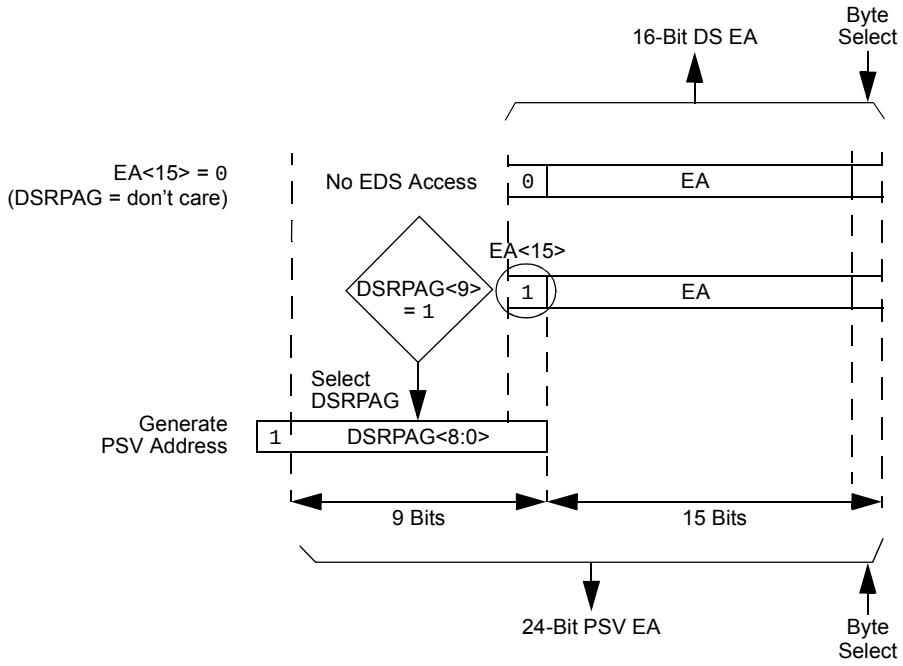
The dsPIC33EPXXGS50X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EAs). The upper half of the base Data Space address is used in conjunction with the Data Space Page (DSRPAG) register to form the Program Space Visibility (PSV) address.

The Data Space Page (DSRPAG) register is located in the SFR space. Construction of the PSV address is shown in Figure 4-9. When DSRPAG<9> = 1 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit PSV read address.

The paged memory scheme provides access to multiple 32-Kbyte windows in the PSV memory. The Data Space Page (DSRPAG) register, in combination with the upper half of the Data Space address, can provide up to 8 Mbytes of PSV address space. The paged data memory space is shown in Figure 4-10.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG.

FIGURE 4-9: PROGRAM SPACE VISIBILITY (PSV) READ ADDRESS GENERATION



Note: DS read access when DSRPAG = 0x000 will force an address error trap.

9.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (DS70615) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS50X family devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXGS50X family devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

9.1 Clock Frequency and Clock Switching

The dsPIC33EPXXGS50X family devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 8.0 "Oscillator Configuration"**.

9.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXGS50X family devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 9-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

EXAMPLE 9-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV  #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV  #IDLE_MODE     ; Put the device into Idle mode
```

REGISTER 10-6: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC4R7	IC4R6	IC4R5	IC4R4	IC4R3	IC4R2	IC4R1	IC4R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC3R7	IC3R6	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **IC4R<7:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

bit 7-0 **IC3R<7:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

REGISTER 10-12: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK1INR7	SCK1INR6	SCK1INR5	SCK1INR4	SCK1INR3	SCK1INR2	SCK1INR1	SCK1INR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI1R7	SDI1R6	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **SCK1INR<7:0>:** Assign SPI1 Clock Input (SCK1) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

bit 7-0 **SDI1R<7:0>:** Assign SPI1 Data Input (SDI1) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

13.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Input Capture"** (DS70000352) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurements. The dsPIC33EPXXGS50X family devices support four input capture channels.

Key features of the input capture module include:

- Hardware-Configurable for 32-Bit Operation in All modes by Cascading Two Adjacent Modules
- Synchronous and Trigger modes of Output Compare Operation, with up to 21 User-Selectable Trigger/Sync Sources Available
- A 4-Level FIFO Buffer for Capturing and Holding Timer Values for Several Events
- Configurable Interrupt Generation
- Up to Six Clock Sources Available for Each Module, Driving a Separate Internal 16-Bit Counter

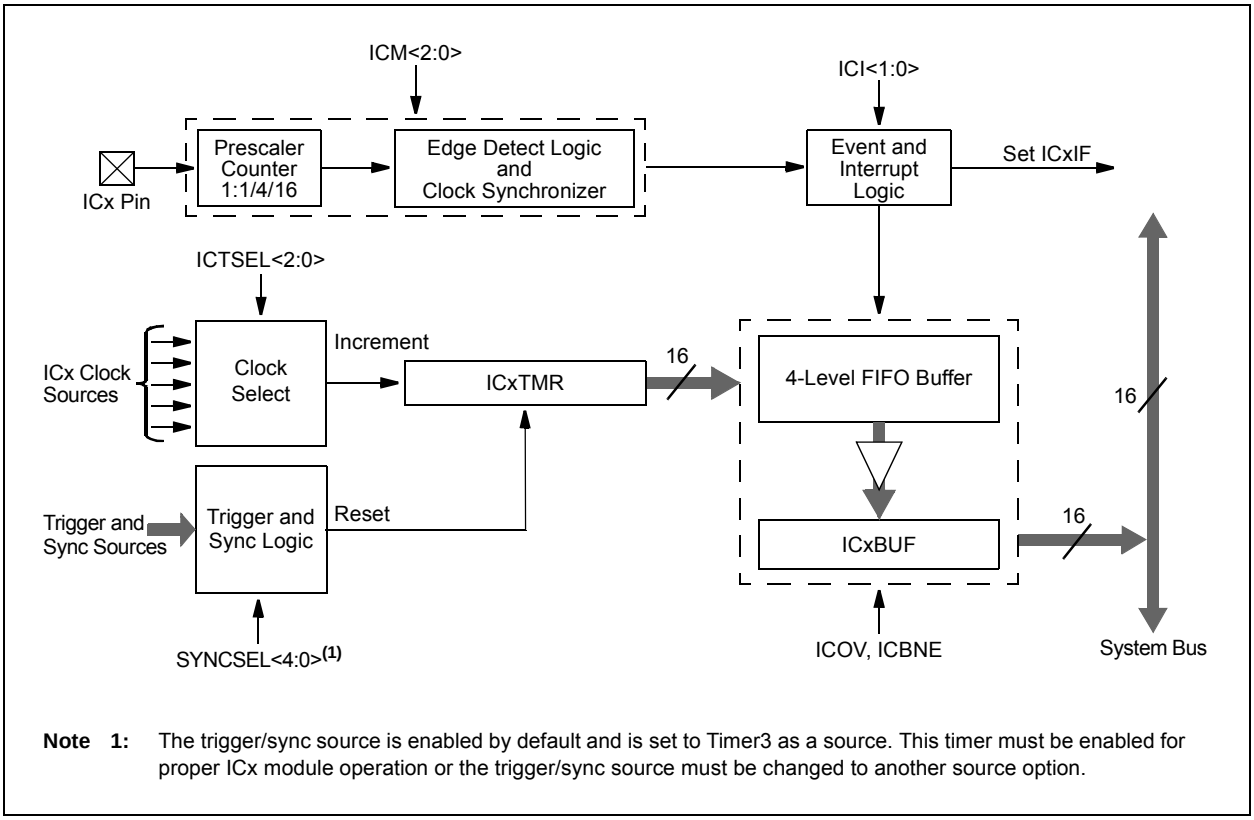
13.1 Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

13.1.1 KEY RESOURCES

- **"Input Capture"** (DS70000352) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

FIGURE 13-1: INPUT CAPTURE x MODULE BLOCK DIAGRAM



Note 1: The trigger/sync source is enabled by default and is set to Timer3 as a source. This timer must be enabled for proper ICx module operation or the trigger/sync source must be changed to another source option.

REGISTER 14-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

11111 = OCxRS compare event is used for synchronization
11110 = INT2 pin synchronizes or triggers OCx
11101 = INT1 pin synchronizes or triggers OCx
11100 = Reserved
11011 = CMP4 module synchronizes or triggers OCx
11010 = CMP3 module synchronizes or triggers OCx
11001 = CMP2 module synchronizes or triggers OCx
11000 = CMP1 module synchronizes or triggers OCx
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = Reserved
10011 = IC4 input capture interrupt event synchronizes or triggers OCx
10010 = IC3 input capture interrupt event synchronizes or triggers OCx
10001 = IC2 input capture interrupt event synchronizes or triggers OCx
10000 = IC1 input capture interrupt event synchronizes or triggers OCx
01111 = Timer5 synchronizes or triggers OCx
01110 = Timer4 synchronizes or triggers OCx
01101 = Timer3 synchronizes or triggers OCx
01100 = Timer2 synchronizes or triggers OCx **(default)**
01011 = Timer1 synchronizes or triggers OCx
01010 = Reserved
01001 = Reserved
01000 = IC4 input capture event synchronizes or triggers OCx
00111 = IC3 input capture event synchronizes or triggers OCx
00110 = IC2 input capture event synchronizes or triggers OCx
00101 = IC1 input capture event synchronizes or triggers OCx
00100 = OC4 module synchronizes or triggers OCx**(1,2)**
00011 = OC3 module synchronizes or triggers OCx**(1,2)**
00010 = OC2 module synchronizes or triggers OCx**(1,2)**
00001 = OC1 module synchronizes or triggers OCx**(1,2)**
00000 = No sync or trigger source for OCx

Note 1: Do not use the OCx module as its own synchronization or trigger source.

2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

REGISTER 15-12: PWMCONx: PWMx CONTROL REGISTER (x = 1 to 5) (CONTINUED)

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
11 = Reserved
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied for all Output modes

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **MTBS:** Master Time Base Select bit
1 = PWMx generator uses the secondary master time base for synchronization and the clock source for the PWMx generation logic (if secondary time base is available)
0 = PWMx generator uses the primary master time base for synchronization and the clock source for the PWMx generation logic

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,3,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWMx Reset Control bit(5)
1 = Current-limit source resets the time base for this PWMx generator if it is in Independent Time Base mode
0 = External pins do not affect the PWMx time base

bit 0 **IUE:** Immediate Update Enable bit
1 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are immediate
0 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are synchronized to the local PWMx time base

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
3: These bits should not be changed after the PWMx is enabled by setting PTEN = 1 (PTCON<15>).
4: Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.
5: Configure CLMOD = 0 (FCLCONx<8>) and ITB = 1 (PWMCONx<9>) to operate in External Period Reset mode.

REGISTER 15-15: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER (x = 1 to 5)(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx<15:0>:** PWMx Phase-Shift Value or Independent Time Base Period for the PWMx Generator bits

Note 1: If PWMCONx<9> = 0, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (IOCONx<11:10> = 00, 01 or 10); PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs
- True Independent Output mode (IOCONx<11:10> = 11); PHASEx<15:0> = Phase-shift value for PWMxH only
- When the PHASEx/SPHASEx registers provide the phase shift with respect to the master time base; therefore, the valid range is 0x0000 through period

2: If PWMCONx<9> = 1, the following applies based on the mode of operation:
- Complementary, Redundant, and Push-Pull Output mode (IOCONx<11:10> = 00, 01 or 10); PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL
- True Independent Output mode (IOCONx<11:10> = 11); PHASEx<15:0> = Independent time base period value for PWMxH only
- When the PHASEx/SPHASEx registers provide the local period, the valid range is 0x0000 through 0xFFF8

REGISTER 15-20: IOCONx: PWMx I/O CONTROL REGISTER (x = 1 to 5)

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1(1)	PMOD0(1)	OVRENH	OVRENL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1(2)	FLTDAT0(2)	CLDAT1(2)	CLDAT0(2)	SWAP	OSYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PENH:** PWMxH Output Pin Ownership bit
1 = PWMx module controls the PWMxH pin
0 = GPIO module controls the PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit
1 = PWMx module controls the PWMxL pin
0 = GPIO module controls the PWMxL pin

bit 13 **POLH:** PWMxH Output Pin Polarity bit
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWMxL Output Pin Polarity bit
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD<1:0>:** PWMx I/O Pin Mode bits(1)
11 = PWMx I/O pin pair is in the True Independent Output mode
10 = PWMx I/O pin pair is in the Push-Pull Output mode
01 = PWMx I/O pin pair is in the Redundant Output mode
00 = PWMx I/O pin pair is in the Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT1 provides data for output on the PWMxH pin
0 = PWMx generator provides data for the PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT0 provides data for output on the PWMxL pin
0 = PWMx generator provides data for the PWMxL pin

bit 7-6 **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
If OVERENH = 1, OVRDAT1 provides data for the PWMxH pin
If OVERENL = 1, OVRDAT0 provides data for the PWMxL pin

bit 5-4 **FLTDAT<1:0>:** State for PWMxH and PWMxL Pins if FLTMOD<1:0> are Enabled bits(2)
IFLTMOD (FCLCONx<15>) = 0: Normal Fault Mode:
If Fault is active, then FLTDAT1 provides the state for the PWMxH pin.
If Fault is active, then FLTDAT0 provides the state for the PWMxL pin.
IFLTMOD (FCLCONx<15>) = 1: Independent Fault Mode:
If current limit is active, then FLTDAT1 provides the state for the PWMxH pin.
If Fault is active, then FLTDAT0 provides the state for the PWMxL pin.

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: State represents the active/inactive state of the PWMx depending on the POLH and POLL bits settings.

TABLE 26-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		Any I/O Pin and $\overline{MCLR}$	VSS	—	0.2 VDD	V	
DI18		I/O Pins with SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SDAx, SCLx	VSS	—	0.8	V	SMBus enabled
	VIH	**Input High Voltage**					
DI20		I/O Pins Not 5V Tolerant(4)	0.8 VDD	—	VDD	V	
		I/O Pins 5V Tolerant and $\overline{MCLR}$(4)	0.8 VDD	—	5.5	V	
		5V Tolerant I/O Pins with SDAx, SCLx(4)	0.8 VDD	—	5.5	V	SMBus disabled
		5V Tolerant I/O Pins with SDAx, SCLx(4)	2.1	—	5.5	V	SMBus enabled
		I/O Pins with SDAx, SCLx Not 5V Tolerant(4)	0.8 VDD	—	VDD	V	SMBus disabled
		I/O Pins with SDAx, SCLx Not 5V Tolerant(4)	2.1	—	VDD	V	SMBus enabled
DI30	ICNPU	**Input Change Notification Pull-up Current**	150	340	550	μA	VDD = 3.3V, VPIN = VSS
DI31	ICNPD	**Input Change Notification Pull-Down Current(5)**	20	60	100	μA	VDD = 3.3V, VPIN = VDD

Note 1: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See the **"Pin Diagrams"** section for the 5V tolerant I/O pins.

5: VIL Source < (VSS – 0.3). Characterized but not tested.

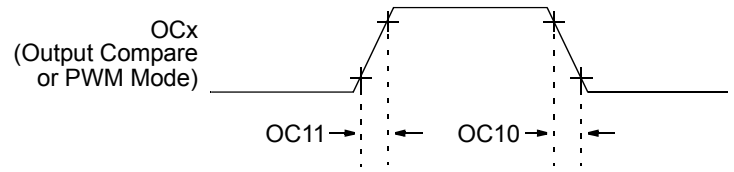
6: VIH Source > (VDD + 0.3) for pins that are not 5V tolerant only.

7: Digital 5V tolerant pins do not have internal high-side diodes to VDD and cannot tolerate any "positive" input injection current.

8: Injection Currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 26-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 26-1 for load conditions.

TABLE 26-28: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 26-8: OCx/PWMx MODULE TIMING CHARACTERISTICS

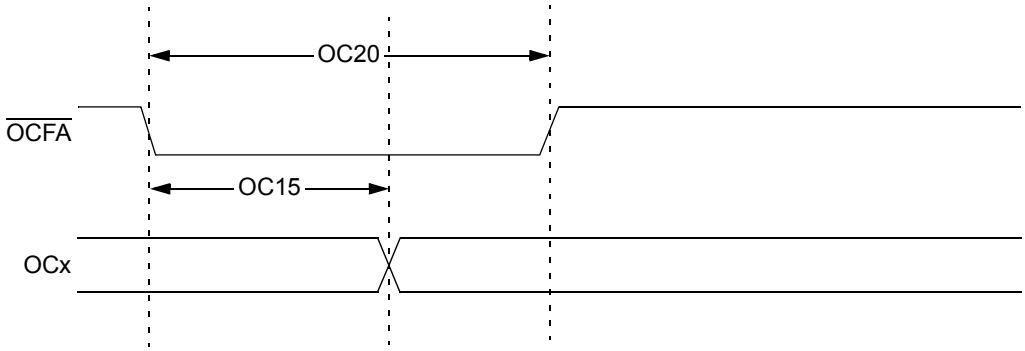


TABLE 26-29: OCx/PWMx MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWMx I/O Change	—	—	TCY + 20	ns	
OC20	TFLT	Fault Input Pulse Width	TCY + 20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

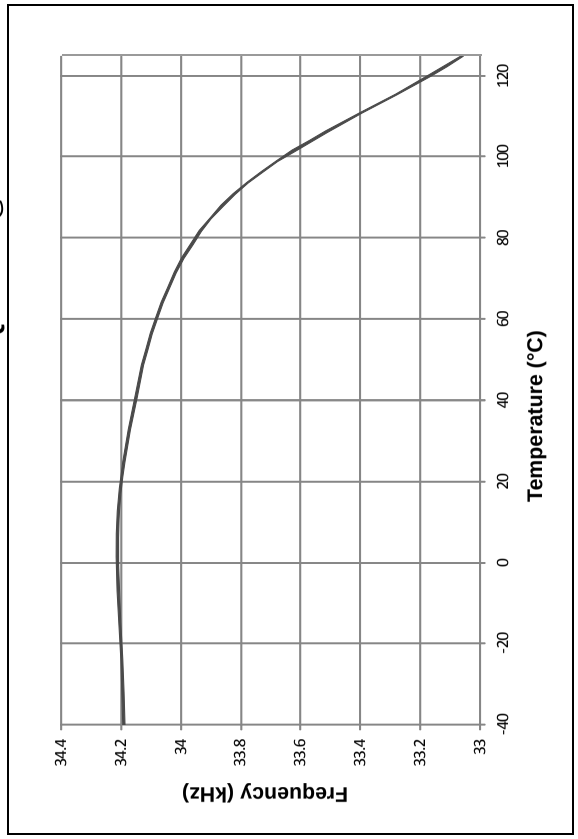


FIGURE 27-10: TYPICAL LPRC FREQUENCY @ V_{DD} = 3.3V

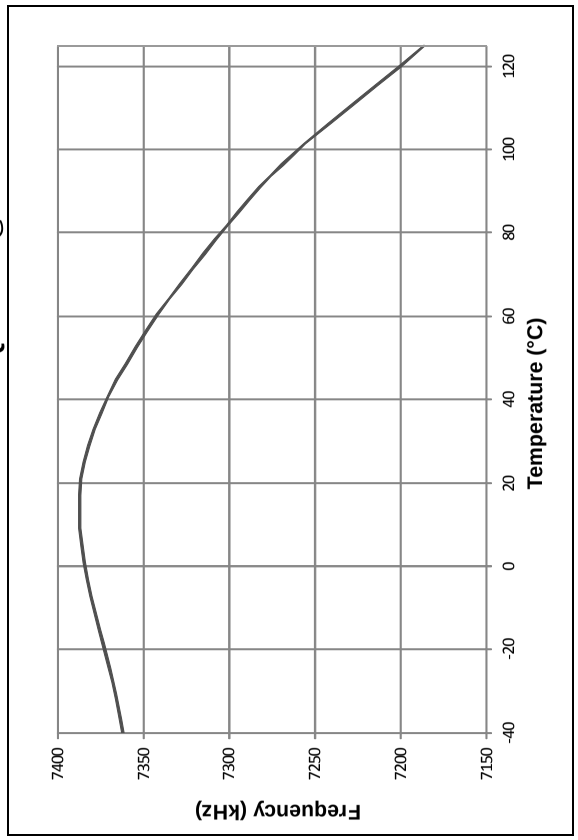
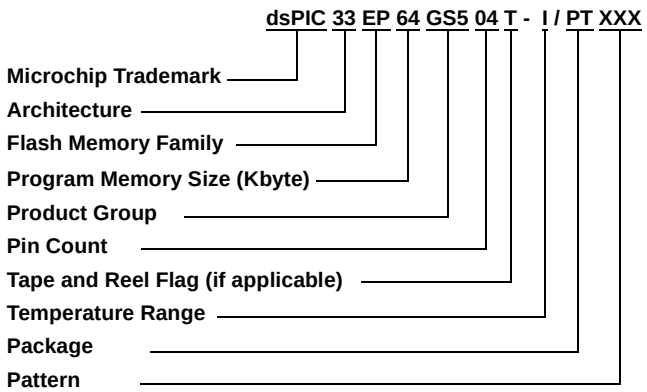


FIGURE 27-9: TYPICAL FRC FREQUENCY @ V_{DD} = 3.3V

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture:	33	=	16-Bit Digital Signal Controller
Flash Memory Family:	EP	=	Enhanced Performance
Product Group:	GS	=	SMPS Family
Pin Count:	02	=	28-pin
	04	=	44-pin
	05	=	48-pin
	06	=	64-pin
Temperature Range:	I	=	-40°C to +85°C (Industrial)
	E	=	-40°C to +125°C (Extended)
Package:	2N	=	Ultra Thin Quad Flat, No Lead – (28-pin) 6x6 mm (UQFN)
	ML	=	Plastic Quad Flat, No Lead – (44-pin) 8x8 mm body (QFN)
	MM	=	Plastic Quad Flat, No Lead – (28-pin) 6x6 mm body (QFN-S)
	PT	=	Plastic Thin Quad Flatpack – (44-pin) 10x10 mm body (TQFP)
	PT	=	Plastic Thin Quad Flatpack – (64-pin) 10x10 mm body (TQFP)
	SO	=	Plastic Small Outline, Wide – (28-pin) 7.50 mm body (SOIC)
	Y8	=	Thin Quad Flatpack – (48-pin) 7x7 mm (TQFP)

Examples:

dsPIC33EP64GS504-I/PT:
dsPIC33, Enhanced Performance, 64-Kbyte Program Memory, SMPS, 44-Pin, Industrial Temperature, TQFP Package.

NOTES: