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Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	48-TQFP Exposed Pad
Supplier Device Package	48-TQFP-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep16gs505t-e-pt

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2	SFA: Stack Frame Active Status bit
	 1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG 0 = Stack frame is not active; W14 and W15 address the base Data Space
bit 1	RND: Rounding Mode Select bit
	1 = Biased (conventional) rounding is enabled0 = Unbiased (convergent) rounding is enabled
bit 0	IF: Integer or Fractional Multiplier Mode Select bit
	 1 = Integer mode is enabled for DSP multiply 0 = Fractional mode is enabled for DSP multiply
Note 1:	This bit is always read as '0'.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	CCTXI2	CCTXI1	CCTXI0
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	MCTXI2	MCTXI1	MCTXI0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown						nown	

bit 15-11	Unimplemented: Read as '0'
bit 10-8	CCTXI<2:0>: Current (W Register) Context Identifier bits
	111 = Reserved
	•
	•
	•
	011 = Reserved
	010 = Alternate Working Register Set 2 is currently in use
	001 = Alternate Working Register Set 1 is currently in use
	000 = Default register set is currently in use
bit 7-3	Unimplemented: Read as '0'
bit 2-0	MCTXI<2:0>: Manual (W Register) Context Identifier bits
	111 = Reserved
	•
	•
	•
	011 = Reserved
	010 = Alternate Working Register Set 2 was most recently manually selected
	001 = Alternate Working Register Set 1 was most recently manually selected
	000 = Default register set was most recently manually selected

TABLE 4-7: PWM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	_	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
PTCON2	0C02								PCLKDIV<2:0>			0000						
PTPER	0C04	PWMx Primary Master Time Base Period Register (PTPER<15:0>)											FFF8					
SEVTCMP	0C06					PW	/Mx Spec	ial Event Cor	npare Registe	er (SEVTCMF	P12:0>)				_	_	_	0000
MDC	0C0A	PWMx Master Duty Cycle Register (MDC<15:0>)											0000					
STCON	0C0E	_	-	_	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
STCON2	0C10	_	-	_	_	-	_	_	_	_	_	_	_	_	F	PCLKDIV<2:0)>	0000
STPER	0C12							PWMx Seco	ondary Master	Time Base F	Period Registe	er (STPER<15	:0>)					FFF8
SSEVTCMP	0C14				P	WMx Se	condary S	Special Event	Compare Re	gister (SSEV	TCMP<12:0>))			_	_	_	0000
CHOP	0C1A	CHPCLKEN	_	_	_	-	_	CHOPCLK6	CHOPCLK5	CHOPCLK4	CHOPCLK3	CHOPCLK2	CHOPCLK1	CHOPCLK0	_	_	_	0000
PWMKEY	0C1E	PWMx Protection Lock/Unlock Key Register (PWMKEY<15:0>)								0000								

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: PWM GENERATOR 1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	_	_	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON1	0C24	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC1	0C26							PWM1 Ger	nerator Duty C	cle Registe	er (PDC1<15	5:0>)						0000
PHASE1	0C28					F	PWM1 Primary	Phase-Shift o	r Independent	Time Base	Period Reg	ister (PHASE	1<15:0>)					0000
DTR1	0C2A	—	_						PWM1 D	ead-Time R	egister (DTF	R1<13:0>)						0000
ALTDTR1	0C2C	—	—					P	WM1 Alternate	e Dead-Tim	e Register (A	ALTDTR1<13	:0>)					0000
SDC1	0C2E							PWM1 Sec	ondary Duty C	ycle Registe	er (SDC1<1	5:0>)						0000
SPHASE1	0C30							PWM1 Second	dary Phase-Sh	ift Register	(SPHASE1	<15:0>)						0000
TRIG1	0C32					PWM1 Pr	imary Trigger	Compare Value	e Register (TR	GCMP<12:	0>)				—	—	_	0000
TRGCON1	0C34	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	_	_	-	_	DTM	_	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG1	0C36					PWM1 Seco	ondary Trigger	Compare Valu	ie Register (S	FRGCMP<1	2:0>)				_	_	—	0000
PWMCAP1	0C38					PWM1 F	Primary Time E	Base Capture I	Register (PWN	1CAP<12:0	>)				_	_	—	0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_	—	_	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	_	_	_	_			PWM1 Lea	ding-Edge Bla	nking Delay	Register (L	EB<8:0>)			_	_	_	0000
AUXCON1	0C3E	HRPDIS	HRDDIS	—	_	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: ANALOG COMPARATOR REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMP1CON	0540	CMPON	—	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE	INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE	0000
CMP1DAC	0542		—	_	—						CMREF	<11:0>						0000
CMP2CON	0544	CMPON	_	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE	INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE	0000
CMP2DAC	0546	_	_	_	_	CMREF<11:0>						0000						
CMP3CON	0548	CMPON	_	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE	INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE	0000
CMP3DAC	054A		—	—	-						CMREF	<11:0>						0000
CMP4CON	054C	CMPON	_	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE	INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE	0000
CMP4DAC	054E	_	_	_	_						CMREF	<11:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-27: JTAG INTERFACE REGISTER MAP

SFR Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	_	_	_	_						JDATA	H<11:0>						xxxx
JDATAL	0FF2								JDATA	L<15:0>								0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	_	_	VREGSF	_	CM	VREGS
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0
Legend:							
R = Reada	ble bit	W = Writable b	bit	U = Unimplen	nented bit, read	1 as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	TRAPR: Trap	Reset Flag bit					
	1 = A Trap Co 0 = A Trap Co	onflict Reset has onflict Reset has	s occurred s not occurre	ed			
bit 14	IOPUWR: Ille	gal Opcode or I	Jninitialized	W Register Acc	ess Reset Flag	g bit	
	1 = An illega	l opcode detec	tion, an illeg	gal address mo	ode or Uninitia	lized W registe	er used as an
	Address	Pointer caused	a Reset	agistar Pasat h	as not occurre	4	
bit 13-12	Unimplemen	ted: Read as '(, ,	egister Reset fi		,	
bit 10 12	VREGSE: Fla	ish Voltage Rec	, Iulator Stand	by During Sleer	o bit		
	1 = Flash vol	tage regulator i	s active durir	ng Sleep			
	0 = Flash vol	tage regulator g	goes into Sta	ndby mode duri	ing Sleep		
bit 10	Unimplemen	ted: Read as '0)'				
bit 9	CM: Configur	ation Mismatch	Flag bit				
	1 = A Configu 0 = A Configu	ration Mismatc ration Mismatc	h Reset has h Reset has	occurred. not occurred			
bit 8	VREGS: Volta	age Regulator S	Standby Durir	ng Sleep bit			
	1 = Voltage r	egulator is activ	e during Sle	ep			
bit 7	0 = Voltage r	egulator goes in	$\frac{10}{2}$ Din hit	mode during Sie	eep		
	$1 = \Delta$ Master	Clear (nin) Res	t) FILLDIL et has occur	red			
	0 = A Master	Clear (pin) Res	et has not oc	curred			
bit 6	SWR: Softwa	re reset (Instr	uction) Flag	bit			
	1 = A RESET 0 = A RESET	instruction has instruction has	been execute not been exe	ed ecuted			
bit 5	SWDTEN: So	oftware Enable/I	Disable of W	DT bit ⁽²⁾			
	1 = WDT is e	nabled					
	0 = WDT is di	isabled					
bit 4	WDTO: Watch	hdog Timer Tim	e-out Flag bi	it			
	1 = WDT time 0 = WDT time	e-out has occurr e-out has not oc	curred				
Note 1:	All of the Reset sta	itus bits can be	set or cleare	d in software. S	etting one of th	ese bits in softw	vare does not
2:	If the WDTEN<1:0	 Configuration 	bits are '11'	(unprogramme	d), the WDT is	always enabled	d, regardless

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

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of the SWDTEN bit setting.

9.0 POWER-SAVING FEATURES

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS50X family devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXGS50X family devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- · Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

EXAMPLE 9-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV #SLEEP_MODE ; Put the device into Sleep mode
PWRSAV #IDLE_MODE ; Put the device into Idle mode

9.1 Clock Frequency and Clock Switching

The dsPIC33EPXXGS50X family devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 8.0 "Oscillator Configuration"**.

9.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXGS50X family devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 9-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

REGISTER 9-2. FMD2. FERIFIERAL MODULE DISABLE CONTROL REGISTER	EGISTER 9-2:	PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2
--	--------------	--

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD
bit 15						•	bit 8
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD
bit 7							bit 0
Legend:							
P = Peadat	ole hit	W - Writable	hit	II – Unimpler	mented bit rea	d as '0'	
n = Value a		'1' = Bit is set	Dit	0' = Bit is clearly	ared	v – Bitis unkn	own
					areu		own
bit 15-12	Unimplemer	nted: Read as '	0'				
bit 11	IC4MD: Inpu	t Capture 4 Mo	dule Disable bi	t			
	1 = Input Ca	oture 4 module	is disabled				
	0 = Input Ca	oture 4 module	is enabled				
bit 10	IC3MD: Inpu	t Capture 3 Mo	dule Disable bi	t			
	1 = Input Cap	oture 3 module	is disabled				
		oture 3 module	is enabled				
bit 9		t Capture 2 Mo	dule Disable bi	t			
	$\perp = $ Input Cap 0 = Input Cap	oture 2 module	is disabled				
bit 8	IC1MD: Input	t Capture 1 Mo	dule Disable bi	t			
	1 = Input Car	oture 1 module	is disabled	•			
	0 = Input Ca	oture 1 module	is enabled				
bit 7-4	Unimplemer	nted: Read as '	0'				
bit 3	OC4MD: Out	put Compare 4	Module Disab	le bit			
	1 = Output C	ompare 4 modu	ule is disabled				
	0 = Output C	ompare 4 modu	ule is enabled				
bit 2	OC3MD: Out	put Compare 3	Module Disab	le bit			
	1 = Output C	ompare 3 modu	ule is disabled				
bit 1		ompare 5 mout	Module Disab	le hit			
		ompare 2 modu	ile is disabled				
	0 = Output C	ompare 2 modu	le is enabled				
bit 0	OC1MD: Out	tput Compare 1	Module Disab	le bit			
	1 = Output C	ompare 1 modu	ule is disabled				
	0 = Output C	ompare 1 modu	ule is enabled				

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	_	CMP4MD	CMP3MD	CMP2MD	CMP1MD
bit 15		•			•		bit 8
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	_			_		PGA1MD	
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	oit	U = Unimplem	nented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15-12	Unimplemen	ted: Read as ')'				
bit 11	CMP4MD: CN	/IP4 Module Dis	sable bit				
	1 = CMP4 mc	dule is disable	d				
L:1 10) aabla bit				
DIT 10		/IP3 MOdule Di					
	1 = CMP3 md 0 = CMP3 md	dule is enable	1				
bit 9	CMP2MD: CN	/IP2 Module Di	sable bit				
	1 = CMP2 mc	dule is disable	d				
	0 = CMP2 mo	dule is enabled	t				
bit 8	CMP1MD: CN	/IP1 Module Dis	sable bit				
	1 = CMP1 mc	dule is disable	d				
	0 = CMP1 mc	dule is enabled					
bit 7-2	Unimplemen	ted: Read as ')'				
bit 1	PGA1MD: PG	SA1 Module Dis	able bit				
	1 = PGA1 mo 0 = PGA1 mo	dule is disabled	נ				
hit 0		ted. Read as '	י ז'				
	ommplemen	ieu. Neau as	,				

REGISTER 9-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP61R5	RP61R4	RP61R3	RP61R2	RP61R1	RP61R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP60R5	RP60R4	RP60R3	RP60R2	RP60R1	RP60R0
							1.11.0

|--|

Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP61R<5:0>: Peripheral Output Function is Assigned to RP61 Output Pin bits (see Table 10-2 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP60R<5:0>: Peripheral Output Function is Assigned to RP60 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-35: RPOR15: PERIPHERAL PIN SELECT OUTPUT REGISTER 15

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—		RP63R5	RP63R4	RP63R3	RP63R2	RP63R1	RP63R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP62R5	RP62R4	RP62R3	RP62R2	RP62R1	RP62R0
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimplemented bit, read as '0'			
-n = Value at POR '1' = Bit is se				'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP63R<5:0>:** Peripheral Output Function is Assigned to RP63 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **RP62R<5:0>:** Peripheral Output Function is Assigned to RP62 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 0

REGISTER 15-24: LEBCONX: PWMx LEADING-EDGE BLANKING (LEB) CONTROL REGISTER (x = 1 to 5)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_	
bit 15	bit 8							
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
		BCH ⁽¹⁾	BCL ⁽¹⁾	BPHH	BPHL	BPLH	BPLL	
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' n = Velue et BOR (1' = Rit is get (0' = Rit is gleared very = Rit is upknown)								
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown								
bit 15 PHR: PWMxH Rising Edge Trigger Enable bit								
	1 = Rising edge of PWMxH will trigger the Leading-Edge Blanking counter							
	0 = Leading-E	dge Blanking i	gnores the risi	ng edge of PW	MxH			
bit 14	PHF: PWMxH Falling Edge Trigger Enable bit							
	\perp = Failing edge of PWMXH will trigger the Leading-Edge Blanking counter 0 = Leading-Edge Blanking ignores the falling edge of PWMxH							
bit 13	PLR: PWMxL Rising Edge Trigger Enable bit							
	1 = Rising edge of PWMxL will trigger the Leading-Edge Blanking counter							
	0 = Leading-Edge Blanking ignores the rising edge of PWMxL							
bit 12	PLF: PWMxL Falling Edge Trigger Enable bit							
	1 = Falling edge of PWMxL will trigger the Leading-Edge Blanking counter							
bit 11	0 = Leading-Edge Blanking ignores the falling edge of PWMxL							
	FLTLEBEN: Fault Input Leading-Edge Blanking Enable bit							
	 1 = Leading-Edge Blanking is applied to the selected Fault input 0 = Leading-Edge Blanking is not applied to the selected Fault input 							
bit 10	CLLEBEN: C	urrent-Limit Lea	ading-Edge Bla	anking Enable I	oit			
	1 = Leading-E 0 = Leading-E	dge Blanking i dge Blanking i	s applied to the s not applied to	e selected curre the selected o	ent-limit input current-limit inp	ut		
bit 9-6	Unimplement	ted: Read as '0)'					
bit 5	BCH: Blankin	g in Selected B	lanking Signal	High Enable b	it ⁽¹⁾			
	1 = State blan 0 = No blankir	king (of current	-limit and/or Fa	ault input signa signal is high	ls) when the se	elected blanking	g signal is high	
bit 4	BCL: Blanking	a in Selected B	lanking Signal	Low Enable bit	(1)			
	1 = State blan	king (of curren	t-limit and/or F	ault input signa	ls) when the se	elected blanking	g signal is low	
	0 = No blankir	ng when the se	lected blanking	g signal is low				
bit 3	BPHH: Blanki	ng in PWMxH	High Enable bi	t				
	1 = State blan 0 = No blankir	king (of curren ng when the PV	t-limit and/or F VMxH output i	ault input signa s high	ls) when the P	WMxH output i	s high	
bit 2	BPHL: Blanki	ng in PWMxH I	ow Enable bit					
	1 = State blan 0 = No blankir	king (of curren ng when the PV	t-limit and/or F VMxH output is	ault input signa s low	ls) when the P	WMxH output i	s low	

Note 1: The blanking signal is selected via the BLANKSEL<3:0> bits in the AUXCONx register.

REGISTER 19-8: ADCON4H: ADC CONTROL REGISTER 4 HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| C3CHS1 | C3CHS0 | C2CHS1 | C2CHS0 | C1CHS1 | C1CHS0 | C0CHS1 | C0CHS0 |
| bit 7 | | | | | | | bit 0 |

Legend:								
R = Readable	e bit	W = Writable bit	U = Unimplemented bit, read	d as '0'				
-n = Value at	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				
bit 15-8	Unimplemented: Read as '0'							
bit 7-6	C3CHS<1:0>: Dedicated ADC Core 3 Input Channel Selection bits							
	1x = Reserved 01 = AN15 (differential negative input when DIFF3 (ADMOD0L<7>) = 1) 00 = AN3							
bit 5-4	C2CHS<1:0>: Dedicated ADC Core 2 Input Channel Selection bits							
	11 = Reserved 10 = VREF Band Gap 01 = AN11 (differential negative input when DIFF2 (ADMOD0L<5>) = 1) 00 = AN2							
bit 3-2	C1CHS<1:0>	: Dedicated ADC Core 1 Inpu	t Channel Selection bits					
	11 = AN1ALT 10 = PGA2 01 = AN18 (differential negative input when DIFF1 (ADMOD0L<3>) = 1) 00 = AN1							
bit 1-0	COCHS<1:0> 11 = AN0ALT 10 = PGA1 01 = AN7 (dif 00 = AN0	: Dedicated ADC Core 0 Inpu	t Channel Selection bits DIFF0 (ADMOD0L<1>) = 1)					

R-0, HSC	<u>U-0</u>	<u>U-0</u>	U-0	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	
SHRRDY	—	_	—	C3RDY	C2RDY	C1RDY	CORDY	
bit 15							bit 8	
R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
SHRPWR			—	C3PWR	C2PWR	C1PWR	COPWR	
bit 7							bit 0	
Logondy			antad hit raa	d aa '0'				
R = Readable bit W = Writable bit HSC = Hardware Settable/Clearable bit								
R = Readable bit W = Writable bit HSC = Hardware Settable/Clearable bit 1^{2} = Nelue at POP (1) = Rit is set (0) = Rit is cleared x = Rit is unknown					014/0			
	-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown						Own	
bit 15	hit 15 SUPPRY: Sharad ADC Care Ready Eleg hit							
bit 10	1 = ADC core	is powered an	d ready for on	eration				
	0 = ADC core	e is not ready fo	r operation	oradori				
bit 14-12	Unimplemen	ted: Read as 'd)'					
bit 11	C3RDY: Dedicated ADC Core 3 Ready Flag bit							
	1 = ADC core is powered and ready for operation							
	0 = ADC core is not ready for operation							
bit 10	C2RDY: Dedicated ADC Core 2 Ready Flag bit							
	 1 = ADC core is powered and ready for operation 0 = ADC core is not ready for operation 							
bit 9	C1RDY: Dedicated ADC Core 1 Ready Flag bit							
	1 = ADC core is powered and ready for operation							
	0 = ADC core is not ready for operation							
bit 8	CORDY: Dedicated ADC Core 0 Ready Flag bit							
	1 = ADC core is powered and ready for operation							
L:1 7		e is not ready to	r operation					
DIT 7		hared ADC Cor	e x Power Ena	adie dit				
	0 = ADC Core	e x is off						
bit 6-4	Unimplemen	ted: Read as 'd)'					
bit 3	C3PWR: Ded	licated ADC Co	re 3 Power Er	nable bit				
	1 = ADC core	e is powered						
	0 = ADC core	e is off						
bit 2	C2PWR: Ded	licated ADC Co	re 2 Power Er	nable bit				
	1 = ADC core	e is powered						
bit 1	C1PWR: Ded	licated ADC Co	re 1 Power Fr	hable bit				
	1 = ADC core	is powered						
	0 = ADC core	e is off						
bit 0	COPWR: Ded	licated ADC Co	re 0 Power Er	nable bit				
	1 = ADC core	is powered						
	0 = ADC core	e is off						

REGISTER 19-9: ADCON5L: ADC CONTROL REGISTER 5 LOW

REGISTER 19-10: ADCON5H: ADC CONTROL REGISTER 5 HIGH

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
	—	—	—	WARMTIME3	WARMTIME2	WARMTIME1	WARMTIME0			
bit 15							bit 8			
R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0			
SHRCIE	—	C3CIE C2CIE C1CIE C0CIE								
bit 7							bit 0			
Legend:										
Legend: D = D = D = d = b = b = b = b = b = b = b = b = b										
R = Readable bit W = Writable bit			bit	U = Unimplem	ented bit, read	as '0'				
-n = Value at	-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is				x = Bit is unkn	own				
DIT 15-12	Unimplemen	ted: Read as								
DIT 11-8		<3:0>: ADC De		x Power-up Del	ay Dits	an Cleak Daria				
	for all ADC co	res	wer-up delay		i the Core Sour	Ce Clock Perio	us (ICORESRC)			
	tor all ADC cores. 1111 = 32768 Source Clock Periods									
	1110 = 16384 Source Clock Periods									
	 1101 = 8192 Source Clock Periods 1100 = 4096 Source Clock Periods 1011 = 2048 Source Clock Periods 1010 = 1024 Source Clock Periods 1001 = 512 Source Clock Periods 									
	1000 = 256 Source Clock Periods									
	0111 = 128 Source Clock Periods									
	0110 = 64 Sc	ource Clock Pe	eriods							
	0101 = 32 So	ource Clock Pe	eriods							
	0100 = 16 Source Clock Periods									
bit 7	SHRCIE: Sha	ared ADC Core	e Ready Comr	non Interrupt Er	nable bit					
	1 = Common	interrupt will b	e generated w	hen ADC core	is powered and	ready for oper	ation			
	0 = Common	interrupt is dis	abled for an A	DC core ready	event					
bit 6-4	Unimplemen	ted: Read as	ʻ0'							
bit 3	C3CIE: Dedic	cated ADC Cor	e 3 Ready Co	mmon Interrupt	Enable bit					
	1 = Common	interrupt will b	e generated w	hen ADC Core	3 is powered a	nd ready for op	eration			
h :# 0				DC Core 3 read	uy event					
DIL 2		interrunt will h	e z Ready Co			nd roady for on	aration			
	1 = Common 0 = Common	interrupt will b	abled for an A	DC Core 2 rea	dv event	nu ready for op	eration			
bit 1	C1CIE: Dedic	cated ADC Cor	e 1 Ready Co	mmon Interrupt	Enable bit					
	1 = Common	interrupt will b	e generated w	hen ADC Core	1 is powered a	nd ready for on	eration			
	0 = Common	interrupt is dis	abled for an A	DC Core 1 read	dy event	, - -				
bit 0	COCIE: Dedic	cated ADC Cor	e 0 Ready Co	mmon Interrupt	Enable bit					
	1 = Common	interrupt will b	e generated w	hen ADC Core	0 is powered a	nd ready for op	eration			
	0 = Common	interrupt is dis	abled for an A	DC Core 0 read	dv event					

REGISTER 19-17: ADEISTATL: ADC EARLY INTERRUPT STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			EIST	AT<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			EIST	AT<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimplen	nplemented bit, read as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown

bit 15-0 EISTAT<15:0>: Early Interrupt Status for Corresponding Analog Inputs bits

1 = Early interrupt was generated

0 = Early interrupt was not generated since the last ADCBUFx read

REGISTER 19-18: ADEISTATH: ADC EARLY INTERRUPT STATUS REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	_		_
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				EISTAT	<21:16>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0 EISTAT<21:16>: Early Interrupt Status for Corresponding Analog Inputs bits

1 = Early interrupt was generated

0 = Early interrupt was not generated since the last ADCBUFx read

23.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXGS50X family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Emulation
- Brown-out Reset (BOR)

23.1 Configuration Bits

In dsPIC33EPXXGS50X family devices, the Configuration Words are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the end of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 23-1 with detailed descriptions in Table 23-2. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration Shadow registers during device Resets.

For devices operating in Dual Partition modes, the BSEQx bits (FBTSEQ<11:0>) determine which panel is the Active Partition at start-up and the Configuration Words from that panel are loaded into the Configuration Shadow registers.

Note:	Configuration data is reloaded on all types
	of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Words for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled. Program code executing out of configuration space will cause a device Reset.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Words.

TABLE 23-1: CONFIGURATION REGISTER MAP⁽³⁾ (CONTINUED)

Name	Address	Device Memory Size (Kbytes)	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FDEVOPT	002BAC	16																	
	0057AC	32	_	_	_	_	_	_	_	_	_	_	DBCC	_	ALTI2C2	ALTI2C1	Reserved ⁽¹⁾	_	PWMLOCH
	00AFAC	64																	
FALTREG	002BB0	16																	
	0057B0	32	_	_	_	_	_	_	_	_	_	-		CTXT2<2:	0>	—	c	CTXT1<2:0	>
	00AFB0	64																	
FBTSEQ	002BFC	16								•	•								
	0057FC	32		IBSE	EQ<11:0>								I	BSEQ<11:0	>				
	00AFFC	64																	
FBOOT ⁽⁴⁾	801000	—	_	_		_	_	_		_	_	_	—		_	_	_	BTMC	DDE<1:0>

Note 1: These bits are reserved and must be programmed as '1'.

2: This bit is reserved and must be programmed as '0'.

3: When operating in Dual Partition mode, each partition will have dedicated Configuration registers. On a device Reset, the configuration values of the Active Partition are read at start-up, but during a soft swap condition, the configuration settings of the newly Active Partition are ignored.

4: FBOOT resides in configuration memory space.

DC CH	ARACTE	RISTICS	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions	
DI60a	licl	Input Low Injection Current	0	_	₋₅ (5,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7	
DI60b	Іісн	Input High Injection Current	0	_	+5 ^(6,7,8)	mA	All pins excep <u>t VDD,</u> VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins ⁽⁷⁾	
DI60c	∑lict	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁹⁾	_	+20 ⁽⁹⁾	mA	Absolute instantaneous sum of all \pm input injection currents from all I/O pins (IICL + IICH) $\leq \sum$ IICT	

TABLE 26-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 3: Negative current is defined as current sourced by the pin.
- 4: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 5: VIL Source < (Vss 0.3). Characterized but not tested.
- 6: VIH Source > (VDD + 0.3) for pins that are not 5V tolerant only.
- 7: Digital 5V tolerant pins do not have internal high-side diodes to VDD and cannot tolerate any "positive" input injection current.
- 8: Injection Currents > | 0 | can affect the ADC results by approximately 4-6 counts.
- **9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

- (1)



TABLE 26-24:	TIMER1 EXTERNAL CLOCK	

АС СН	ARACTERIS	STICS		Standard Ope (unless other Operating tem	erating (wise sta perature	tated) re $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param No.	Symbol	Charao	cteristic ⁽²⁾	Min.	Тур.	Max.	Units	Conditions		
TA10	T⊤xH	T1CK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N		_	ns	Must also meet Parameter TA15, N = Prescale Value (1, 8, 64, 256)		
			Asynchronous	35	—	—	ns			
TA11	ΤτxL	T1CK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TA15, N = Prescale Value (1, 8, 64, 256)		
			Asynchronous	10	_	—	ns			
TA15	ΤτχΡ	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	_	_	ns	N = Prescale Value (1, 8, 64, 256)		
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC	_	50	kHz			
TA20	TCKEXTMRL	Delay from E Clock Edge t Increment	xternal T1CK o Timer	0.75 Tcy + 40		1.75 Tcy + 40	ns			

Note 1: Timer1 is a Type A timer.

2: These parameters are characterized but not tested in manufacturing.



FIGURE 26-17: SPIX SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

AC/DC	CHARAC	TERISTICS ⁽¹⁾		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteris	tic	Min.	Тур.	Max.	Units	Comments
PA01	Vin	Input Voltage Rang	е	AVss - 0.3	_	AVDD + 0.3	V	
PA02	Vсм	Common-Mode Inp Voltage Range	out	AVss	—	AVDD - 1.6	V	
PA03	Vos	Input Offset Voltage	Э	-10		10	mV	
PA04	Vos	Input Offset Voltage Drift with Temperature		_	±15	—	µV/∘C	
PA05	Rin+	Input Impedance of Positive Input		_	>1M 7 pF	—	Ω pF	
PA06	Rin-	Input Impedance of Negative Input	_	10K 7 pF	—	Ω pF		
PA07	Gerr	Gain Error		-2	_	2	%	Gain = 4x, 8x
				-3	—	3	%	Gain = 16x
				-4	—	4	%	Gain = 32x, 64x
PA08	Lerr	Gain Nonlinearity Error			_	0.5	%	% of full scale, Gain = 16x
PA09	IDD	Current Consumption			2.0	—	mA	Module is enabled with a 2-volt P-P output voltage swing
PA10a	BW	Small Signal	G = 4x		10	—	MHz	
PA10b		Bandwidth (-3 dB)	G = 8x		5	—	MHz	
PA10c			G = 16x	_	2.5	—	MHz	
PA10d			G = 32x		1.25		MHz	
PA10e			G = 64x	_	0.625	—	MHz	
PA11	OST	Output Settling Tim of Final Value	e to 1%	_	0.4	—	μs	Gain = 16x, 100 mV input step change
PA12	SR	Output Slew Rate		_	40	_	V/µs	Gain = 16x
PA13	TGSEL	Gain Selection Tim	е	_	1		μs	
PA14	TON	Module Turn On/Set	tting Time	_	_	10	μs	

TABLE 26-48: PGAx MODULE SPECIFICATIONS

Note 1: The PGAx module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

TABLE 26-49: CONSTANT-CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS ⁽¹⁾					$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions			
CC01	Idd	Current Consumption	_	30	—	μA				
CC02	IREG	Regulation of Current with Voltage On		±3	_	%				
CC03	IOUT	Current Output at Terminal	_	10	_	μA				

Note 1: The constant-current source module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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