Microchip Technology - DSPIC33EP16GS505T-I/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-TQFP Exposed Pad
Supplier Device Package	48-TQFP-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep16gs505t-i-pt

TABLE 4-11: PWM GENERATOR 4 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON4	0C80	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	MTBS	CAM	XPRES	IUE	0000
IOCON4	0C82	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON4	0C84	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC4	0C86	PWM4 Generator Duty Cycle Register (PDC4<15:0>)																0000
PHASE4	0C88	PWM4 Primary Phase-Shift or Independent Time Base Period Register (PHASE4<15:0>)																0000
DTR4	0C8A	—	—	PWM4 Dead-Time Register (DTR4<13:0>)														0000
ALTDTR4	0C8C	—	—	PWM4 Alternate Dead-Time Register (ALTDTR4<13:0>)														0000
SDC4	0C8E	PWM4 Secondary Duty Cycle Register (SDC4<15:0>)																0000
SPHASE4	0C90	PWM4 Secondary Phase-Shift Register (SPHASE4<15:0>)																0000
TRIG4	0C92	PWM4 Primary Trigger Compare Value Register (TRGCMP<12:0>)													—	—	—	0000
TRGCON4	0C94	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG4	0C96	PWM4 Secondary Trigger Compare Value Register (STRGCMP<12:0>)													—	—	—	0000
PWMCAP4	0C98	PWM4 Primary Time Base Capture Register (PWMCAP<12:0>)													—	—	—	0000
LEBCON4	0C9A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY4	0C9C	—	—	—	—	PWM4 Leading-Edge Blanking Delay Register (LEB<8:0>)									—	—	—	0000
AUXCON4	0C9E	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: PWM GENERATOR 5 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON5	0CA0	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	MTBS	CAM	XPRES	IUE	0000
IOCON5	0CA2	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON5	0CA4	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC5	0CA6	PWM5 Generator Duty Cycle Register (PDC5<15:0>)																0000
PHASE5	0CA8	PWM5 Primary Phase-Shift or Independent Time Base Period Register (PHASE5<15:0>)																0000
DTR5	0CAA	—	—	PWM5 Dead-Time Register (DTR5<13:0>)														0000
ALTDTR5	0CAC	—	—	PWM5 Alternate Dead-Time Register (ALTDTR5<13:0>)														0000
SDC5	0CAE	PWM5 Secondary Duty Cycle Register (SDC5<15:0>)																0000
SPHASE5	0CB0	PWM5 Secondary Phase-Shift Register (SPHASE5<15:0>)																0000
TRIG5	0CB2	PWM5 Primary Trigger Compare Value Register (TRGCMP<12:0>)													—	—	—	0000
TRGCON5	0CB4	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG5	0CB6	PWM5 Secondary Trigger Compare Value Register (STRGCMP<12:0>)													—	—	—	0000
PWMCAP5	0CB8	PWM5 Primary Time Base Capture Register (PWMCAP<12:0>)													—	—	—	0000
LEBCON5	0CBA	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY5	0CBC	—	—	—	—	PWM5 Leading-Edge Blanking Delay Register (LEB<8:0>)									—	—	—	0000
AUXCON5	0CBE	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 8-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-n (FRCDIVN)	Internal	xx	111	**1, 2**
Fast RC Oscillator with Divide-by-16	Internal	xx	110	**1**
Low-Power RC Oscillator (LPRC)	Internal	xx	101	**1**
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	**1**
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	**1**
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	**1**
Fast RC Oscillator (FRC)	Internal	xx	000	**1**

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

8.2 Auxiliary Clock Generation

The auxiliary clock generation is used for peripherals that need to operate at a frequency unrelated to the system clock, such as PWM or ADC.

The primary oscillator and internal FRC oscillator sources can be used with an Auxiliary PLL (APLL) to obtain the auxiliary clock. The Auxiliary PLL has a fixed 16x multiplication factor.

The auxiliary clock has the following configuration restrictions:

- For proper PWM operation, auxiliary clock generation must be configured for 120 MHz (see Parameter OS56 in **Section 26.0 “Electrical Characteristics”**). If a slower frequency is desired, the PWM Input Clock Prescaler (Divider) Select bits (PCLKDIV<2:0>) should be used.
- To achieve 1.04 ns PWM resolution, the auxiliary clock must use the 16x Auxiliary PLL (APLL). All other clock sources will have a minimum PWM resolution of 8 ns.
- If the primary PLL is used as a source for the auxiliary clock, the primary PLL should be configured up to a maximum operation of 30 MIPS or less.

8.3 Reference Clock Generation

The reference clock output logic provides the user with the ability to output a clock signal based on the system clock or the crystal oscillator on a device pin. The user application can specify a wide range of clock scaling prior to outputting the reference clock.

8.4 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

8.4.1 KEY RESOURCES

- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

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REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1) (CONTINUED)

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit(3)
1 = FSCM has detected a clock failure
0 = FSCM has not detected a clock failure

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Requests oscillator switch to the selection specified by the NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and will trigger an oscillator failure trap.

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REGISTER 9-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CMP4MD	CMP3MD	CMP2MD	CMP1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	PGA1MD	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **CMP4MD:** CMP4 Module Disable bit
1 = CMP4 module is disabled
0 = CMP4 module is enabled

bit 10 **CMP3MD:** CMP3 Module Disable bit
1 = CMP3 module is disabled
0 = CMP3 module is enabled

bit 9 **CMP2MD:** CMP2 Module Disable bit
1 = CMP2 module is disabled
0 = CMP2 module is enabled

bit 8 **CMP1MD:** CMP1 Module Disable bit
1 = CMP1 module is disabled
0 = CMP1 module is enabled

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **PGA1MD:** PGA1 Module Disable bit
1 = PGA1 module is disabled
0 = PGA1 module is enabled

bit 0 **Unimplemented:** Read as '0'

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REGISTER 10-18: RPINR42: PERIPHERAL PIN SELECT INPUT REGISTER 42

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT6R7	FLT6R6	FLT6R5	FLT6R4	FLT6R3	FLT6R2	FLT6R1	FLT6R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT5R7	FLT5R6	FLT5R5	FLT5R4	FLT5R3	FLT5R2	FLT5R1	FLT5R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **FLT6R<7:0>:** Assign PWM Fault 6 (FLT6) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

bit 7-0 **FLT5R<7:0>:** Assign PWM Fault 5 (FLT5) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

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REGISTER 10-26: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP45R5	RP45R4	RP45R3	RP45R2	RP45R1	RP45R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP44R5	RP44R4	RP44R3	RP44R2	RP44R1	RP44R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP45R<5:0>:** Peripheral Output Function is Assigned to RP45 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP44R<5:0>:** Peripheral Output Function is Assigned to RP44 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-27: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP47R5	RP47R4	RP47R3	RP47R2	RP47R1	RP47R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP46R5	RP46R4	RP46R3	RP46R2	RP46R1	RP46R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP47R<5:0>:** Peripheral Output Function is Assigned to RP47 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP46R<5:0>:** Peripheral Output Function is Assigned to RP46 Output Pin bits (see Table 10-2 for peripheral function numbers)

12.0 TIMER2/3 AND TIMER4/5

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with All 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare modules (Timer2 and Timer3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 12-1. T3CON and T5CON are shown in Register 12-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 12-2.

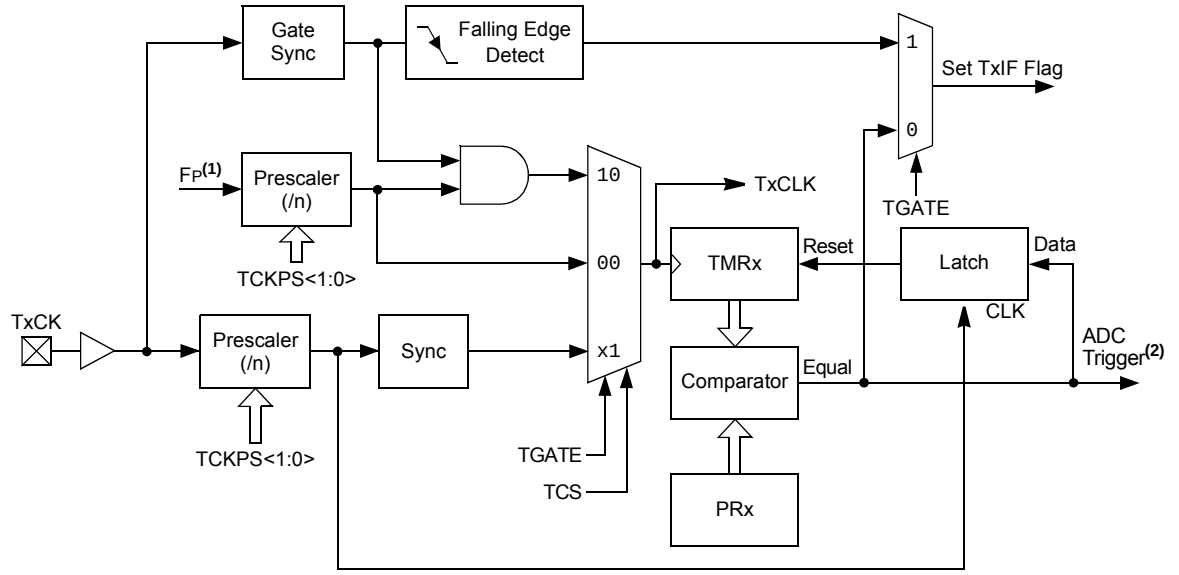
12.1 Timer Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

12.1.1 KEY RESOURCES

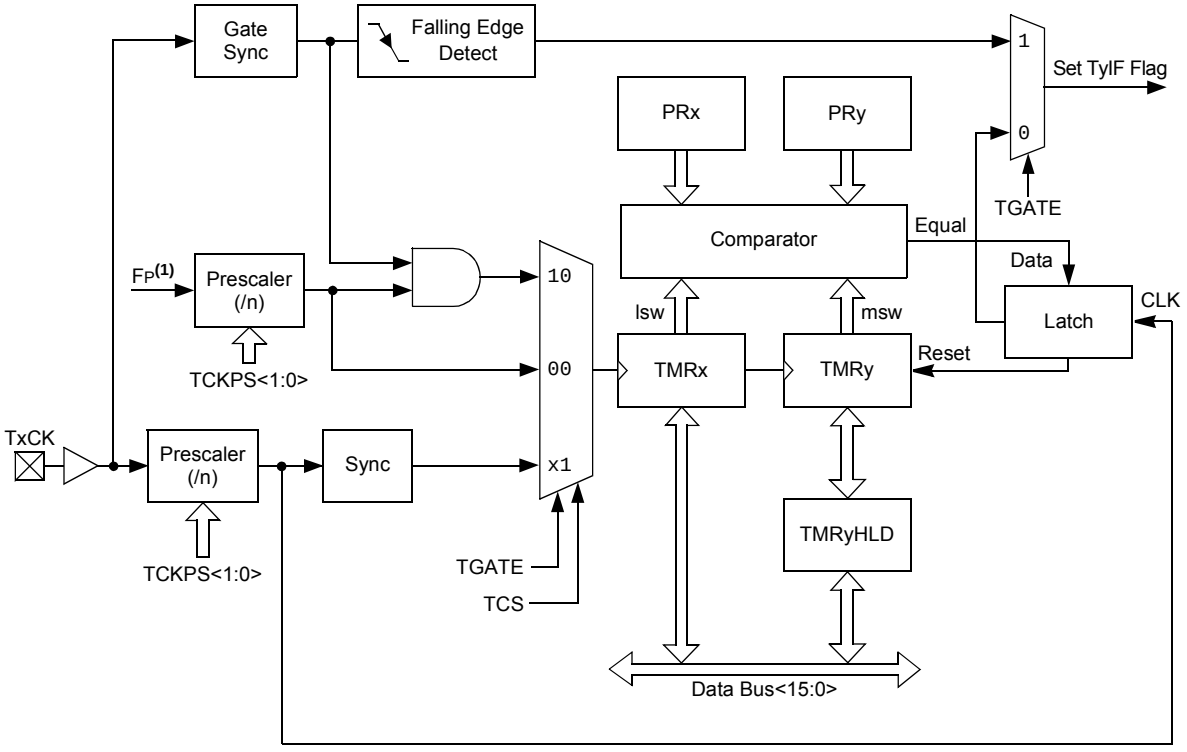
- **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

FIGURE 12-1: TIMERx BLOCK DIAGRAM (x = 2 THROUGH 5)



Note 1: FP is the peripheral clock.
2: The ADC trigger is only available on TMR2.

FIGURE 12-2: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



Note 1: Timerx is a Type B timer (x = 2 and 4).
2: Timery is a Type C timer (y = 3 and 5).

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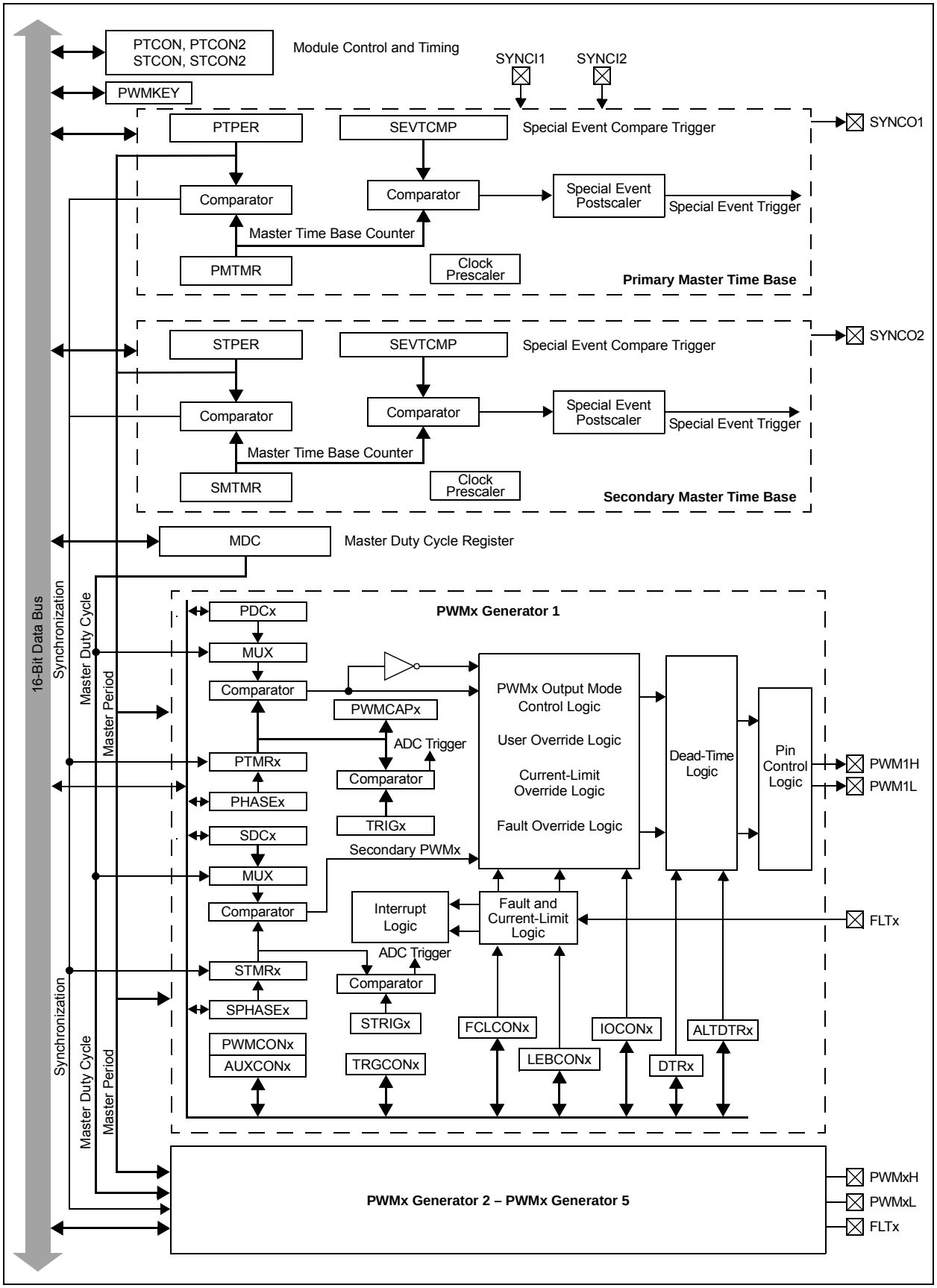
FIGURE 15-2: SIMPLIFIED CONCEPTUAL BLOCK DIAGRAM OF THE HIGH-SPEED PWM



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REGISTER 15-24: LEBCONx: PWMx LEADING-EDGE BLANKING (LEB) CONTROL REGISTER (x = 1 to 5) (CONTINUED)

bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is high
0 = No blanking when the PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is low
0 = No blanking when the PWMxL output is low

Note 1: The blanking signal is selected via the BLANKSEL<3:0> bits in the AUXCONx register.

REGISTER 15-25: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER (x = 1 to 5)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	LEB<8:5>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
LEB<4:0>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-3 **LEB<8:0>:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits
The value is in 8.32 ns increments.

bit 2-0 **Unimplemented:** Read as ‘0’

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REGISTER 19-27: ADTRIGxH: ADC CHANNEL TRIGGER x SELECTION REGISTER HIGH (x = 0 to 5)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRC(4x+3)<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRC(4x+2)<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC(4x+3)<4:0>:** Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
11110 = Reserved
11101 = Reserved
11100 = PWM Generator 5 current-limit trigger
11011 = PWM Generator 4 current-limit trigger
11010 = PWM Generator 3 current-limit trigger
11001 = PWM Generator 2 current-limit trigger
11000 = PWM Generator 1 current-limit trigger
10111 = Output Compare 2 trigger
10110 = Output Compare 1 trigger
10101 = Reserved
10100 = Reserved
10011 = PWM Generator 5 secondary trigger
10010 = PWM Generator 4 secondary trigger
10001 = PWM Generator 3 secondary trigger
10000 = PWM Generator 2 secondary trigger
01111 = PWM Generator 1 secondary trigger
01110 = PWM secondary Special Event Trigger
01101 = Timer2 period match
01100 = Timer1 period match
01011 = Reserved
01010 = Reserved
01001 = PWM Generator 5 primary trigger
01000 = PWM Generator 4 primary trigger
00111 = PWM Generator 3 primary trigger
00110 = PWM Generator 2 primary trigger
00101 = PWM Generator 1 primary trigger
00100 = PWM Special Event Trigger
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

bit 7-5 **Unimplemented:** Read as '0'

REGISTER 19-27: ADTRIGxH: ADC CHANNEL TRIGGER x SELECTION REGISTER HIGH (x = 0 to 5) (CONTINUED)

bit 4-0 **TRGSRC(4x+2)<4:0>:** Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
11110 = Reserved
11101 = Reserved
11100 = PWM Generator 5 current-limit trigger
11011 = PWM Generator 4 current-limit trigger
11010 = PWM Generator 3 current-limit trigger
11001 = PWM Generator 2 current-limit trigger
11000 = PWM Generator 1 current-limit trigger
10111 = Output Compare 2 trigger
10110 = Output Compare 1 trigger
10101 = Reserved
10100 = Reserved
10011 = PWM Generator 5 secondary trigger
10010 = PWM Generator 4 secondary trigger
10001 = PWM Generator 3 secondary trigger
10000 = PWM Generator 2 secondary trigger
01111 = PWM Generator 1 secondary trigger
01110 = PWM secondary Special Event Trigger
01101 = Timer2 period match
01100 = Timer1 period match
01011 = Reserved
01010 = Reserved
01001 = PWM Generator 5 primary trigger
01000 = PWM Generator 4 primary trigger
00111 = PWM Generator 3 primary trigger
00110 = PWM Generator 2 primary trigger
00101 = PWM Generator 1 primary trigger
00100 = PWM Special Event Trigger
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

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REGISTER 19-32: ADCMPxENL: ADC DIGITAL COMPARATOR x CHANNEL ENABLE REGISTER LOW (x = 0 or 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPEN<15:8>							
bit 15							bit 8

R/W/0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CMPEN<15:0>:** Comparator Enable for Corresponding Input Channels bits
1 = Conversion result for corresponding channel is used by the comparator
0 = Conversion result for corresponding channel is not used by the comparator

REGISTER 19-33: ADCMPxENH: ADC DIGITAL COMPARATOR x CHANNEL ENABLE REGISTER HIGH (x = 0 or 1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CMPEN<21:16>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **CMPEN<21:16>:** Comparator Enable for Corresponding Input Channels bits
1 = Conversion result for corresponding channel is used by the comparator
0 = Conversion result for corresponding channel is not used by the comparator

REGISTER 20-1: CMPxCON: COMPARATOR x CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMPON	—	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	HC-0, HS	R/W-0	R/W-0	R/W-0
INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMPON:** Comparator Operating Mode bit
1 = Comparator module is enabled
0 = Comparator module is disabled (reduces power consumption)

bit 14 **Unimplemented:** Read as '0'

bit 13 **CMPSIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode.
0 = Continues module operation in Idle mode
If a device has multiple comparators, any CMPSIDL bit set to '1' disables all comparators while in Idle mode.

bit 12-11 **HYSSEL<1:0>:** Comparator Hysteresis Select bits
11 = 20 mV hysteresis
10 = 10 mV hysteresis
01 = 5 mV hysteresis
00 = No hysteresis is selected

bit 10 **FLTREN:** Digital Filter Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled

bit 9 **FCLKSEL:** Digital Filter and Pulse Stretcher Clock Select bit
1 = Digital filter and pulse stretcher operate with the PWM clock
0 = Digital filter and pulse stretcher operate with the system clock

bit 8 **DACOE:** DACx Output Enable bit
1 = DACx analog voltage is connected to the DACOUTx pin(1)
0 = DACx analog voltage is not connected to the DACOUTx pin

bit 7-6 **INSEL<1:0>:** Input Source Select for Comparator bits
If ALTINP = 0, Select from Comparator Inputs:
11 = Selects CMPxD input pin
10 = Selects CMPxC input pin
01 = Selects CMPxB input pin
00 = Selects CMPxA input pin
If ALTINP = 1, Select from Alternate Inputs:
11 = Reserved
10 = Reserved
01 = Selects PGA2 output
00 = Selects PGA1 output

Note 1: DACOUTx can be associated only with a single comparator at any given time. The software must ensure that multiple comparators do not enable the DACx output by setting their respective DACOE bit.

TABLE 24-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
74	SL	SL	f	f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
75	SUB	SUB	Acc	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
76	SUBB	SUBB	f	f = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	Wn = Wn – lit10 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	Wd = Wb – Ws – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
77	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
78	SUBBR	SUBBR	f	f = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	Wd = Ws – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
79	SWAP	SWAP.b	Wn	Wn = nibble swap Wn	1	1	None
		SWAP	Wn	Wn = byte swap Wn	1	1	None
80	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
81	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	5	None
82	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
83	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
84	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
85	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
86	ZE	ZE	Ws,Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

26.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EPXXGS50X family AC characteristics and timing parameters.

TABLE 26-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in **Section 26.1 "DC Characteristics"**.

FIGURE 26-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

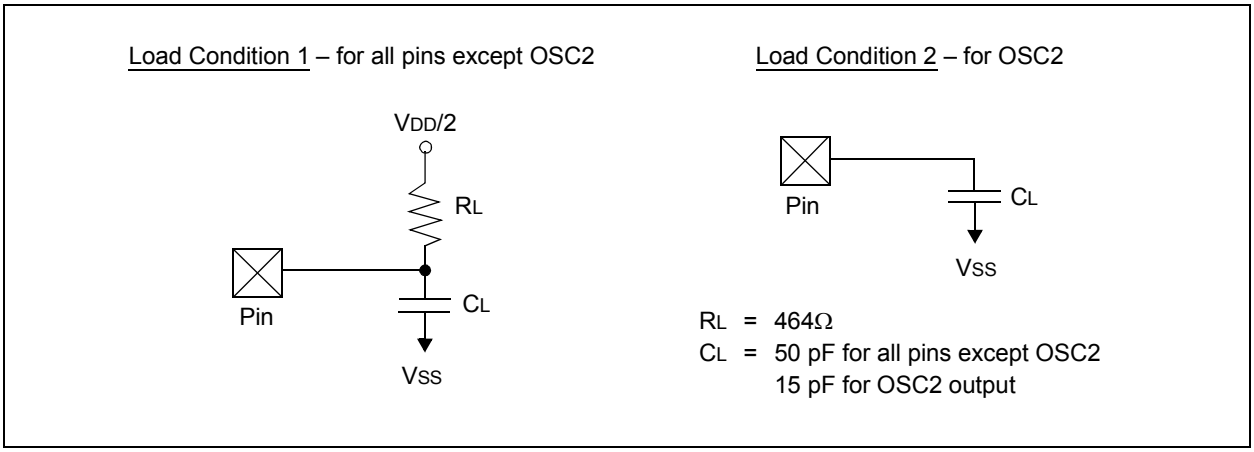

TABLE 26-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	COSCO	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	CIO	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

TABLE 26-43: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[5] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
ADC Accuracy: Single-Ended Input							
AD20b	Nr	Resolution	12			bits	
AD21b	INL	Integral Nonlinearity	> -3	—	< 3	LSb	AVSS = 0V, AVDD = 3.3V
AD22b	DNL	Differential Nonlinearity	> -1	—	< 1.5	LSb	AVSS = 0V, AVDD = 3.3V **(Note 2)**
AD23b	GERR	Gain Error (Dedicated Core)	> 5	13	< 20	LSb	AVSS = 0V, AVDD = 3.3V
		Gain Error (Shared Core)	> -1	5	< 10	LSb	
AD24b	EOFF	Offset Error (Dedicated Core)	> 2	10	< 18	LSb	AVSS = 0V, AVDD = 3.3V
		Offset Error (Shared Core)	> 2	8	< 15	LSb	
AD25b	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD31b	SINAD	Signal-to-Noise and Distortion	63	—	> 65	dB	**(Notes 3, 4)**
AD34b	ENOB	Effective Number of Bits	10.3	—	—	bits	**(Notes 3, 4)**

Note 1: These parameters are not characterized or tested in manufacturing.

2: No missing codes, limits based on characterization results.

3: These parameters are characterized but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

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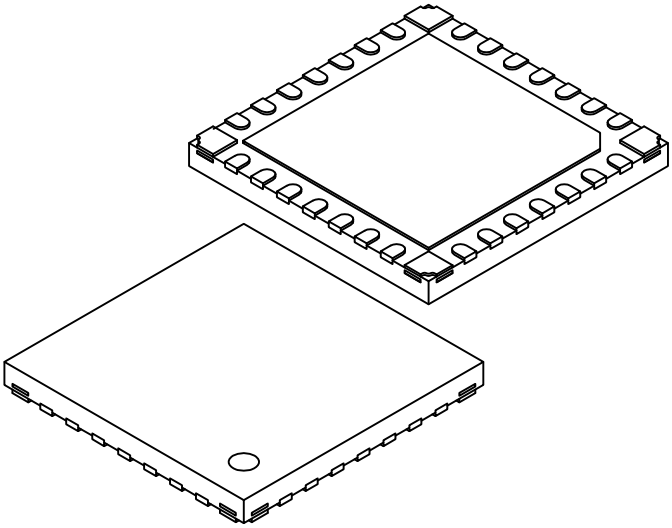
28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (2N) - 6x6x0.55 mm Body [UQFN] With 4.65x4.65 mm Exposed Pad and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.127 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.55	4.65	4.75
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.55	4.65	4.75
Exposed Pad Corner Chamfer	P	-	0.35	-
Terminal Width	b	0.25	0.30	0.35
Corner Anchor Pad	b1	0.35	0.40	0.43
Corner Pad, Metal Free Zone	b2	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

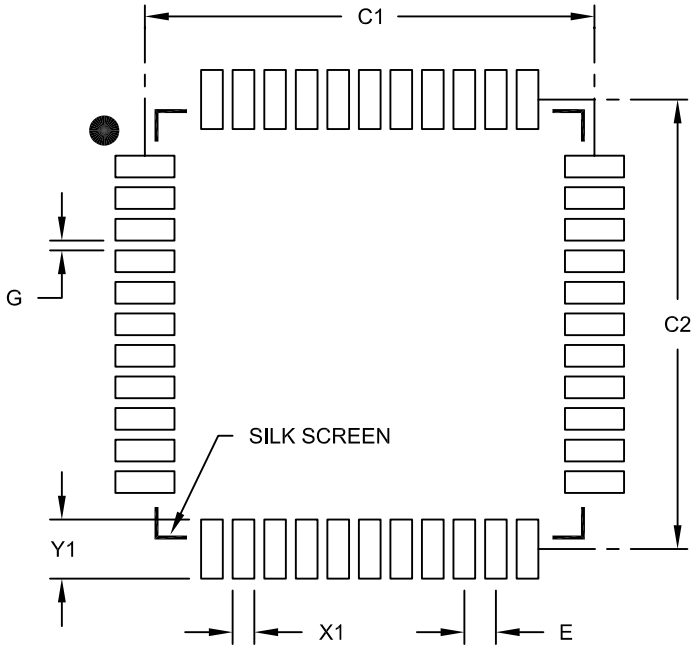
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-385B Sheet 2 of 2

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

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APPENDIX A: REVISION HISTORY

Revision A (June 2013)

This is the initial released version of the document.

Revision B (May 2015)

Adds dsPIC33EPXXGS505 (48-pin) devices to the document:

- Amends the table on page 2 to add the three new devices of this group
- Adds the 48-pin TQFP pin diagram on page 7
- Amends Table 26-3 to include thermal packaging characteristics for 48-pin packages
- Updates **Section 28.1 "Package Marking Information"** to include package marking details for 48-pin TQFP devices
- Updates **Section 28.2 "Package Details"** to include Microchip Drawings C04-183A and C04-2183A (7x7x1.0 mm 48-lead TQFP)

Changes all references to Dual Boot Flash Program Memory throughout the text to "Dual Partition Flash Program Memory". In addition, all accompanying references to "panels" and "Boot modes" are changed to "partitions" and "Partition modes". This includes, but is not limited, to:

- **Section 4.1 "Program Address Space"**
- **Section 5.4 "Dual Partition Flash Configuration"**, and Register 5-1
- **Section 23.10 "Code Protection and CodeGuard™ Security"**, and Table 23-2

Replaces the high-speed pipeline A/D Converter present in pre-production samples with a high-speed, multiple SAR A/D Converter in production devices:

- Replaces **Section 19.0 "High-Speed, 12-Bit Analog-to-Digital Converter (ADC)"** with an entirely new section of the same title, replacing all previous figures and registers
- Updates the summary bullet points under "High-Speed ADC Module" on Page 1 to reflect the feature set of the new module
- Updates Table 4-3 and Table 7-1 to reflect the new module's interrupt structure
- Replaces Table 4-16 with a new register map
- Removes Table 4-16 ("ADC Calibration Register Map"); subsequent tables are renumbered accordingly
- Updates **Section 23.2 "Device Calibration and Identification"** and Table 23-3 to remove the ADCAL registers from the Calibration register table
- Removes all references to the internal temperature sensor, including Table 26-44 (Temperature Sensor Specifications) and Figure 27-11 (Typical Temperature Sensor Voltage vs. Current)

Changes the ESR specification of the V_{CAP} filter capacitor from < 4Ω to < 0.5Ω.

Removes the internal voltage reference in all occurrences. For analog modules, the internal band gap reference is substituted as a replacement source.

Changes the following register names in all occurrences throughout the text:

- "CMPCONx" to "CMPxCON"
- "CMPDACx" to "CMPxDAC"
- "I2CxCON1" to "I2CxCONL"
- "I2CxCON2" to "I2CxCONH"

Updates the text of **Section 5.4.2 "Dual Partition Modes"** to change "Untrusted Dual Panel mode" to "Privileged Dual Partition mode" and clarifies the mode's code security features.

Changes the BSS2 Configuration bit to "BSEN" throughout the text.

Replaces **Section 23.3 "User OTP Memory"** with new text to describe the 64-word User OTP Memory space; also removes Table 23-4.

Amends Table 24-2 with a footnote indicating an increase of instruction execution cycles for most instructions under certain conditions.

Updates the following tables in **Section 26.0 "Electrical Characteristics"** (in addition to changes previously noted):

- Table 26-4, with new specification DC12 (and accompanying footnote)
- Table 26-6, with updated Typical and new Maximum data throughout, and the addition of Parameter DC27 (with accompanying footnote)
- Table 26-7, Table 26-8 and Table 26-10 with updated Typical and Maximum data throughout
- Table 26-9 with updated Typical and Maximum data for Parameters DC61a and DC61b
- Footnotes 6 and 7 of Table 26-11 to clarify the behavior of 5V tolerant pins
- The "ADC Accuracy" specifications of Table 26-43
- Table 26-45 (Table 26-45 in Revision A) with updated specifications for Parameter CM15
- Table 26-46 (Table 26-46 in Revision A) with updated specifications for Parameters DA03 through DA06

Clarifies the text of Footnotes 6 and 7 in Table 26-11 (I/O Pin Input Specifications).

Removes the "Reference Inputs" specifications from Table 26-43 in their entirety.

Replaces Figure 27-5 through Figure 27-10 with new characterization graphs to reflect the most current data and removes "TBD" watermarks.

Updates **Section 28.1 "Package Marking Information"** to reflect the removal of redundant temperature and package code information from all package markings; this is in addition to the new 48-pin package markings previously described.

Other minor typographic corrections throughout the document.