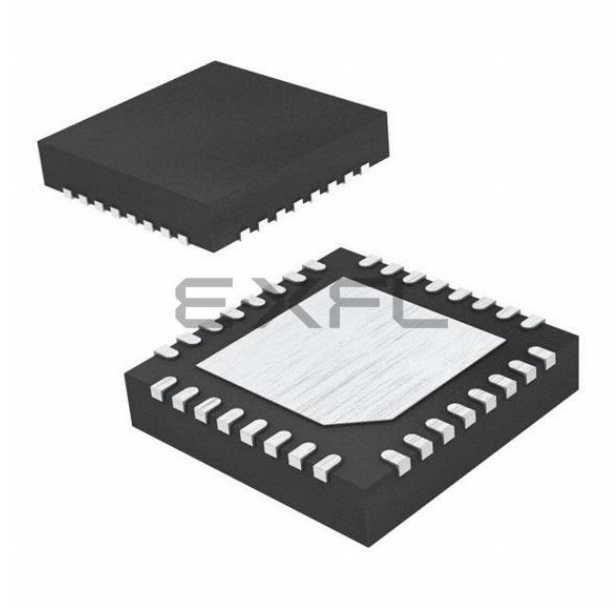
Microchip Technology - DSPIC33EP32GS502T-E/2N Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UQFN Exposed Pad
Supplier Device Package	28-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gs502t-e-2n

TABLE 4-23: PMD REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	ADCMD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	I2C2MD	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	—	—	—	0000
PMD6	076A	—	—	—	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	CMP4MD	CMP3MD	CMP2MD	CMP1MD	—	—	—	—	—	—	PGA1MD	—	0000
PMD8	076E	—	—	—	—	—	PGA2MD	ABGMD	—	—	—	—	—	—	—	CCSMD	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: CONSTANT-CURRENT SOURCE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ISRCCON	0500	ISRCEN	—	—	—	—	OUTSEL2	OUTSEL1	OUTSEL0	—	—	ISRCCAL5	ISRCCAL4	ISRCCAL3	ISRCCAL2	ISRCCAL1	ISRCCAL0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: PROGRAMMABLE GAIN AMPLIFIER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PGA1CON	0504	PGAEN	PGAOEN	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0	—	—	—	—	—	GAIN2	GAIN1	GAIN0	0000
PGA1CAL	0506	—	—	—	—	—	—	—	—	—	—	PGACAL<5:0>						0000
PGA2CON	0508	PGAEN	PGAOEN	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0	—	—	—	—	—	GAIN2	GAIN1	GAIN0	0000
PGA2CAL	050A	—	—	—	—	—	—	—	—	—	—	PGACAL<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PORTA REGISTER MAP FOR dsPIC33EPXXGS504/505 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>					001F
PORTA	0E02	—	—	—	—	—	—	—	—	—	—	—	RA<4:0>					0000
LATA	0E04	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0>					0000
ODCA	0E06	—	—	—	—	—	—	—	—	—	—	—	ODCA<4:0>					0000
CNENA	0E08	—	—	—	—	—	—	—	—	—	—	—	CNIEA<4:0>					0000
CNPUA	0E0A	—	—	—	—	—	—	—	—	—	—	—	CNPUA<4:0>					0000
CNPDA	0E0C	—	—	—	—	—	—	—	—	—	—	—	CNPDA<4:0>					0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSA<2:0>			0007

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31: PORTB REGISTER MAP FOR dsPIC33EPXXGS504/505 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB<15:0>																FFFF
PORTB	0E12	RB<15:0>																xxxx
LATB	0E14	LATB<15:0>																xxxx
ODCB	0E16	ODCB<15:0>																0000
CNENB	0E18	CNIEB<15:0>																0000
CNPUB	0E1A	CNPUB<15:0>																0000
CNPDB	0E1C	CNPDB<15:0>																0000
ANSELB	0E1E	—	—	—	—	—	ANSB<10:9>		—	ANSB<7:5>			—	ANSB<3:0>				06EF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PORTC REGISTER MAP FOR dsPIC33EPXXGS504/505 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	TRISC<13:0>														3FFF
PORTC	0E22	—	—	RC<13:0>														xxxx
LATC	0E24	—	—	LATC<13:0>														xxxx
ODCC	0E26	—	—	ODCC<13:0>														0000
CNENC	0E28	—	—	CNIEC<13:0>														0000
CNPUC	0E2A	—	—	CNPUC<13:0>														0000
CNPDC	0E2C	—	—	CNPDC<13:0>														0000
ANSELC	0E2E	—	—	—	ANSC<12:9>				—	—	ANSC<6:4>			—	ANSC<2:0>			1E77

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.7.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note:	The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed, but the contents of the register remain unchanged.

4.8 Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.8.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all of these situations are met:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^N$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note:	Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

8.1 CPU Clocking System

The dsPIC33EPXXGS50X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (FRCPLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

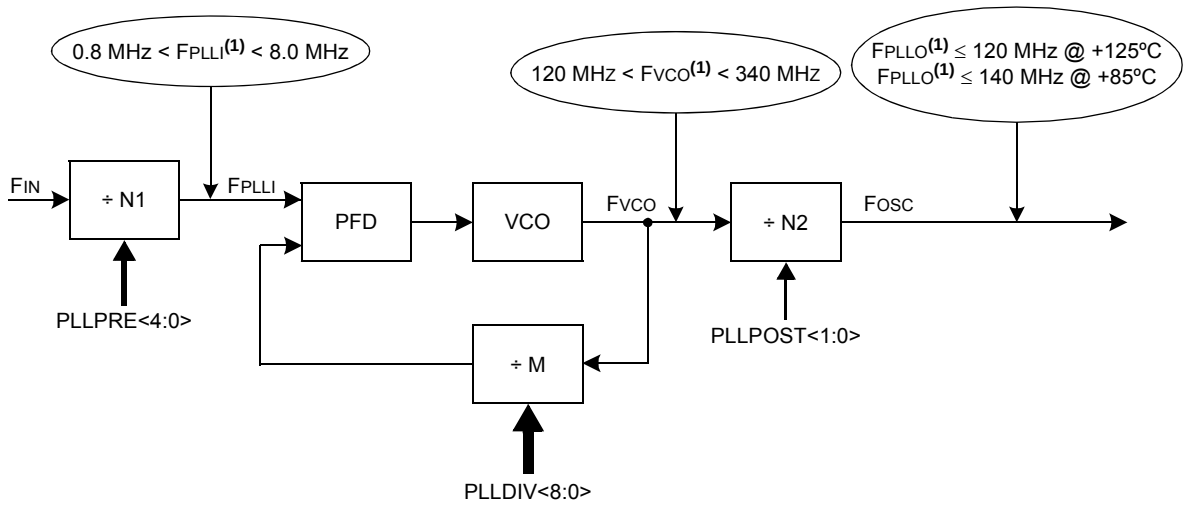
Instruction execution speed or device operating frequency, FCY, is given by Equation 8-1.

EQUATION 8-1: DEVICE OPERATING FREQUENCY

$$FCY = FOSC/2$$

Figure 8-2 is a block diagram of the PLL module. Equation 8-2 provides the relationship between Input Frequency (FIN) and Output Frequency (FPLLO). Equation 8-3 provides the relationship between Input Frequency (FIN) and VCO Frequency (FVCO).

FIGURE 8-2: PLL BLOCK DIAGRAM



Note 1: This frequency range must be met at all times.

EQUATION 8-2: FPLLO CALCULATION

$$FPLLO = FIN \times \left(\frac{M}{N1 \times N2}\right) = FIN \times \left(\frac{PLLDIV\langle 8:0\rangle + 2}{(PLLPRE\langle 4:0\rangle + 2) \times 2(PLLPOST\langle 1:0\rangle + 1)}\right)$$

Where:

$N1 = PLLPRE\langle 4:0\rangle + 2$

$N2 = 2 \text{ x } (PLLPOST\langle 1:0\rangle + 1)$

$M = PLLDIV\langle 8:0\rangle + 2$

EQUATION 8-3: FVCO CALCULATION

$$FVCO = FIN \times \left(\frac{M}{N1}\right) = FIN \times \left(\frac{PLLDIV\langle 8:0\rangle + 2}{(PLLPRE\langle 4:0\rangle + 2)}\right)$$

8.5 Oscillator Control Registers

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2(2)	NOSC1(2)	NOSC0(2)
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF(3)	—	—	OSWEN
bit 7							bit 0

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
1 = If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and PLL configurations may be modified
0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit
1 = I/O lock is active
0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Note 1: Writes to this register require an unlock sequence.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and will trigger an oscillator failure trap.

REGISTER 8-6: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3(1)	RODIV2(1)	RODIV1(1)	RODIV0(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference oscillator output is enabled on the RPn pin(2)
0 = Reference oscillator output is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
1 = Reference oscillator output continues to run in Sleep
0 = Reference oscillator output is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal is used as the reference clock
0 = System clock is used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits(1)
1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
2: This pin is remappable. See **Section 10.4 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 9-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **IC4MD:** Input Capture 4 Module Disable bit
1 = Input Capture 4 module is disabled
0 = Input Capture 4 module is enabled

bit 10 **IC3MD:** Input Capture 3 Module Disable bit
1 = Input Capture 3 module is disabled
0 = Input Capture 3 module is enabled

bit 9 **IC2MD:** Input Capture 2 Module Disable bit
1 = Input Capture 2 module is disabled
0 = Input Capture 2 module is enabled

bit 8 **IC1MD:** Input Capture 1 Module Disable bit
1 = Input Capture 1 module is disabled
0 = Input Capture 1 module is enabled

bit 7-4 **Unimplemented:** Read as '0'

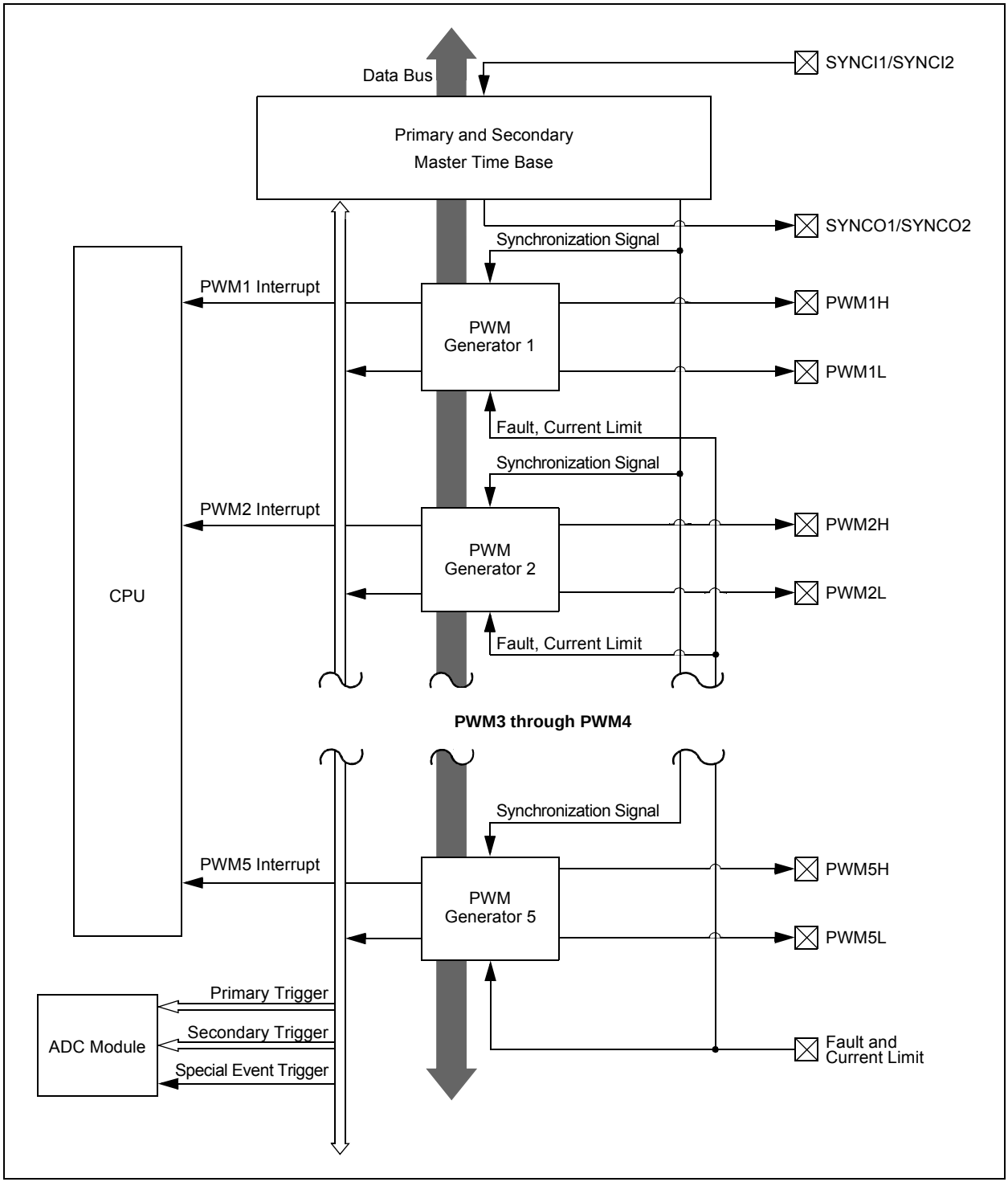
bit 3 **OC4MD:** Output Compare 4 Module Disable bit
1 = Output Compare 4 module is disabled
0 = Output Compare 4 module is enabled

bit 2 **OC3MD:** Output Compare 3 Module Disable bit
1 = Output Compare 3 module is disabled
0 = Output Compare 3 module is enabled

bit 1 **OC2MD:** Output Compare 2 Module Disable bit
1 = Output Compare 2 module is disabled
0 = Output Compare 2 module is enabled

bit 0 **OC1MD:** Output Compare 1 Module Disable bit
1 = Output Compare 1 module is disabled
0 = Output Compare 1 module is enabled

FIGURE 15-1: HIGH-SPEED PWM MODULE ARCHITECTURAL DIAGRAM



REGISTER 15-10: MDC: PWMx MASTER DUTY CYCLE REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **MDC<15:0>:** PWMx Master Duty Cycle Value bits

Note 1: The smallest pulse width that can be generated on the PWMx output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWMx period (0 to 40 ns, depending on the mode of operation), PWMx duty cycle resolution will increase from 1 to 3 LSBs.

REGISTER 15-11: PWMKEY: PWMx PROTECTION LOCK/UNLOCK KEY REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMKEY<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PWMKEY<15:0>:** PWMx Protection Lock/Unlock Key Value bits

REGISTER 15-19: TRGCONx: PWMx TRIGGER CONTROL REGISTER (x = 1 to 5)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTM(1)	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **TRGDIV<3:0>:** Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
1110 = Trigger output for every 15th trigger event
1101 = Trigger output for every 14th trigger event
1100 = Trigger output for every 13th trigger event
1011 = Trigger output for every 12th trigger event
1010 = Trigger output for every 11th trigger event
1001 = Trigger output for every 10th trigger event
1000 = Trigger output for every 9th trigger event
0111 = Trigger output for every 8th trigger event
0110 = Trigger output for every 7th trigger event
0101 = Trigger output for every 6th trigger event
0100 = Trigger output for every 5th trigger event
0011 = Trigger output for every 4th trigger event
0010 = Trigger output for every 3rd trigger event
0001 = Trigger output for every 2nd trigger event
0000 = Trigger output for every trigger event

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **DTM:** Dual Trigger Mode bit(1)

1 = Secondary trigger event is combined with the primary trigger event to create a PWM trigger
0 = Secondary trigger event is not combined with the primary trigger event to create a PWM trigger; two separate PWM triggers are generated

bit 6 **Unimplemented:** Read as '0'

bit 5-0 **TRGSTRT<5:0>:** Trigger Postscaler Start Enable Select bits

111111 = Wait 63 PWM cycles before generating the first trigger event after the module is enabled
•
•
•
000010 = Wait 2 PWM cycles before generating the first trigger event after the module is enabled
000001 = Wait 1 PWM cycle before generating the first trigger event after the module is enabled
000000 = Wait 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary PWMx generator cannot generate PWM trigger interrupts.

REGISTER 16-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit has started, SPIxTXB is empty

Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer Mode:
Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full
0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

NOTES:

REGISTER 17-2: I2CxCONH: I2Cx CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = I2CxRCV is updated and ACK is generated for a received address/data byte, ignoring the state of the I2COV only if the RBF bit = 0
0 = I2CxRCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled
If the rising edge of SCLx and SDAx is sampled low when the module is in a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte, the SCLREL (I2CxCONL<12>) bit will be cleared and SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte, the slave hardware clears the SCLREL (I2CxCONL<12>) bit and SCLx is held low
0 = Data holding is disabled

18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS50X family of devices contains two UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXGS50X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps in 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps in 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit Mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for all UARTx Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 18-1. The UARTx module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 18-1: UARTx SIMPLIFIED BLOCK DIAGRAM

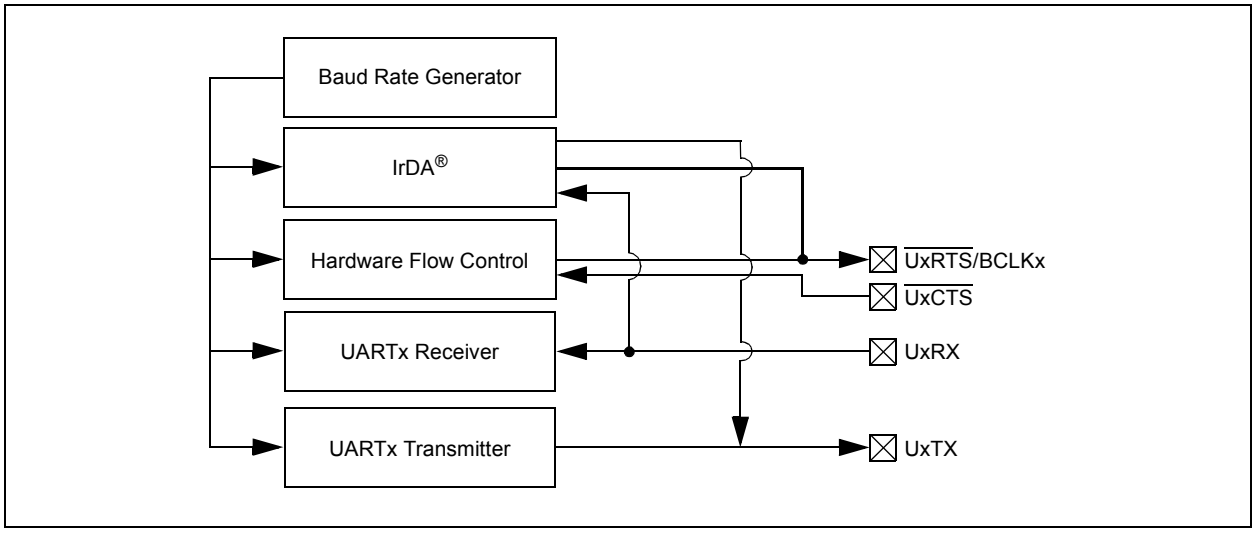


TABLE 24-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
48	MOV	MOV f,Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f,WREG	Move f to WREG	1	1	None
		MOV #lit16,Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b #lit8,Wn	Move 8-bit literal to Wn	1	1	None
		MOV Wn,f	Move Wn to f	1	1	None
		MOV Wso,Wdo	Move Ws to Wd	1	1	None
		MOV WREG,f	Move WREG to f	1	1	None
		MOV.D Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
49	MOVPAG	MOVPAG #lit10,DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG #lit8,TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAGW Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAGW Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
50	MOVSAC	MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB	Prefetch and store accumulator	1	1	None
51	MPY	MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
52	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
53	MSC	MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
54	MUL	MUL.SS Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb,Ws,Acc	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,Ws,Acc	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Acc	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb,Ws,Acc	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb,#lit5,Acc	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,Ws,Acc	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb,Ws,Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb,Ws,Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb,Ws,Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb,Ws,Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb,#lit5,Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 26-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(1) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage**	3.0	—	3.6	V	
DC12	VDR	**RAM Retention Voltage(2)**	1.8	—	—	V	-40ºC
			2	—	—		+25ºC, +85ºC, +125ºC
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1.0	—	—	V/ms	0V-3V in 3 ms

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, PGAs and comparators) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 26-13 for the minimum and maximum BOR values.

2: This is the limit to which VDD may be lowered and the RAM contents will always be retained.

TABLE 26-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
	CEFC	External Filter Capacitor Value(1)	4.7	10	—	μF	Capacitor must have a low series resistance (<1 ohm)

Note 1: Typical VCAP Voltage = 1.8 volts when VDD ≥ VDDMIN.

TABLE 26-38: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCKx Input Frequency	—	—	11	MHz	**(Note 3)**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ After SCKx Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 26-43: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[5] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
ADC Accuracy: Single-Ended Input							
AD20b	Nr	Resolution	12			bits	
AD21b	INL	Integral Nonlinearity	> -3	—	< 3	LSb	AVSS = 0V, AVDD = 3.3V
AD22b	DNL	Differential Nonlinearity	> -1	—	< 1.5	LSb	AVSS = 0V, AVDD = 3.3V **(Note 2)**
AD23b	GERR	Gain Error (Dedicated Core)	> 5	13	< 20	LSb	AVSS = 0V, AVDD = 3.3V
		Gain Error (Shared Core)	> -1	5	< 10	LSb	
AD24b	EOFF	Offset Error (Dedicated Core)	> 2	10	< 18	LSb	AVSS = 0V, AVDD = 3.3V
		Offset Error (Shared Core)	> 2	8	< 15	LSb	
AD25b	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD31b	SINAD	Signal-to-Noise and Distortion	63	—	> 65	dB	**(Notes 3, 4)**
AD34b	ENOB	Effective Number of Bits	10.3	—	—	bits	**(Notes 3, 4)**

Note 1: These parameters are not characterized or tested in manufacturing.

2: No missing codes, limits based on characterization results.

3: These parameters are characterized but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

TABLE 26-48: PGAx MODULE SPECIFICATIONS

AC/DC CHARACTERISTICS(1)				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
PA01	VIN	Input Voltage Range		AVSS – 0.3	—	AVDD + 0.3	V	
PA02	VCM	Common-Mode Input Voltage Range		AVSS	—	AVDD – 1.6	V	
PA03	VOS	Input Offset Voltage		-10	—	10	mV	
PA04	VOS	Input Offset Voltage Drift with Temperature		—	±15	—	µV/°C	
PA05	RIN+	Input Impedance of Positive Input		—	>1M || 7 pF	—	Ω|| pF	
PA06	RIN-	Input Impedance of Negative Input		—	10K || 7 pF	—	Ω|| pF	
PA07	GERR	Gain Error		-2	—	2	%	Gain = 4x, 8x
				-3	—	3	%	Gain = 16x
				-4	—	4	%	Gain = 32x, 64x
PA08	LERR	Gain Nonlinearity Error		—	—	0.5	%	% of full scale, Gain = 16x
PA09	IDD	Current Consumption		—	2.0	—	mA	Module is enabled with a 2-volt P-P output voltage swing
PA10a	BW	Small Signal Bandwidth (-3 dB)	G = 4x	—	10	—	MHz	
PA10b			G = 8x	—	5	—	MHz	
PA10c			G = 16x	—	2.5	—	MHz	
PA10d			G = 32x	—	1.25	—	MHz	
PA10e			G = 64x	—	0.625	—	MHz	
PA11	OST	Output Settling Time to 1% of Final Value		—	0.4	—	µs	Gain = 16x, 100 mV input step change
PA12	SR	Output Slew Rate		—	40	—	V/µs	Gain = 16x
PA13	TGSEL	Gain Selection Time		—	1	—	µs	
PA14	TON	Module Turn On/Setting Time		—	—	10	µs	

Note 1: The PGAx module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

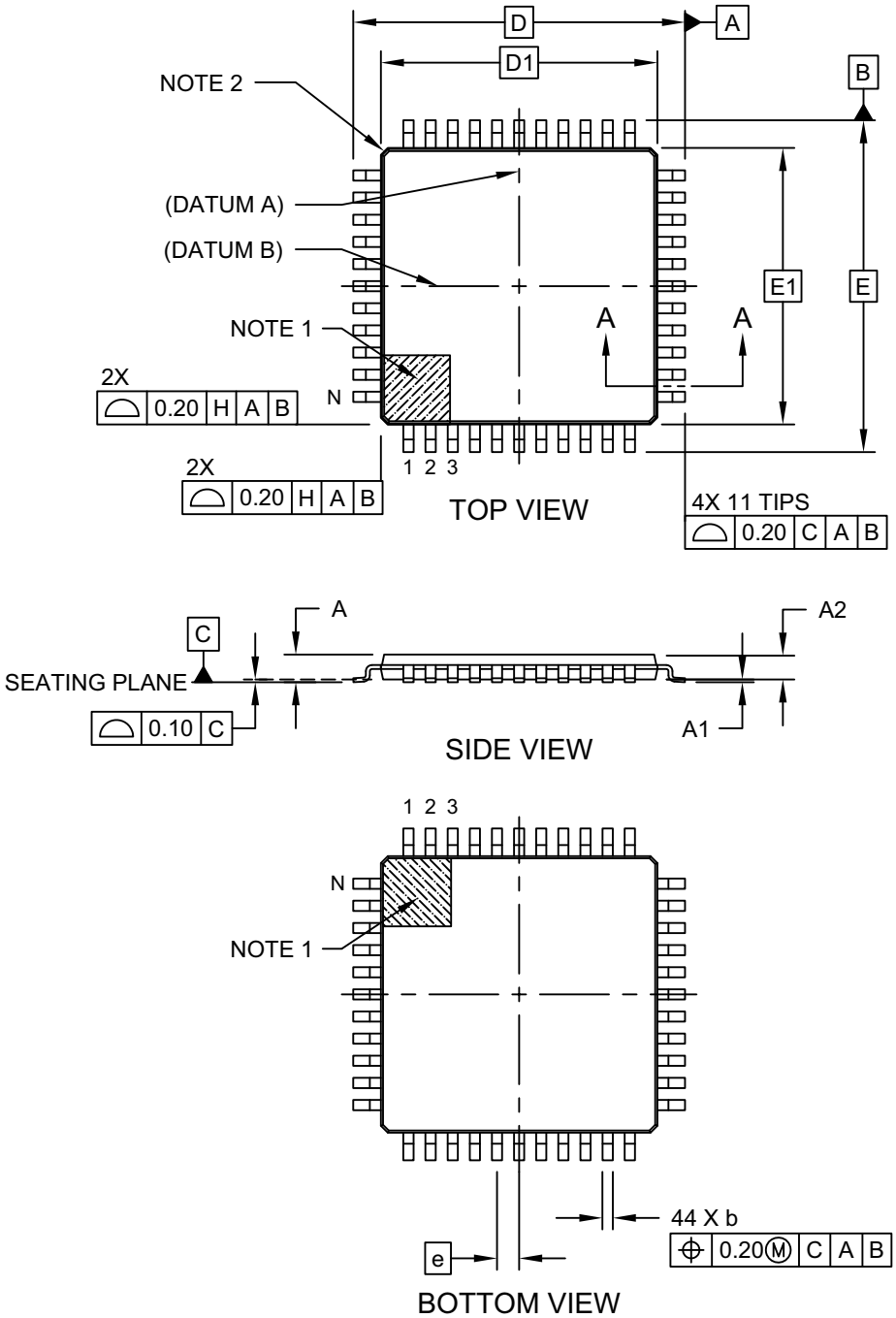
TABLE 26-49: CONSTANT-CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS(1)				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CC01	IDD	Current Consumption	—	30	—	µA	
CC02	IREG	Regulation of Current with Voltage On	—	±3	—	%	
CC03	IOUT	Current Output at Terminal	—	10	—	µA	

Note 1: The constant-current source module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-076C Sheet 1 of 2