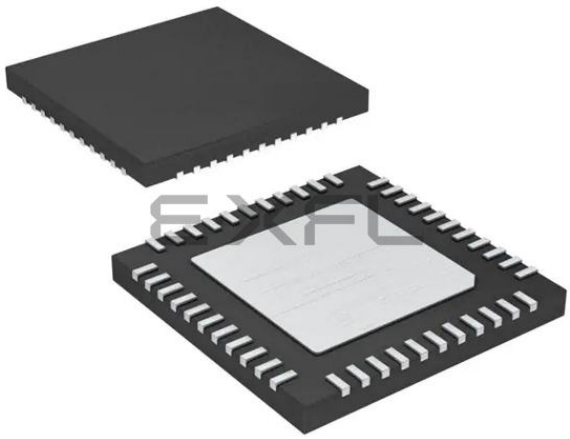
Microchip Technology - DSPIC33EP32GS504-I/ML Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gs504-i-ml

Communication Interfaces

- Two UART modules (15 Mbps):
  - Supports LIN/J2602 protocols and IrDA®
- Two 4-Wire SPI modules (15 Mbps)
- Two I^2C modules (up to 1 Mbaud) with SMBus Support

Input/Output

- Constant-Current Source (10 µA nominal)
- Sink/Source up to 12mA/15mA, respectively; Pin-Specific for Standard VOH/VOL
- 5V Tolerant Pins
- Selectable, Open-Drain Pull-ups and Pull-Downs
- External Interrupts on All I/O Pins
- Peripheral Pin Select (PPS) to allow Function Remap with Six Virtual I/Os

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40°C to +125°C)
- Class B Safety Library, IEC 60730
- The 6x6x0.5 mm UQFN Package is Designed and Optimized to ease IPC9592B 2nd Level Temperature Cycle Qualification

Debugger Development Support

- In-Circuit and In-Application Programming
- Five Program and Three Complex Data Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

Device	Pins	Program Memory Bytes	RAM (Bytes)	General Purpose I/O (GPIO)	Remappable Peripherals								12-Bit ADC		PGA	Analog Comparator	DAC Output	Constant-Current Source	Packages
					Timers(1)	Input Capture	Output Compare	UART	SPI	PWM(2)	External Interrupts(3)	Reference Clock	I^2C	Analog Inputs	S&H Circuits				
dsPIC33EP16GS502	28	16K	2K	21	5	4	4	2	2	5x2	3	1	2	12	5	2	4	1	1	SOIC, QFN-S, UQFN
dsPIC33EP32GS502	28	32K	4K	21	5	4	4	2	2	5x2	3	1	2	12	5	2	4	1	1	
dsPIC33EP64GS502	28	64K	8K	21	5	4	4	2	2	5x2	3	1	2	12	5	2	4	1	1	
dsPIC33EP16GS504	44	16K	2K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	QFN, TQFP
dsPIC33EP32GS504	44	32K	4K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	
dsPIC33EP64GS504	44	64K	8K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	
dsPIC33EP16GS505	48	16K	2K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	TQFP
dsPIC33EP32GS505	48	32K	4K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	
dsPIC33EP64GS505	48	64K	8K	35	5	4	4	2	2	5x2	3	1	2	19	5	2	4	1	1	
dsPIC33EP16GS506	64	16K	2K	53	5	4	4	2	2	5x2	4	1	2	22	5	2	4	2	1	TQFP
dsPIC33EP32GS506	64	32K	4K	53	5	4	4	2	2	5x2	4	1	2	22	5	2	4	2	1	
dsPIC33EP64GS506	64	64K	8K	53	5	4	4	2	2	5x2	4	1	2	22	5	2	4	2	1	

Note 1: The external clock for Timer1, Timer2 and Timer3 is remappable.

2: PWM4 and PWM5 are remappable on all devices except the 64-pin devices.

3: External interrupts, INT0 and INT4, are not remappable.

TABLE 4-7: PWM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
PTCON2	0C02	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
PTPER	0C04	PWMx Primary Master Time Base Period Register (PTPER<15:0>)																FFF8
SEVTCMP	0C06	PWMx Special Event Compare Register (SEVTCMP12:0>)													—	—	—	0000
MDC	0C0A	PWMx Master Duty Cycle Register (MDC<15:0>)																0000
STCON	0C0E	—	—	—	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
STCON2	0C10	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
STPER	0C12	PWMx Secondary Master Time Base Period Register (STPER<15:0>)																FFF8
SSEVTCMP	0C14	PWMx Secondary Special Event Compare Register (SSEVTCMP<12:0>)													—	—	—	0000
CHOP	0C1A	CHPCLKEN	—	—	—	—	—	CHOPCLK6	CHOPCLK5	CHOPCLK4	CHOPCLK3	CHOPCLK2	CHOPCLK1	CHOPCLK0	—	—	—	0000
PWMKEY	0C1E	PWMx Protection Lock/Unlock Key Register (PWMKEY<15:0>)																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: PWM GENERATOR 1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON1	0C24	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC1	0C26	PWM1 Generator Duty Cycle Register (PDC1<15:0>)																0000
PHASE1	0C28	PWM1 Primary Phase-Shift or Independent Time Base Period Register (PHASE1<15:0>)																0000
DTR1	0C2A	—	—	PWM1 Dead-Time Register (DTR1<13:0>)														0000
ALTDTR1	0C2C	—	—	PWM1 Alternate Dead-Time Register (ALTDTR1<13:0>)														0000
SDC1	0C2E	PWM1 Secondary Duty Cycle Register (SDC1<15:0>)																0000
SPHASE1	0C30	PWM1 Secondary Phase-Shift Register (SPHASE1<15:0>)																0000
TRIG1	0C32	PWM1 Primary Trigger Compare Value Register (TRGCMP<12:0>)													—	—	—	0000
TRGCON1	0C34	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG1	0C36	PWM1 Secondary Trigger Compare Value Register (STRGCMP<12:0>)													—	—	—	0000
PWMCAP1	0C38	PWM1 Primary Time Base Capture Register (PWMCAP<12:0>)													—	—	—	0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	—	—	—	—	PWM1 Leading-Edge Blanking Delay Register (LEB<8:0>)									—	—	—	0000
AUXCON1	0C3E	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: PWM GENERATOR 4 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON4	0C80	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	MTBS	CAM	XPRES	IUE	0000
IOCON4	0C82	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON4	0C84	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC4	0C86	PWM4 Generator Duty Cycle Register (PDC4<15:0>)																0000
PHASE4	0C88	PWM4 Primary Phase-Shift or Independent Time Base Period Register (PHASE4<15:0>)																0000
DTR4	0C8A	—	—	PWM4 Dead-Time Register (DTR4<13:0>)														0000
ALTDTR4	0C8C	—	—	PWM4 Alternate Dead-Time Register (ALTDTR4<13:0>)														0000
SDC4	0C8E	PWM4 Secondary Duty Cycle Register (SDC4<15:0>)																0000
SPHASE4	0C90	PWM4 Secondary Phase-Shift Register (SPHASE4<15:0>)																0000
TRIG4	0C92	PWM4 Primary Trigger Compare Value Register (TRGCMP<12:0>)													—	—	—	0000
TRGCON4	0C94	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG4	0C96	PWM4 Secondary Trigger Compare Value Register (STRGCMP<12:0>)													—	—	—	0000
PWMCAP4	0C98	PWM4 Primary Time Base Capture Register (PWMCAP<12:0>)													—	—	—	0000
LEBCON4	0C9A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY4	0C9C	—	—	—	—	PWM4 Leading-Edge Blanking Delay Register (LEB<8:0>)									—	—	—	0000
AUXCON4	0C9E	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: PWM GENERATOR 5 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON5	0CA0	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	—	—	MTBS	CAM	XPRES	IUE	0000
IOCON5	0CA2	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON5	0CA4	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC5	0CA6	PWM5 Generator Duty Cycle Register (PDC5<15:0>)																0000
PHASE5	0CA8	PWM5 Primary Phase-Shift or Independent Time Base Period Register (PHASE5<15:0>)																0000
DTR5	0CAA	—	—	PWM5 Dead-Time Register (DTR5<13:0>)														0000
ALTDTR5	0CAC	—	—	PWM5 Alternate Dead-Time Register (ALTDTR5<13:0>)														0000
SDC5	0CAE	PWM5 Secondary Duty Cycle Register (SDC5<15:0>)																0000
SPHASE5	0CB0	PWM5 Secondary Phase-Shift Register (SPHASE5<15:0>)																0000
TRIG5	0CB2	PWM5 Primary Trigger Compare Value Register (TRGCMP<12:0>)													—	—	—	0000
TRGCON5	0CB4	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	DTM	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
STRIG5	0CB6	PWM5 Secondary Trigger Compare Value Register (STRGCMP<12:0>)													—	—	—	0000
PWMCAP5	0CB8	PWM5 Primary Time Base Capture Register (PWMCAP<12:0>)													—	—	—	0000
LEBCON5	0CBA	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY5	0CBC	—	—	—	—	PWM5 Leading-Edge Blanking Delay Register (LEB<8:0>)									—	—	—	0000
AUXCON5	0CBE	HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: I2C1 AND I2C2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1CONL	0200	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1CONH	0202	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
I2C1STAT	0204	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	0206	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	0208	—	—	—	—	—	—	I2C1 Slave Mode Address Mask Register										0000
I2C1BRG	020A	Baud Rate Generator Register																0000
I2C1TRN	020C	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1RCV	020E	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
I2C2CON1	0210	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2CON2	0212	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
I2C2STAT	0214	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C2ADD	0216	—	—	—	—	—	—	I2C2 Address Register										0000
I2C2MSK	0218	—	—	—	—	—	—	I2C2 Slave Mode Address Mask Register										0000
I2C2BRG	021A	Baud Rate Generator Register																0000
I2C2TRN	021C	—	—	—	—	—	—	—	—	I2C2 Transmit Register								00FF
I2C2RCV	021E	—	—	—	—	—	—	—	—	I2C2 Receive Register								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-14: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler Register																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	Baud Rate Generator Prescaler Register																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: PERIPHERAL PIN SELECT INPUT REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	INT1R<7:0>								—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	INT2R<7:0>								0000
RPINR2	06A4	T1CKR<7:0>								—	—	—	—	—	—	—	—	0000
RPINR3	06A6	T3CKR7	T3CKR6	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0	T2CKR7	T2CKR6	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0	0000
RPINR7	06AE	IC2R7	IC2R6	IC2R5	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0	IC1R7	IC1R6	IC1R5	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0	0000
RPINR8	06B0	IC4R7	IC4R6	IC4R5	IC4R4	IC4R3	IC4R2	IC4R1	IC4R0	IC3R7	IC3R6	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0	0000
RPINR11	06B6	—	—	—	—	—	—	—	—	OCFAR<7:0>								0000
RPINR12	06B8	FLT2R7	FLT2R6	FLT2R5	FLT2R4	FLT2R3	FLT2R2	FLT2R1	FLT2R0	FLT1R7	FLT1R6	FLT1R5	FLT1R4	FLT1R3	FLT1R2	FLT1R1	FLT1R0	0000
RPINR13	06BA	FLT4R7	FLT4R6	FLT4R5	FLT4R4	FLT4R3	FLT4R2	FLT4R1	FLT4R0	FLT3R7	FLT3R6	FLT3R5	FLT3R4	FLT3R3	FLT3R2	FLT3R1	FLT3R0	0000
RPINR18	06C4	U1CTSR7	U1CTSR6	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTS0	U1RXR7	U1RXR6	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0	0000
RPINR19	06C6	U2CTSR7	U2CTSR6	U2CTSR5	U2CTSR4	U2CTSR3	U2CTSR2	U2CTSR1	U2CTSR0	U2RXR7	U2RXR6	U2RXR5	U2RXR4	U2RXR3	U2RXR2	U2RXR1	U2RXR0	0000
RPINR20	06C8	SCK1INR7	SCK1INR6	SCK1INR5	SCK1INR4	SCK1INR3	SCK1INR2	SCK1INR1	SCK1INR0	SDI1R7	SDI1R6	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0	0000
RPINR21	06CA	—	—	—	—	—	—	—	—	SS1R<7:0>								0000
RPINR22	06CC	SCK2INR7	SCK2INR6	SCK2INR5	SCK2INR4	SCK2INR3	SCK2INR2	SCK2INR1	SCK2INR0	SDI2R7	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0	0000
RPINR23	06CE	—	—	—	—	—	—	—	—	SS2R<7:0>								0000
RPINR37	06EA	SYNCI1R<7:0>								—	—	—	—	—	—	—	—	0000
RPINR38	06EC	—	—	—	—	—	—	—	—	SYNCI2R<7:0>								0000
RPINR42	06F4	FLT6R7	FLT6R6	FLT6R5	FLT6R4	FLT6R3	FLT6R2	FLT6R1	FLT6R0	FLT5R7	FLT5R6	FLT5R5	FLT5R4	FLT5R3	FLT5R2	FLT5R1	FLT5R0	0000
RPINR43	06F6	FLT8R7	FLT8R6	FLT8R5	FLT8R4	FLT8R3	FLT8R2	FLT8R1	FLT8R0	FLT7R7	FLT7R6	FLT7R5	FLT7R4	FLT7R3	FLT7R2	FLT7R1	FLT7R0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 10-30: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP53R5	RP53R4	RP53R3	RP53R2	RP53R1	RP53R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP52R5	RP52R4	RP52R3	RP52R2	RP52R1	RP52R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP53R<5:0>:** Peripheral Output Function is Assigned to RP53 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP52R<5:0>:** Peripheral Output Function is Assigned to RP52 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-31: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP55R<5:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP54R<5:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 14-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTMD:** Fault Mode Select bit
- 1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTA bit is cleared in software and a new PWMx period starts
- 0 = Fault mode is maintained until the Fault source is removed and a new PWMx period starts

bit 14 **FLTOUT:** Fault Out bit
- 1 = PWMx output is driven high on a Fault
- 0 = PWMx output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
- 1 = OCx pin is tri-stated on a Fault condition
- 0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition

bit 12 **OCINV:** Output Compare x Invert bit
- 1 = OCx output is inverted
- 0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
- 1 = Cascade module operation is enabled
- 0 = Cascade module operation is disabled

bit 7 **OCTRIG:** Output Compare x Trigger/Sync Select bit
- 1 = Triggers OCx from the source designated by the SYNCSELx bits
- 0 = Synchronizes OCx with the source designated by the SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
- 1 = Timer source has been triggered and is running
- 0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** Output Compare x Output Pin Direction Select bit
- 1 = OCx is tri-stated
- 0 = OCx module drives the OCx pin

Note 1: Do not use the OCx module as its own synchronization or trigger source.

2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

REGISTER 16-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit has started, SPIxTXB is empty

Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer Mode:
Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full
0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

REGISTER 17-1: I2CxCONL: I2Cx CONTROL REGISTER LOW (CONTINUED)

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; hardware is clear at the end of the master Acknowledge sequence
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C; hardware is clear at the end of the eighth bit of the master receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on SDAx and SCLx pins; hardware is clear at the end of the master Stop sequence
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Repeated Start sequence
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Start sequence
0 = Start condition is not in progress

REGISTER 18-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
0 = Baud rate measurement is disabled or completed

bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

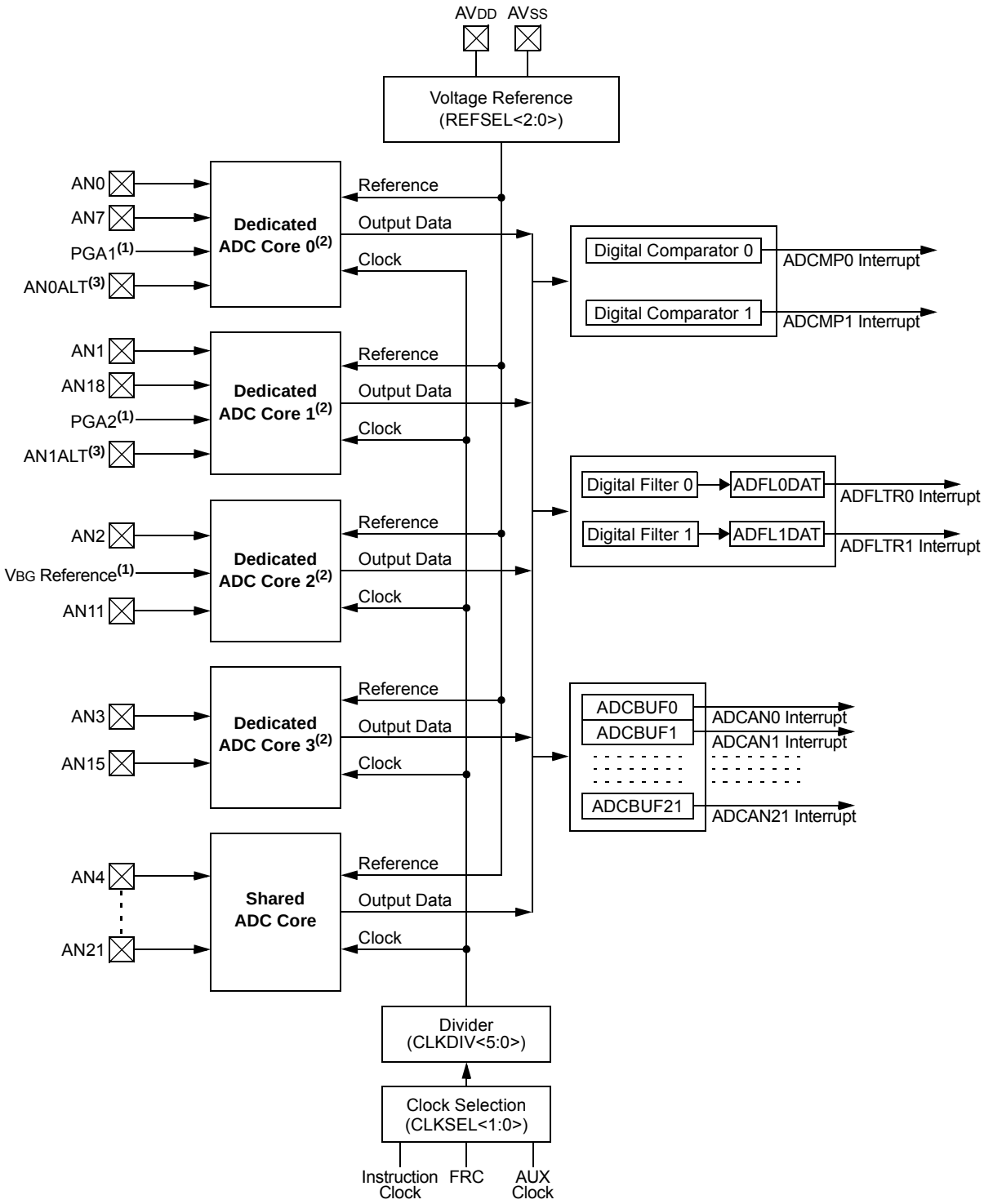
bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

Note 1: Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

FIGURE 19-1: ADC MODULE BLOCK DIAGRAM



Note 1: PGA1, PGA2 and Band Gap Reference (V_{BG}) are internal analog inputs and are not available on device pins.
2: If the dedicated core uses an alternate channel, then shared core function cannot be used.
3: AN0ALT and AN1ALT are not available on dsPIC33EPXXGS502 devices.

REGISTER 19-5: ADCON3L: ADC CONTROL REGISTER 3 LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HSC	R/W-0	R-0, HSC
REFSEL2	REFSEL1	REFSEL0	SUSPEND	SUSPCIE	SUSPRDY	SHRSAMP	CNVRTCH
bit 15							bit 8

R/W-0	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SWLCTRG	SWCTRG	CNVCHSEL5	CNVCHSEL4	CNVCHSEL3	CNVCHSEL2	CNVCHSEL1	CNVCHSEL0
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **REFSEL<2:0>:** ADC Reference Voltage Selection bits

Value	VREFH	VREFL
000	AVDD	AVSS

001-111 = **Unimplemented:** Do not use

bit 12 **SUSPEND:** All ADC Cores Triggers Disable bit

1 = All new trigger events for all ADC cores are disabled
0 = All ADC cores can be triggered

bit 11 **SUSPCIE:** Suspend All ADC Cores Common Interrupt Enable bit

1 = Common interrupt will be generated when ADC core triggers are suspended (SUSPEND bit = 1) and all previous conversions are finished (SUSPRDY bit becomes set)
0 = Common interrupt is not generated for suspend ADC cores event

bit 10 **SUSPRDY:** All ADC Cores Suspended Flag bit

1 = All ADC cores are suspended (SUSPEND bit = 1) and have no conversions in progress
0 = ADC cores have previous conversions in progress

bit 9 **SHRSAMP:** Shared ADC Core Sampling Direct Control bit

This bit should be used with the individual channel conversion trigger controlled by the CNVRTCH bit. It connects an analog input, specified by the CNVCHSEL<5:0> bits, to the shared ADC core and allows extending the sampling time. This bit is not controlled by hardware and must be cleared before the conversion starts (setting CNVRTCH to '1').

1 = Shared ADC core samples an analog input specified by the CNVCHSEL<5:0> bits
0 = Sampling is controlled by the shared ADC core hardware

bit 8 **CNVRTCH:** Software Individual Channel Conversion Trigger bit

1 = Single trigger is generated for an analog input specified by the CNVCHSEL<5:0> bits; when the bit is set, it is automatically cleared by hardware on the next instruction cycle
0 = Next individual channel conversion trigger can be generated

bit 7 **SWLCTRG:** Software Level-Sensitive Common Trigger bit

1 = Triggers are continuously generated for all channels with the software, level-sensitive common trigger selected as a source in the ADTRIGxL and ADTRIGxH registers
0 = No software, level-sensitive common triggers are generated

bit 6 **SWCTRG:** Software Common Trigger bit

1 = Single trigger is generated for all channels with the software, common trigger selected as a source in the ADTRIGxL and ADTRIGxH registers; when the bit is set, it is automatically cleared by hardware on the next instruction cycle
0 = Ready to generate the next software, common trigger

bit 5-0 **CNVCHSEL <5:0>:** Channel Number Selection for Software Individual Channel Conversion Trigger bits

These bits define a channel to be converted when the CNVRTCH bit is set.

REGISTER 19-27: ADTRIGxH: ADC CHANNEL TRIGGER x SELECTION REGISTER HIGH (x = 0 to 5) (CONTINUED)

bit 4-0 **TRGSRC(4x+2)<4:0>:** Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
11110 = Reserved
11101 = Reserved
11100 = PWM Generator 5 current-limit trigger
11011 = PWM Generator 4 current-limit trigger
11010 = PWM Generator 3 current-limit trigger
11001 = PWM Generator 2 current-limit trigger
11000 = PWM Generator 1 current-limit trigger
10111 = Output Compare 2 trigger
10110 = Output Compare 1 trigger
10101 = Reserved
10100 = Reserved
10011 = PWM Generator 5 secondary trigger
10010 = PWM Generator 4 secondary trigger
10001 = PWM Generator 3 secondary trigger
10000 = PWM Generator 2 secondary trigger
01111 = PWM Generator 1 secondary trigger
01110 = PWM secondary Special Event Trigger
01101 = Timer2 period match
01100 = Timer1 period match
01011 = Reserved
01010 = Reserved
01001 = PWM Generator 5 primary trigger
01000 = PWM Generator 4 primary trigger
00111 = PWM Generator 3 primary trigger
00110 = PWM Generator 2 primary trigger
00101 = PWM Generator 1 primary trigger
00100 = PWM Special Event Trigger
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

REGISTER 19-29: ADCAL0H: ADC CALIBRATION REGISTER 0 HIGH

R-0, HSC	U-0	U-0	U-0	r-0	R/W-0	R/W-0	R/W-0
CAL3RDY	—	—	—	—	CAL3DIFF	CAL3EN	CAL3RUN
bit 15							bit 8

R-0, HSC	U-0	U-0	U-0	r-0	R/W-0	R/W-0	R/W-0
CAL2RDY	—	—	—	—	CAL2DIFF	CAL2EN	CAL2RUN
bit 7							bit 0

Legend:	r = Reserved bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CAL3RDY:** Dedicated ADC Core 3 Calibration Status Flag bit
1 = Dedicated ADC Core 3 calibration is finished
0 = Dedicated ADC Core 3 calibration is in progress

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **Reserved:** Must be written as '0'

bit 10 **CAL3DIFF:** Dedicated ADC Core 3 Differential-Mode Calibration bit
1 = Dedicated ADC Core 3 will be calibrated in Differential Input mode
0 = Dedicated ADC Core 3 will be calibrated in Single-Ended Input mode

bit 9 **CAL3EN:** Dedicated ADC Core 3 Calibration Enable bit
1 = Dedicated ADC Core 3 calibration bits (CALxRDY, CALxDIFF and CALxRUN) can be accessed by software
0 = Dedicated ADC Core 3 calibration bits are disabled

bit 8 **CAL3RUN:** Dedicated ADC Core 3 Calibration Start bit
1 = If this bit is set by software, the dedicated ADC Core 3 calibration cycle is started; this bit is automatically cleared by hardware
0 = Software can start the next calibration cycle

bit 7 **CAL2RDY:** Dedicated ADC Core 2 Calibration Status Flag bit
1 = Dedicated ADC Core 2 calibration is finished
0 = Dedicated ADC Core 2 calibration is in progress

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **Reserved:** Must be written as '0'

bit 2 **CAL2DIFF:** Dedicated ADC Core 2 Differential-Mode Calibration bit
1 = Dedicated ADC Core 2 will be calibrated in Differential Input mode
0 = Dedicated ADC Core 2 will be calibrated in Single-Ended Input mode

bit 1 **CAL2EN:** Dedicated ADC Core 2 Calibration Enable bit
1 = Dedicated ADC Core 2 calibration bits (CALxRDY, CALxDIFF and CALxRUN) can be accessed by software
0 = Dedicated ADC Core 2 calibration bits are disabled

bit 0 **CAL2RUN:** Dedicated ADC Core 2 Calibration Start bit
1 = If this bit is set by software, the dedicated ADC Core 2 calibration cycle is started; this bit is automatically cleared by hardware
0 = Software can start the next calibration cycle

NOTES:

23.7 JTAG Interface

The dsPIC33EPXXGS50X family devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

Note: Refer to **"Programming and Diagnostics"** (DS70608) in the *"dsPIC33/PIC24 Family Reference Manual"* for further information on usage, configuration and operation of the JTAG interface.

23.8 In-Circuit Serial Programming™

The dsPIC33EPXXGS50X family devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for details about In-Circuit Serial Programming™ (ICSP™).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

23.9 In-Circuit Debugger

When MPLAB® ICD 3 or REAL ICE™ emulator is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{\text{MCLR}}$, VDD, VSS and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

23.10 Code Protection and CodeGuard™ Security

dsPIC33EPXXGS50X devices offer multiple levels of security for protecting individual intellectual property. The program Flash protection can be broken up into three segments: Boot Segment (BS), General Segment (GS) and Configuration Segment (CS). Boot Segment has the highest security privilege and can be thought to have limited restrictions when accessing other segments. General Segment has the least security and is intended for the end user system code. Configuration Segment contains only the device user configuration data which is located at the end of the program memory space.

The code protection features are controlled by the Configuration registers, FSEC and FBSLIM. The FSEC register controls the code-protect level for each segment and if that segment is write-protected. The size of BS and GS will depend on the BSLIM<12:0> setting and if the Alternate Interrupt Vector Table (AIVT) is enabled. The BSLIM<12:0> bits define the number of pages for BS with each page containing 512 IW. The smallest BS size is one page, which will consist of the Interrupt Vector Table (IVT) and 256 IW of code protection.

If the AIVT is enabled, the last page of BS will contain the AIVT and will not contain any BS code. With AIVT enabled, the smallest BS size is now two pages (1024 IW), with one page for the IVT and BS code, and the other page for the AIVT. Write protection of the BS does not cover the AIVT. The last page of BS can always be programmed or erased by BS code. The General Segment will start at the next page and will consume the rest of program Flash except for the Flash Configuration Words. The IVT will assume GS security only if BS is not enabled. The IVT is protected from being programmed or page erased when either security segment has enabled write protection.

Note: Refer to **"CodeGuard™ Intermediate Security"** (DS70005182) in the *"dsPIC33/PIC24 Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security.

TABLE 24-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
48	MOV	MOV f,Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f,WREG	Move f to WREG	1	1	None
		MOV #lit16,Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b #lit8,Wn	Move 8-bit literal to Wn	1	1	None
		MOV Wn,f	Move Wn to f	1	1	None
		MOV Wso,Wdo	Move Ws to Wd	1	1	None
		MOV WREG,f	Move WREG to f	1	1	None
		MOV.D Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
49	MOVPAG	MOVPAG #lit10,DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG #lit8,TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAGW Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAGW Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
50	MOVSAC	MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB	Prefetch and store accumulator	1	1	None
51	MPY	MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
52	MPY.N	MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
53	MSC	MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
54	MUL	MUL.SS Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb,Ws,Acc	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,Ws,Acc	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Acc	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb,Ws,Acc	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb,#lit5,Acc	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,Ws,Acc	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb,Ws,Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb,Ws,Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb,Ws,Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb,Ws,Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb,#lit5,Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 26-7: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**		
Idle Current (I_{IDLE})(1)						
DC40d	2	4	mA	-40°C	3.3V	10 MIPS
DC40a	2	4	mA	+25°C		
DC40b	2	4	mA	+85°C		
DC40c	2	4	mA	+125°C		
DC42d	3	6	mA	-40°C	3.3V	20 MIPS
DC42a	3	6	mA	+25°C		
DC42b	3	6	mA	+85°C		
DC42c	3	6	mA	+125°C		
DC44d	6	12	mA	-40°C	3.3V	40 MIPS
DC44a	6	12	mA	+25°C		
DC44b	6	12	mA	+85°C		
DC44c	6	12	mA	+125°C		
DC45d	8	15	mA	-40°C	3.3V	60 MIPS
DC45a	8	15	mA	+25°C		
DC45b	8	15	mA	+85°C		
DC45c	8	15	mA	+125°C		
DC46d	10	20	mA	-40°C	3.3V	70 MIPS
DC46a	10	20	mA	+25°C		
DC46b	10	20	mA	+85°C		

Note 1: Base Idle current (I_{IDLE}) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating or being clocked (all defined PMDx bits are set)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

TABLE 26-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**	
Power-Down Current (I_{PD})(1)					
DC60d	12	100	μA	-40°C	3.3V
DC60a	18	100	μA	+25°C	
DC60b	130	400	μA	+85°C	
DC60c	500	1100	μA	+125°C	

Note 1: I_{PD} (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

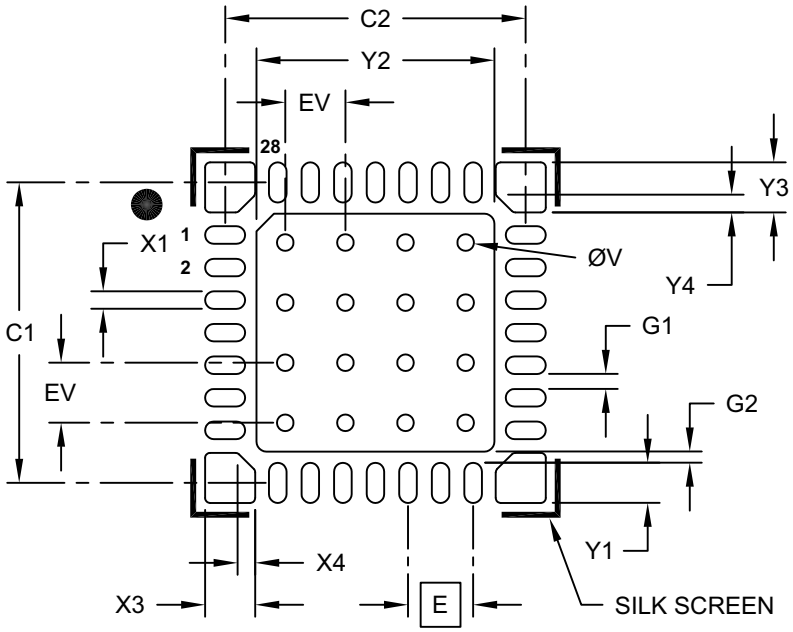
TABLE 26-9: DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT (ΔI_{WDT})(1)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**	
DC61d	13	50	μA	-40°C	3.3V
DC61a	19	80	μA	+25°C	
DC61b	12	—	μA	+85°C	
DC61c	13	—	μA	+125°C	

Note 1: The ΔI_{WDT} current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current. All parameters are characterized but not tested during manufacturing.

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (2N) - 6x6x0.55 mm Body [UQFN] With 4.65x4.65 mm Exposed Pad and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			4.75
Optional Center Pad Length	Y2			4.75
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.35
Contact Pad Length (X28)	Y1			0.80
Corner Anchor (X4)	X3			1.00
Corner Anchor (X4)	Y3			1.00
Corner Anchor Chamfer (X4)	X4			0.35
Corner Anchor Chamfer (X4)	Y4			0.35
Contact Pad to Pad (X28)	G1	0.20		
Contact Pad to Center Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2385B

Note: Corner anchor pads are not connected internally and are designed as mechanical features when the package is soldered to the PCB.