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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32gs504-i-pt

dsPIC33EPXXGS50X FAMILY

FIGURE 2-6: OFF-LINE UPS

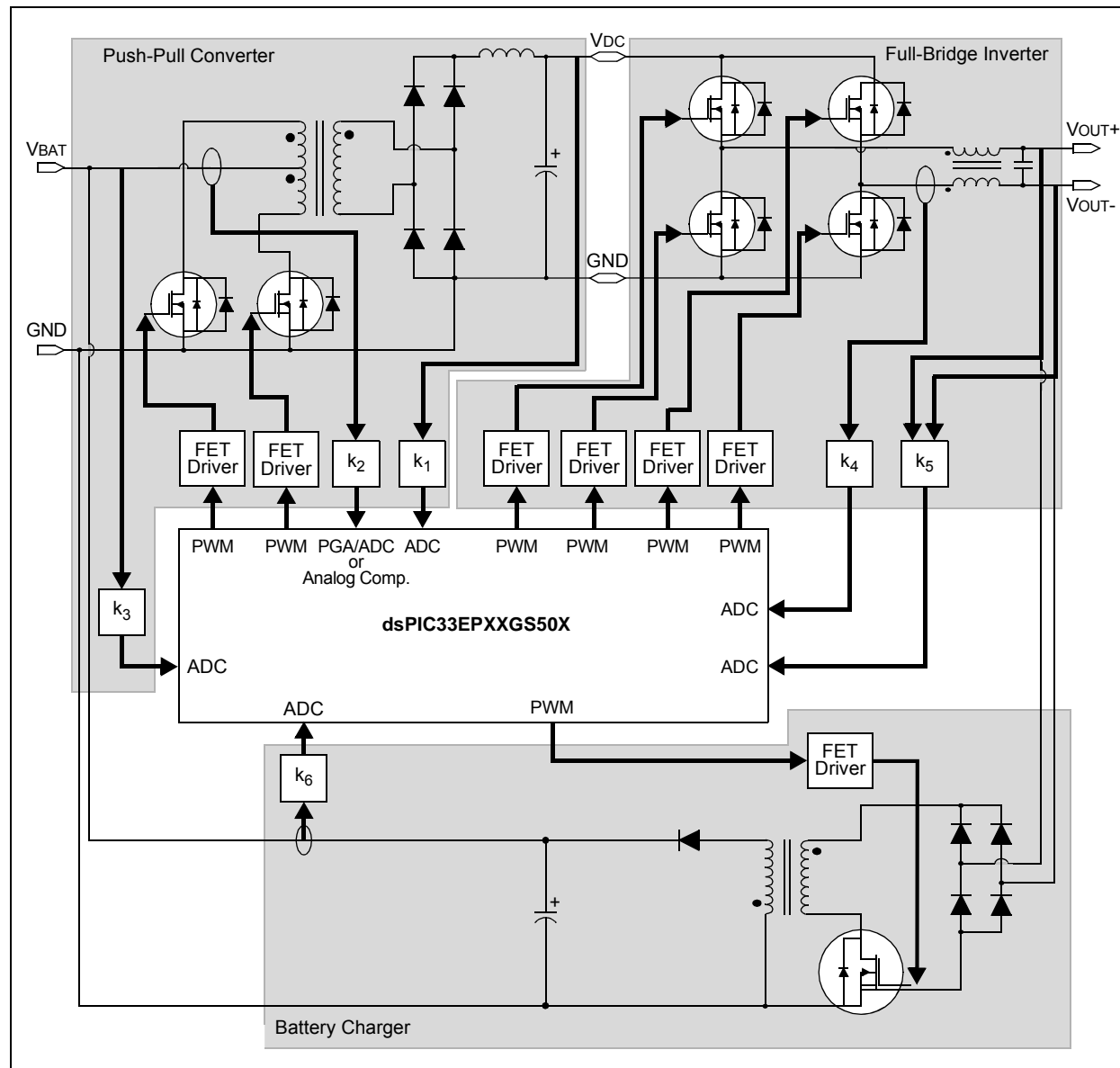


TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	NVMIF	—	ADCIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	—	—	—	—	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	—	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	PSEMIF	—	—	INT4IF	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	—	—	—	—	PSESIF	—	—	—	—	—	—	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	ADCAN1IF	ADCAN0IF	—	—	—	—	AC4IF	AC3IF	AC2IF	—	—	—	—	PWM5IF	PWM4IF	PWM3IF	0000
IFS7	080E	—	—	—	—	—	—	—	—	—	—	ADCAN7IF	ADCAN6IF	ADCAN5IF	ADCAN4IF	ADCAN3IF	ADCAN2IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	ADCAN16IF ⁽¹⁾	ADCAN15IF ⁽¹⁾	ADCAN14IF ⁽²⁾	ADCAN13IF ⁽¹⁾	ADCAN12IF ⁽²⁾	ADCAN11IF ⁽²⁾	ADCAN10IF ⁽²⁾	ADCAN9IF ⁽²⁾	ADCAN8IF ⁽²⁾	—	—	—	—	—	—	—	0000
IFS10	0814	—	I2C2BCIF	I2C1BCIF	—	—	—	—	—	—	—	—	ADCAN21IF	ADCAN20IF	ADCAN19IF	ADCAN18IF	ADCAN17IF ⁽²⁾	0000
IFS11	0816	—	—	—	—	—	—	—	—	—	—	—	ADFLTR1IF	ADFLTR0IF	ADCMP1IF	ADCMP0IF	—	0000
IEC0	0820	NVMIE	—	ADCIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	—	—	—	—	INT1IE	CNIE	AC1IF	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	—	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	PSEMIIE	—	—	INT4IE	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	—	—	—	—	PSESIIE	—	—	—	—	—	—	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	ADCAN1IE	ADCAN0IE	—	—	—	—	AC4IE	AC3IE	AC2IE	—	—	—	—	PWM5IE	PWM4IE	PWM3IE	0000
IEC7	082E	—	—	—	—	—	—	—	—	—	—	ADCAN7IE	ADCAN6IE	ADCAN5IE	ADCAN4IE	ADCAN3IE	ADCAN2IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	ADCAN16IE ⁽¹⁾	ADCAN15IE ⁽¹⁾	ADCAN14IE ⁽²⁾	ADCAN13IE ⁽¹⁾	ADCAN12IE ⁽²⁾	ADCAN11IE ⁽²⁾	ADCAN10IE ⁽²⁾	ADCAN9IE ⁽²⁾	ADCAN8IE ⁽²⁾	—	—	—	—	—	—	—	0000
IEC10	0834	—	I2C2BCIE	I2C1BCIE	—	—	—	—	—	—	—	—	ADCAN21IE	ADCAN20IE	ADCAN19IE	ADCAN18IE	ADCAN17IE ⁽²⁾	0000
IEC11	0836	—	—	—	—	—	—	—	—	—	—	—	ADFLTR1IE	ADFLTR0IE	ADCMP1IE	ADCMP0IE	—	0000
IPC0	0840	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	0842	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	—	—	—	4440
IPC2	0844	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	0846	—	NVMIP2	NVMIP1	NVMIP0	—	—	—	—	—	ADCIP2	ADCIP1	ADCIP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4044
IPC4	0848	—	CNIP2	CNIP1	CNIP0	—	AC1IP2	AC1IP1	AC1IP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0004
IPC6	084C	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	—	—	—	4440
IPC7	084E	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP2	SPI2IP1	SPI2IP0	—	SPI2EIP2	SPI2EIP1	SPI2EIP0	0044
IPC9	0852	—	—	—	—	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	—	—	—	0440

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Only available on dsPIC33EPXXGS506 devices.

Note 2: Only available on dsPIC33EPXXGS504/505 and dsPIC33EPXXGS506 devices.

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4.6.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, and the DSP accumulator class of instructions, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the `MOV` instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit `Wb` (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.6.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MPY`, `MPY.N`, `MOVSAC` and `MSC`), also referred to as `MAC` instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {`W8`, `W9`, `W10`, `W11`}. For data reads, `W8` and `W9` are always directed to the X RAGU, and `W10` and `W11` are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for `W8` and `W9`, and Y Data Space for `W10` and `W11`.

Note: Register Indirect with Register Offset Addressing mode is available only for `W9` (in X space) and `W11` (in Y space).

In summary, the following addressing modes are supported by the `MAC` class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.6.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, `BRA` (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the `DISI` instruction uses a 14-bit unsigned literal field. In some instructions, such as `ULNK`, the source of an operand or result is implied by the opcode itself. Certain operations, such as a `NOP`, do not have any operands.

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REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 ⁽²⁾	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
 1 = Variable exception processing is enabled
 0 = Fixed exception processing is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽²⁾
 1 = CPU Interrupt Priority Level is greater than 7
 0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

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REGISTER 10-24: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 10-2 for peripheral function numbers)

REGISTER 10-25: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0
bit 15						bit 8	

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 10-2 for peripheral function numbers)

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REGISTER 15-16: SPHASE_x: PWM_x SECONDARY PHASE-SHIFT REGISTER (x = 1 to 5)^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASE _x <15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASE _x <7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **SPHASE_x<15:0>**: Secondary Phase Offset for PWM_xL Output Pin bits
(used in Independent PWM mode only)

Note 1: If PWMCON_x<9> = 0, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (IOCON_x<11:10> = 00, 01 or 10);
SPHASE_x<15:0> = Not used
- True Independent Output mode (IOCON_x<11:10> = 11), PHASE_x<15:0> = Phase-shift value for PWM_xL only

2: If PWMCON_x<9> = 1, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (IOCON_x<11:10> = 00, 01 or 10);
SPHASE_x<15:0> = Not used
- True Independent Output mode (IOCON_x<11:10> = 11); PHASE_x<15:0> = Independent time base period value for PWM_xL only
- When the PHASE_x/SPHASE_x registers provide the local period, the valid range of values is 0x0010-0xFFFF8

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REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSSEN ⁽²⁾	CKP	MSTEN	SPRE2 ⁽³⁾	SPRE1 ⁽³⁾	SPRE0 ⁽³⁾	PPRE1 ⁽³⁾	PPRE0 ⁽³⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCKx Pin bit (SPIx Master modes only)

1 = Internal SPIx clock is disabled, pin functions as I/O

0 = Internal SPIx clock is enabled

bit 11 **DISSDO:** Disable SDOx Pin bit

1 = SDOx pin is not used by the module; pin functions as I/O

0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit

1 = Communication is word-wide (16 bits)

0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit

Master Mode:

1 = Input data is sampled at the end of data output time

0 = Input data is sampled at the middle of data output time

Slave Mode:

SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** SPIx Clock Edge Select bit⁽¹⁾

1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)

0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)

bit 7 **SSSEN:** Slave Select Enable bit (Slave mode)⁽²⁾

1 = \overline{SSx} pin is used for Slave mode

0 = \overline{SSx} pin is not used by the module; pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit

1 = Idle state for clock is a high level; active state is a low level

0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit

1 = Master mode

0 = Slave mode

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).

2: This bit must be cleared when FRMEN = 1.

3: Do not set both primary and secondary prescalers to the value of 1:1.

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REGISTER 17-3: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	R-0, HSC	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
bit 15						bit 8	

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7						bit 0	

Legend:	C = Clearable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	'0' = Bit is cleared	x = Bit is unknown
-n = Value at POR	'1' = Bit is set	U = Unimplemented bit, read as '0'	

- bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I²C master, applicable to master transmit operation)
 1 = NACK was received from slave
 0 = ACK was received from slave
 Hardware is set or clear at the end of a slave Acknowledge.
- bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
 1 = Master transmit is in progress (8 bits + ACK)
 0 = Master transmit is not in progress
 Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
- bit 13 **ACKTIM:** Acknowledge Time Status bit (I²C Slave mode only)
 1 = I²C bus is an Acknowledge sequence, set on the 8th falling edge of SCLx
 0 = Not an Acknowledge sequence, cleared on the 9th rising edge of SCLx
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10 **BCL:** Master Bus Collision Detect bit
 1 = A bus collision has been detected during a master operation
 0 = No bus collision detected
 Hardware is set at detection of a bus collision.
- bit 9 **GCSTAT:** General Call Status bit
 1 = General call address was received
 0 = General call address was not received
 Hardware is set when address matches the general call address. Hardware is clear at Stop detection.
- bit 8 **ADD10:** 10-Bit Address Status bit
 1 = 10-bit address was matched
 0 = 10-bit address was not matched
 Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
- bit 7 **IWCOL:** I2Cx Write Collision Detect bit
 1 = An attempt to write to the I2CxTRN register failed because the I²C module is busy
 0 = No collision
 Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
- bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
 1 = A byte was received while the I2CxRCV register was still holding the previous byte
 0 = No overflow
 Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5 **D_A:** Data/Address bit (I²C Slave mode only)
 1 = Indicates that the last byte received was data
 0 = Indicates that the last byte received was a device address
 Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

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REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled
- bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active
- bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected
- bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected
- bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state
- bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1: Refer to “**Universal Asynchronous Receiver Transmitter (UART)**” (DS70000582) in the “*dsPIC33/PIC24 Family Reference Manual*” for information on enabling the UARTx module for transmit operation.

19.0 HIGH-SPEED, 12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**12-Bit High-Speed, Multiple SARs A/D Converter (ADC)**” (DS70005213) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

dsPIC33EPXXGS50X devices have a high-speed, 12-bit Analog-to-Digital Converter (ADC) that features a low conversion latency, high resolution and oversampling capabilities to improve performance in AC/DC, DC/DC power converters.

19.1 Features Overview

The High Speed, 12-Bit Multiple SARs Analog-to-Digital Converter (ADC) includes the following features:

- Five ADC Cores: Four Dedicated Cores and One Shared (Common) Core
- User-Configurable Resolution of up to 12 Bits for each Core
- Up to 3.25 Msps Conversion Rate per Channel at 12-Bit Resolution
- Low-Latency Conversion
- Up to 22 Analog Input Channels, with a Separate 16-Bit Conversion Result Register for each Input
- Conversion Result can be Formatted as Unsigned or Signed Data, on a per Channel Basis, for All Channels
- Single-Ended and Pseudodifferential Conversions are available on All ADC Cores

- Simultaneous Sampling of up to 5 Analog Inputs
- Channel Scan Capability
- Multiple Conversion Trigger Options for each Core, including:
 - PWM1 through PWM5 (primary and secondary triggers, and current-limit event trigger)
 - PWM Special Event Trigger
 - Timer1/Timer2 period match
 - Output Compare 1 and event trigger
 - External pin trigger event (ADTRG31)
 - Software trigger
- Two Integrated Digital Comparators with Dedicated Interrupts:
 - Multiple comparison options
 - Assignable to specific analog inputs
- Two Oversampling Filters with Dedicated Interrupts:
 - Provide increased resolution
 - Assignable to a specific analog input

The module consists of five independent SAR ADC cores. Simplified block diagrams of the Multiple SARs 12-Bit ADC are shown in Figure 19-1, Figure 19-2 and Figure 19-3.

The analog inputs (channels) are connected through multiplexers and switches to the Sample-and-Hold (S&H) circuit of each ADC core. The core uses the channel information (the output format, the measurement mode and the input number) to process the analog sample. When conversion is complete, the result is stored in the result buffer for the specific analog input, and passed to the digital filter and digital comparator if they were configured to use data from this particular channel.

The ADC module can sample up to five inputs at a time (four inputs from the dedicated SAR cores and one from the shared SAR core). If multiple ADC inputs request conversion on the shared core, the module will convert them in a sequential manner, starting with the lowest order input.

The ADC provides each analog input the ability to specify its own trigger source. This capability allows the ADC to sample and convert analog inputs that are associated with PWM generators operating on independent time bases.

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REGISTER 19-7: ADCON4L: ADC CONTROL REGISTER 4 LOW

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SYNCTRG3	SYNCTRG2	SYNCTRG1	SYNCTRG0
bit 15				bit 8			

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SAMC3EN	SAMC2EN	SAMC1EN	SAMC0EN
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **SYNCTRG3:** Dedicated ADC Core 3 Trigger Synchronization bit

1 = All triggers are synchronized with the core source clock (TCORESRC)

0 = The ADC core triggers are not synchronized

bit 10 **SYNCTRG2:** Dedicated ADC Core 2 Trigger Synchronization bit

1 = All triggers are synchronized with the core source clock (TCORESRC)

0 = The ADC core triggers are not synchronized

bit 9 **SYNCTRG1:** Dedicated ADC Core 1 Trigger Synchronization bit

1 = All triggers are synchronized with the core source clock (TCORESRC)

0 = The ADC core triggers are not synchronized

bit 8 **SYNCTRG0:** Dedicated ADC Core 0 Trigger Synchronization bit

1 = All triggers are synchronized with the core source clock (TCORESRC)

0 = The ADC core triggers are not synchronized

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **SAMC3EN:** Dedicated ADC Core 3 Conversion Delay Enable bit

1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCORE3L register

0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle

bit 2 **SAMC2EN:** Dedicated ADC Core 2 Conversion Delay Enable bit

1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCORE2L register

0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle

bit 1 **SAMC1EN:** Dedicated ADC Core 1 Conversion Delay Enable bit

1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCORE1L register

0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle

bit 0 **SAMC0EN:** Dedicated ADC Core 0 Conversion Delay Enable bit

1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCORE0L register

0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle

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REGISTER 19-19: ADMOD0L: ADC INPUT MODE CONTROL REGISTER 0 LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-1(odd) **DIFF<7:0>**: Differential-Mode for Corresponding Analog Inputs bits

1 = Channel is differential

0 = Channel is single-ended

bit 14-0 (even) **SIGN<7:0>**: Output Data Sign for Corresponding Analog Inputs bits

1 = Channel output data is signed

0 = Channel output data is unsigned

REGISTER 19-20: ADMOD0H: ADC INPUT MODE CONTROL REGISTER 0 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-1(odd) **DIFF<15:8>**: Differential-Mode for Corresponding Analog Inputs bits

1 = Channel is differential

0 = Channel is single-ended

bit 14-0 (even) **SIGN<15:8>**: Output Data Sign for Corresponding Analog Inputs bits

1 = Channel output data is signed

0 = Channel output data is unsigned

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REGISTER 19-27: ADTRIGxH: ADC CHANNEL TRIGGER x SELECTION REGISTER HIGH (x = 0 to 5)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRC(4x+3)<4:0>				
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TRGSRC(4x+2)<4:0>				
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC(4x+3)<4:0>:** Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31
11110 = Reserved
11101 = Reserved
11100 = PWM Generator 5 current-limit trigger
11011 = PWM Generator 4 current-limit trigger
11010 = PWM Generator 3 current-limit trigger
11001 = PWM Generator 2 current-limit trigger
11000 = PWM Generator 1 current-limit trigger
10111 = Output Compare 2 trigger
10110 = Output Compare 1 trigger
10101 = Reserved
10100 = Reserved
10011 = PWM Generator 5 secondary trigger
10010 = PWM Generator 4 secondary trigger
10001 = PWM Generator 3 secondary trigger
10000 = PWM Generator 2 secondary trigger
01111 = PWM Generator 1 secondary trigger
01110 = PWM secondary Special Event Trigger
01101 = Timer2 period match
01100 = Timer1 period match
01011 = Reserved
01010 = Reserved
01001 = PWM Generator 5 primary trigger
01000 = PWM Generator 4 primary trigger
00111 = PWM Generator 3 primary trigger
00110 = PWM Generator 2 primary trigger
00101 = PWM Generator 1 primary trigger
00100 = PWM Special Event Trigger
00011 = Reserved
00010 = Level software trigger
00001 = Common software trigger
00000 = No trigger is enabled

bit 7-5 **Unimplemented:** Read as '0'

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23.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXGS50X family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation
- Brown-out Reset (BOR)

23.1 Configuration Bits

In dsPIC33EPXXGS50X family devices, the Configuration Words are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the end of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 23-1 with detailed descriptions in Table 23-2. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration Shadow registers during device Resets.

For devices operating in Dual Partition modes, the BSEQx bits (FBTSEQ<11:0>) determine which panel is the Active Partition at start-up and the Configuration Words from that panel are loaded into the Configuration Shadow registers.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Words for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled. Program code executing out of configuration space will cause a device Reset.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration Words.

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TABLE 24-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier Working register pair for Square instructions $\in \{W4 * W4, W5 * W5, W6 * W6, W7 * W7\}$
Wm*Wn	Multiplicand and Multiplier Working register pair for DSP instructions $\in \{W4 * W5, W4 * W6, W4 * W7, W5 * W6, W5 * W7, W6 * W7\}$
Wn	One of 16 Working registers $\in \{W0...W15\}$
Wnd	One of 16 Destination Working registers $\in \{W0...W15\}$
Wns	One of 16 Source Working registers $\in \{W0...W15\}$
WREG	W0 (Working register used in file register instructions)
Ws	Source W register $\in \{Ws, [Ws], [Ws++] , [Ws--], [++Ws], [--Ws] \}$
Wso	Source W register $\in \{Wns, [Wns], [Wns++] , [Wns--], [++Wns], [--Wns], [Wns+Wb] \}$
Wx	X Data Space Prefetch Address register for DSP instructions $\in \{[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], \text{none}\}$
Wxd	X Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$
Wy	Y Data Space Prefetch Address register for DSP instructions $\in \{[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], \text{none}\}$
Wyd	Y Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$

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FIGURE 26-2: EXTERNAL CLOCK TIMING

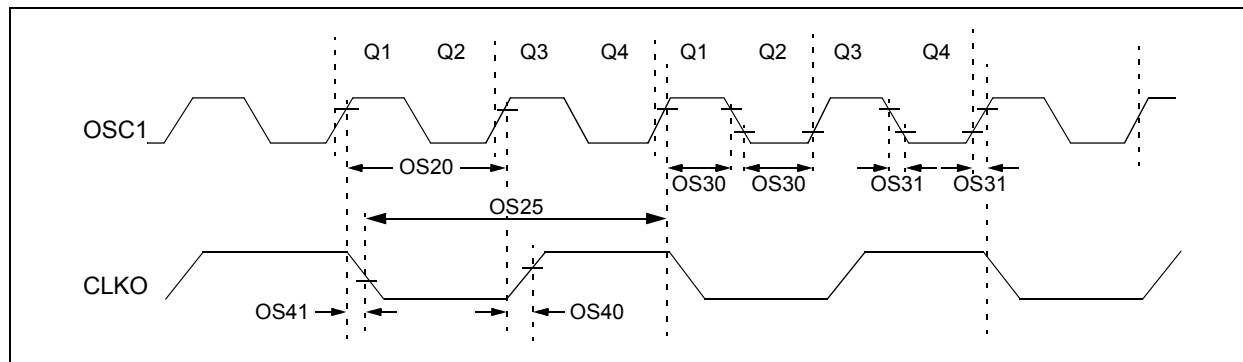


TABLE 26-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symb	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	60	MHz	EC
		Oscillator Crystal Frequency	3.5 10	— —	10 40	MHz MHz	XT HS
OS20	Tosc	Tosc = 1/Fosc	8.33	—	DC	ns	+125°C
		Tosc = 1/Fosc	7.14	—	DC	ns	+85°C
OS25	Tcy	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	+125°C
		Instruction Cycle Time ⁽²⁾	14.28	—	DC	ns	+85°C
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x Tosc	—	0.55 x Tosc	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ^(3,4)	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time ^(3,4)	—	5.2	—	ns	
OS42	GM	External Oscillator Transconductance ⁽⁴⁾	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25°C

Note 1: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

2: Instruction cycle period (Tcy) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Minimum” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “Maximum” cycle time limit is “DC” (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4: This parameter is characterized but not tested in manufacturing.

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FIGURE 26-9: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS

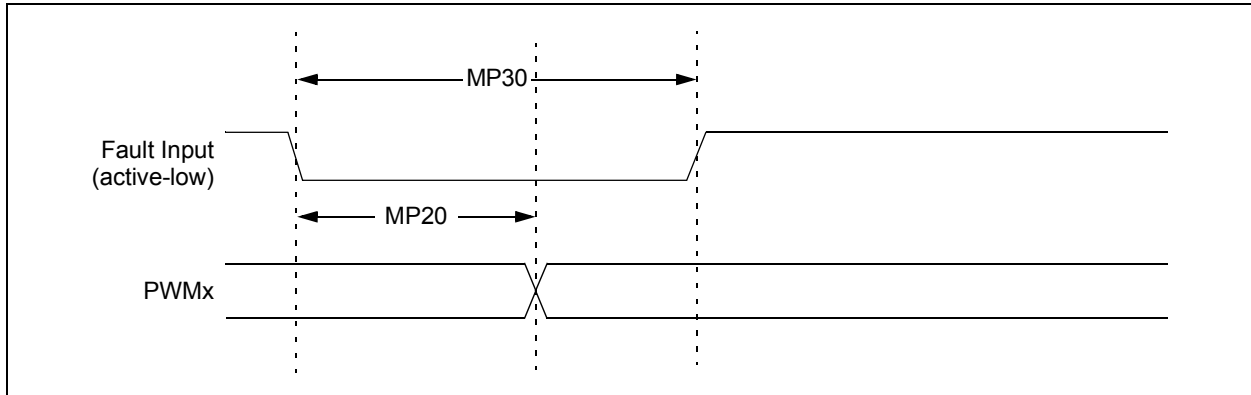


FIGURE 26-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS

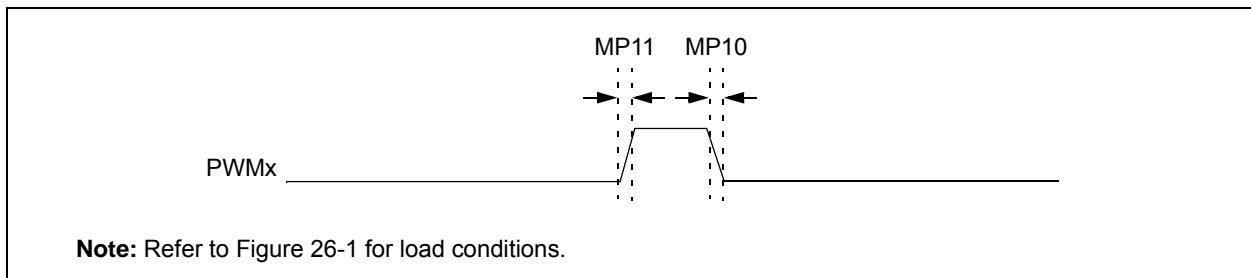


TABLE 26-30: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
MP10	T _{FPWM}	PWMx Output Fall Time	—	—	—	ns	See Parameter DO32
MP11	T _{RPWM}	PWMx Output Rise Time	—	—	—	ns	See Parameter DO31
MP20	T _{FD}	Fault Input ↓ to PWMx I/O Change	—	—	15	ns	
MP30	T _{FH}	Fault Input Pulse Width	15	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

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