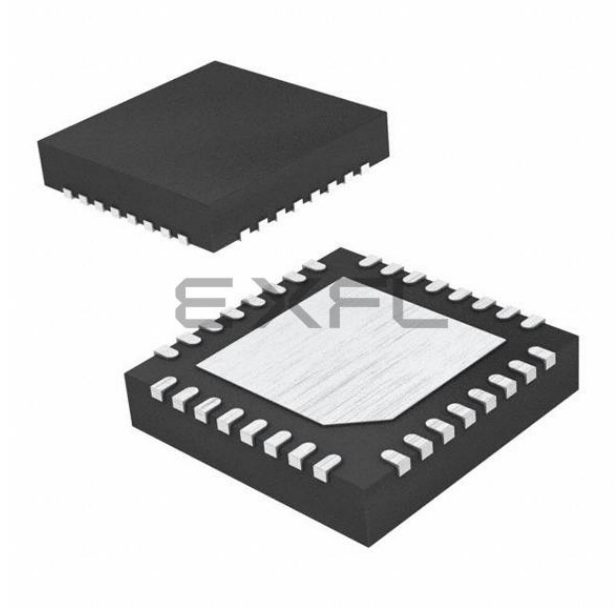
Microchip Technology - DSPIC33EP64GS502T-E/MM Datasheet



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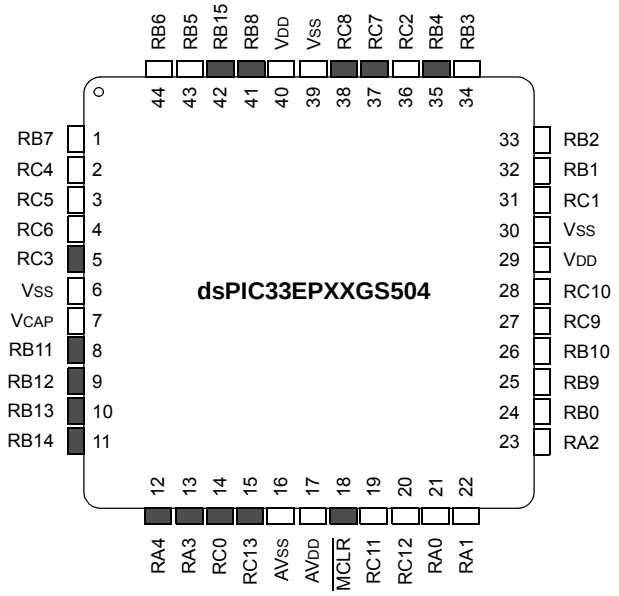
Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs502t-e-mm

Pin Diagrams (Continued)

44-Pin TQFP



Pin	Pin Function	Pin	Pin Function
1	PGEC1/AN21/SDA1/**RP39**/RB7	23	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2
2	AN1ALT/**RP52**/RC4	24	AN3/PGA2P3/CMP1D/CMP2B/**RP32**/RB0
3	AN0ALT/**RP53**/RC5	25	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9
4	AN17/**RP54**/RC6	26	AN5/CMP2D/CMP3B/ISRC3/**RP42**/RB10
5	**RP51**/RC3	27	AN11/PGA1N3/**RP57**/RC9
6	VSS	28	AN10/PGA1P4/EXTREF2/**RP58**/RC10
7	VCAP	29	VDD
8	TMS/PWM3H/**RP43**/RB11	30	VSS
9	TCK/PWM3L/**RP44**/RB12	31	AN8/PGA2P4/CMP4C/**RP49**/RC1
10	PWM2H/**RP45**/RB13	32	OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1
11	PWM2L/**RP46**/RB14	33	OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/**RP34**/RB2
12	PWM1H/RA4	34	PGED2/AN18/DACOUT1/INT0/**RP35**/RB3
13	PWM1L/RA3	35	PGEC2/ADTRG31/**RP36**/RB4
14	FLT12/**RP48**/RC0	36	AN9/CMP4D/EXTREF1/**RP50** /RC2
15	FLT11/**RP61**/RC13	37	ASDA1/**RP55**/RC7
16	AVSS	38	ASCL1/**RP56**/RC8
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	AN12/ISRC1/**RP59**/RC11	41	PGED3/SDA2/FLT31/**RP40**/RB8
20	AN14/PGA2N3/**RP60**/RC12	42	PGEC3/SCL2/**RP47**/RB15
21	AN0/PGA1P1/CMP1A/RA0	43	TDO/AN19/PGA2N2/**RP37**/RB5
22	AN1/PGA1P2/PGA2P1/CMP1B/RA1	44	PGED1/TDI/AN20/SCL1/**RP38**/RB6

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules. This pin must be connected at all times.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output
Analog = Analog input
P = Power
ST = Schmitt Trigger input with CMOS levels
O = Output
I = Input
PPS = Peripheral Pin Select
TTL = TTL input buffer

1: Not all pins are available in all packages variants. See the **"Pin Diagrams"** section for pin availability.

2: These pins are dedicated on 64-pin devices.

FIGURE 2-6: OFF-LINE UPS

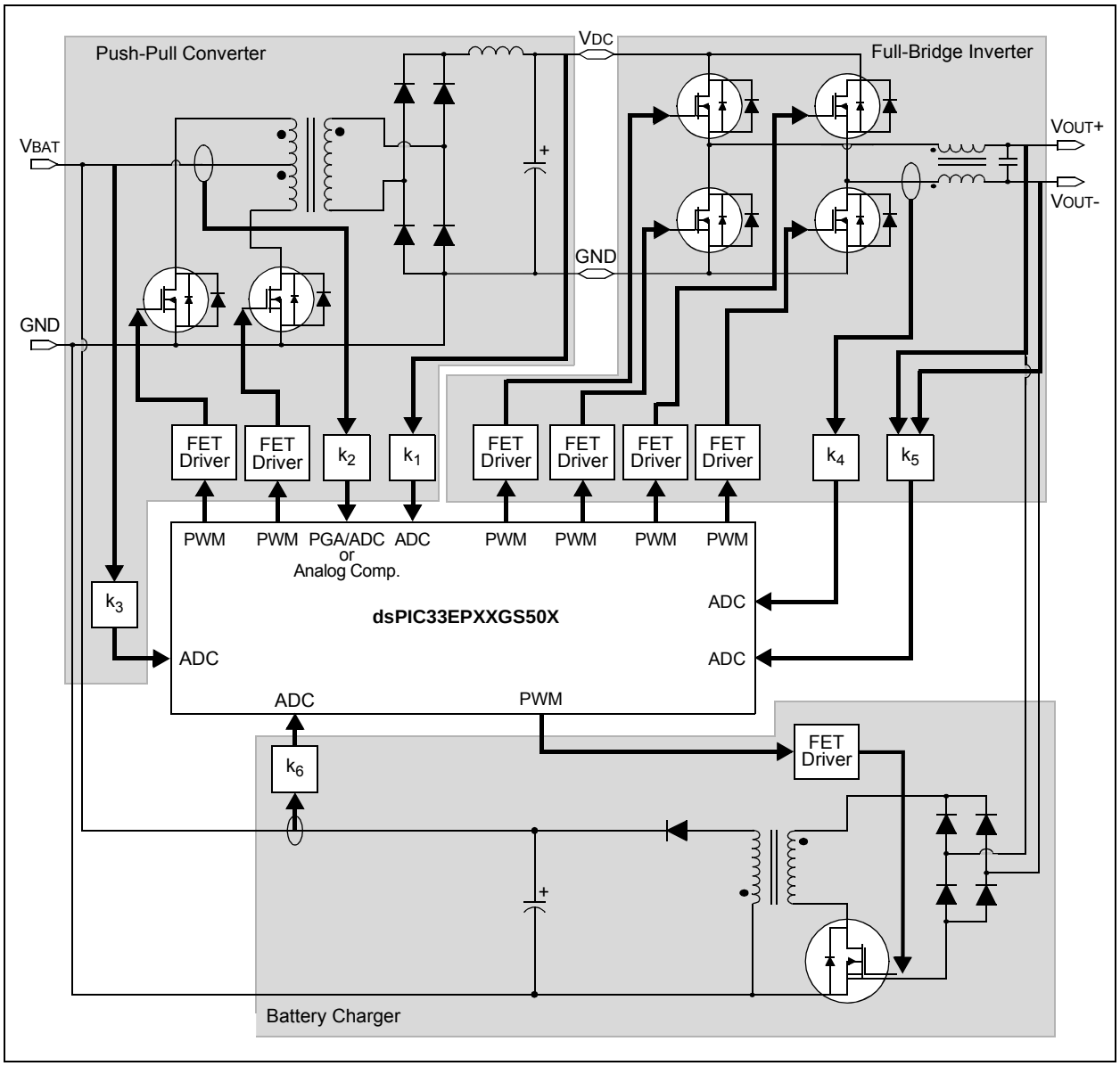
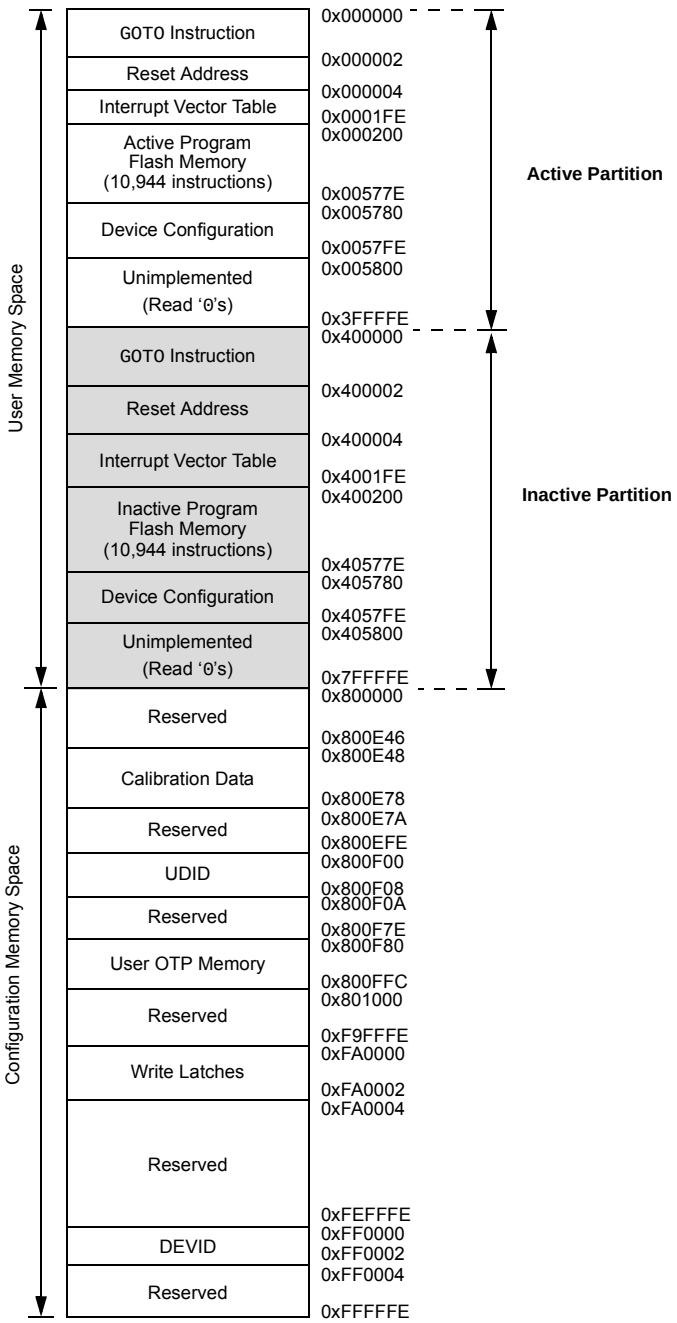
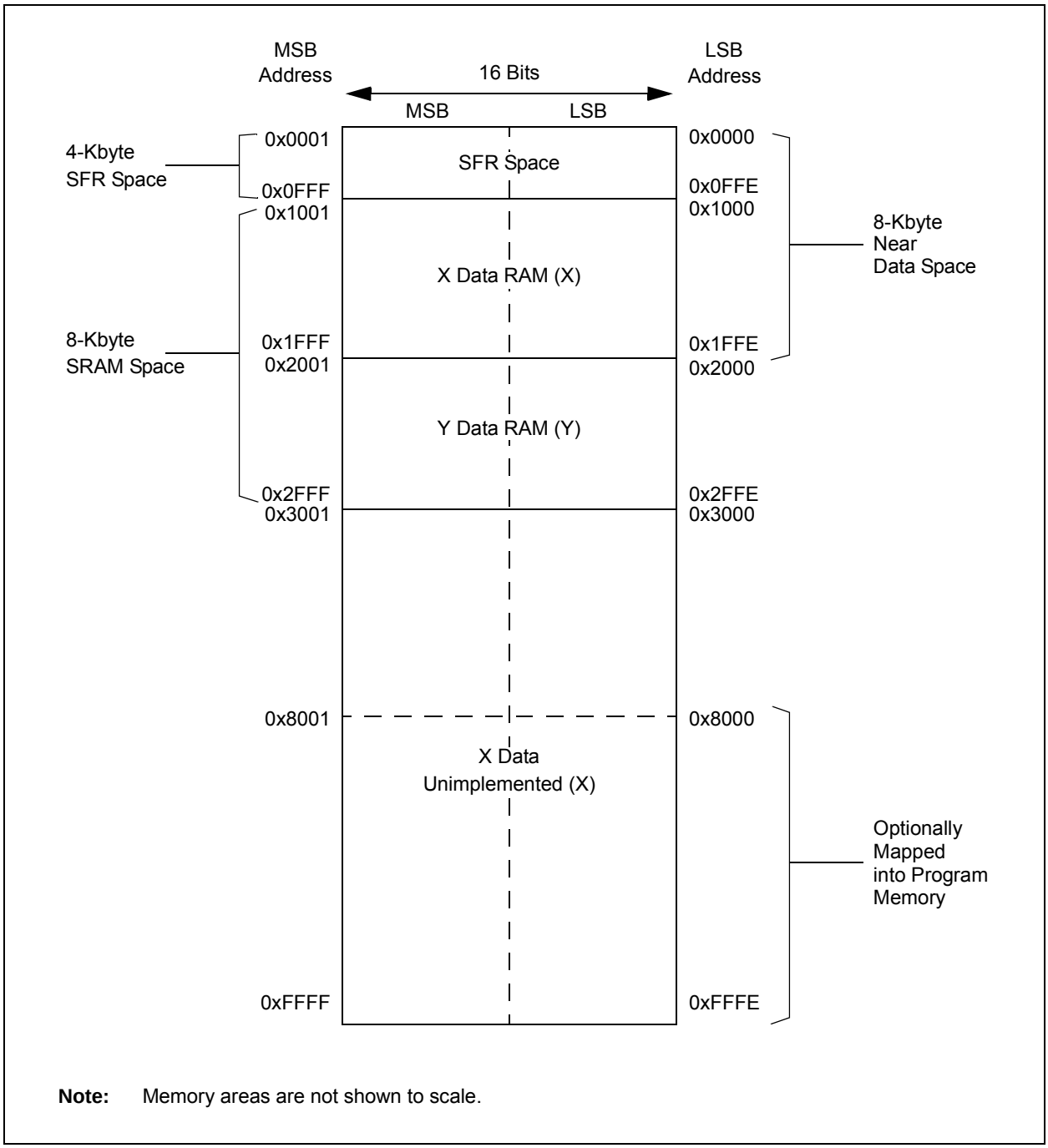


FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP64GS50X DEVICES (DUAL PARTITION)



Note: Memory areas are not shown to scale.

FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64GS50X DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	NVMIF	—	ADCIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	—	—	—	—	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	—	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	PSEMIF	—	—	INT4IF	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	—	—	—	—	PSESIF	—	—	—	—	—	—	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—		—	—	—	—	—	—	—	0000
IFS6	080C	ADCAN1IF	ADCAN0IF	—	—	—	—	AC4IF	AC3IF	AC2IF	—	—	—	—	PWM5IF	PWM4IF	PWM3IF	0000
IFS7	080E	—	—	—	—	—	—	—	—	—	—	ADCAN7IF	ADCAN6IF	ADCAN5IF	ADCAN4IF	ADCAN3IF	ADCAN2IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	ADCAN16IF(1)	ADCAN15IF(1)	ADCAN14IF(2)	ADCAN13IF(1)	ADCAN12IF(2)	ADCAN11IF(2)	ADCAN10IF(2)	ADCAN9IF(2)	ADCAN8IF(2)	—	—	—	—	—	—	—	0000
IFS10	0814	—	I2C2BCIF	I2C1BCIF	—	—	—	—	—	—	—	—	ADCAN21IF	ADCAN20IF	ADCAN19IF	ADCAN18IF	ADCAN17IF(2)	0000
IFS11	0816	—	—	—	—	—	—	—	—	—	—	—	ADFLTR1IF	ADFLTR0IF	ADCMP1IF	ADCMP0IF	—	0000
IEC0	0820	NVMIE	—	ADCIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	—	—	—	—	INT1IE	CNIE	AC1IF	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	—	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	PSEMIE	—	—	INT4IE	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	—	—	—	—	PSESIE	—	—	—	—	—	—	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	ADCAN1IE	ADCAN0IE	—	—	—	—	AC4IE	AC3IE	AC2IE	—	—	—	—	PWM5IE	PWM4IE	PWM3IE	0000
IEC7	082E	—	—	—	—	—	—	—	—	—	—	ADCAN7IE	ADCAN6IE	ADCAN5IE	ADCAN4IE	ADCAN3IE	ADCAN2IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	ADCAN16IE(1)	ADCAN15IE(1)	ADCAN14IE(2)	ADCAN13IE(1)	ADCAN12IE(2)	ADCAN11IE(2)	ADCAN10IE(2)	ADCAN9IE(2)	ADCAN8IE(2)	—	—	—	—	—	—	—	0000
IEC10	0834	—	I2C2BCIE	I2C1BCIE	—	—	—	—	—	—	—	—	ADCAN21IE	ADCAN20IE	ADCAN19IE	ADCAN18IE	ADCAN17IE(2)	0000
IEC11	0836	—	—	—	—	—	—	—	—	—	—	—	ADFLTR1IE	ADFLTR0IE	ADCMP1IE	ADCMP0IE	—	0000
IPC0	0840	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	0842	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	—	—	—	4440
IPC2	0844	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	0846	—	NVMIP2	NVMIP1	NVMIP0	—	—	—	—	—	ADCIP2	ADCIP1	ADCIP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4044
IPC4	0848	—	CNIP2	CNIP1	CNIP0	—	AC1IP2	AC1IP1	AC1IP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0004
IPC6	084C	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	—	—	—	4440
IPC7	084E	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP2	SPI2IP1	SPI2IP0	—	SPI2EIP2	SPI2EIP1	SPI2EIP0	0044
IPC9	0852	—	—	—	—	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	—	—	—	0440

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Only available on dsPIC33EPXXGS506 devices.

2: Only available on dsPIC33EPXXGS504/505 and dsPIC33EPXXGS506 devices.

REGISTER 9-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CMPMD	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
—	—	—	—	—	—	I2C2MD	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9-2 **Unimplemented:** Read as '0'

bit 1 **I2C2MD:** I2C2 Module Disable bit
1 = I2C2 module is disabled
0 = I2C2 module is enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 9-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	REFOMD	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled

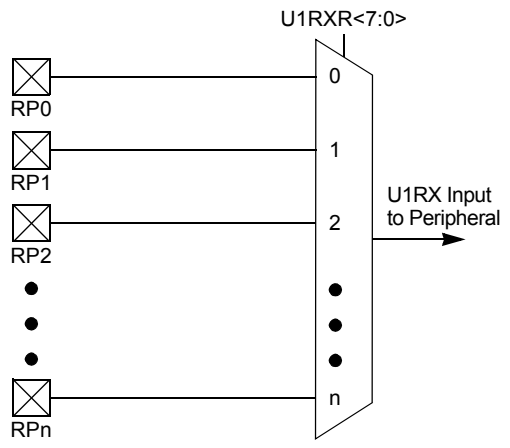
bit 2-0 **Unimplemented:** Read as '0'

10.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 10-1 through Register 10-19). Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 8-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 10-2 illustrates remappable pin selection for the U1RX input.

FIGURE 10-2: REMAPPABLE INPUT FOR U1RX



Note: For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

10.4.4.1 Virtual Connections

The dsPIC33EPXXGS50X devices support six virtual RPn pins (RP176-RP181), which are identical in functionality to all other RPn pins, with the exception of pinouts. These six pins are internal to the devices and are not connected to a physical device pin.

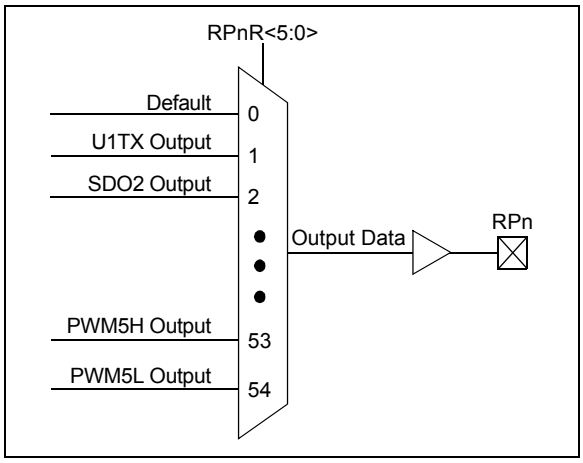
These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP176 and the PWM Fault input can be configured for RP176 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

10.4.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 10-20 through Register 10-38). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 10-2 and Figure 10-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 10-3: MULTIPLEXING REMAPPABLE OUTPUTS FOR RPn



10.4.5.1 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings, across any or all of the RPn pins, is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs, and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

REGISTER 12-2: TyCON: (TIMER3 AND TIMER5) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL(2)	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(1)	TCKPS1(1)	TCKPS0(1)	—	—	TCS(1,3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,3)
1 = External clock is from pin, TyCK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (TxCON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

2: When 32-bit timer operation is enabled (T32 = 1) in the Timerx Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

3: The TyCK pin is not available on all devices. See the **"Pin Diagrams"** section for the available pins.

REGISTER 15-12: PWMCONx: PWMx CONTROL REGISTER (x = 1 to 5)

R-0, HSC	R-0, HSC	R-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT(1)	CLSTAT(1)	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB(3)	MDCS(3)
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
DTC1	DTC0	—	—	MTBS	CAM(2,3,4)	XPRES(5)	IUE
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
- 1 = Fault interrupt is pending
- 0 = No Fault interrupt is pending
- This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
- 1 = Current-limit interrupt is pending
- 0 = No current-limit interrupt is pending
- This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
- 1 = Trigger interrupt is pending
- 0 = No trigger interrupt is pending
- This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
- 1 = Fault interrupt is enabled
- 0 = Fault interrupt is disabled and the FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
- 1 = Current-limit interrupt is enabled
- 0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
- 1 = A trigger event generates an interrupt request
- 0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(3)
- 1 = PHASEx/SPHASEx registers provide the time base period for this PWMx generator
- 0 = PTPER register provides timing for this PWMx generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(3)
- 1 = MDC register provides duty cycle information for this PWMx generator
- 0 = PDCx and SDCx registers provide duty cycle information for this PWMx generator

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.

2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

3: These bits should not be changed after the PWMx is enabled by setting PTEN = 1 (PTCON<15>).

4: Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.

5: Configure CLMOD = 0 (FCLCONx<8>) and ITB = 1 (PWMCONx<9>) to operate in External Period Reset mode.

REGISTER 15-22: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (x = 1 to 5)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL(1)	CLMOD
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL(1)	FLTMOD1	FLTMOD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IFLTMOD:** Independent Fault Mode Enable bit
1 = Independent Fault mode: Current-limit input maps FLTDAT1 to the PWMxH output and the Fault input maps FLTDAT0 to the PWMxL output; the CLDAT<1:0> bits are not used for override functions
0 = Normal Fault mode: Current-Limit mode maps CLDAT<1:0> bits to the PWMxH and PWMxL outputs; the PWM Fault mode maps FLTDAT<1:0> to the PWMxH and PWMxL outputs

bit 14-10 **CLSRC<4:0>:** Current-Limit Control Signal Source Select for PWMx Generator bits
11111 = Reserved
10001 = Reserved
10000 = Analog Comparator 4
01111 = Analog Comparator 3
01110 = Analog Comparator 2
01101 = Analog Comparator 1
01100 = Fault 12
01011 = Fault 11
01010 = Fault 10
01001 = Fault 9
01000 = Fault 8
00111 = Fault 7
00110 = Fault 6
00101 = Fault 5
00100 = Fault 4
00011 = Fault 3
00010 = Fault 2
00001 = Fault 1
00000 = Reserved

bit 9 **CLPOL:** Current-Limit Polarity for PWMx Generator bit(1)
1 = The selected current-limit source is active-low
0 = The selected current-limit source is active-high

bit 8 **CLMOD:** Current-Limit Mode Enable for PWMx Generator bit
1 = Current-Limit mode is enabled
0 = Current-Limit mode is disabled

Note 1: These bits should be changed only when PTEN = 0 (PTCON<15>).

REGISTER 17-3: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

bit 2 **R_W:** Read/Write Information bit (I^2C Slave mode only)
1 = Read – Indicates data transfer is output from the slave
0 = Write – Indicates data transfer is input to the slave
Hardware is set or clear after reception of an I^2C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit is in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.

REGISTER 19-15: ADEIEL: ADC EARLY INTERRUPT ENABLE REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EIEN<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EIEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **EIEN<15:0>:** Early Interrupt Enable for Corresponding Analog Inputs bits
1 = Early interrupt is enabled for the channel
0 = Early interrupt is disabled for the channel

REGISTER 19-16: ADEIEH: ADC EARLY INTERRUPT ENABLE REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	EIEN<21:16>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **EIEN<21:16>:** Early Interrupt Enable for Corresponding Analog Inputs bits
1 = Early interrupt is enabled for the channel
0 = Early interrupt is disabled for the channel

TABLE 23-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Description
BSS<1:0>	Boot Segment Code-Protect Level bits 11 = Boot Segment is not code-protected other than BWRP 10 = Standard security 0x = High security
BSEN	Boot Segment Control bit 1 = No Boot Segment is enabled 0 = Boot Segment size is determined by the BSLIM<12:0> bits
BWRP	Boot Segment Write-Protect bit 1 = Boot Segment can be written 0 = Boot Segment is write-protected
BSLIM<12:0>	Boot Segment Flash Page Address Limit bits Contains the last active Boot Segment page. The value to be programmed is the inverted page address, such that programming additional '0's can only increase the Boot Segment size (i.e., 0x1FFD = 2 Pages or 1024 IW).
GSS<1:0>	General Segment Code-Protect Level bits 11 = User program memory is not code-protected 10 = Standard security 0x = High security
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
CWRP	Configuration Segment Write-Protect bit 1 = Configuration data is not write-protected 0 = Configuration data is write-protected
CSS<2:0>	Configuration Segment Code-Protect Level bits 111 = Configuration data is not code-protected 110 = Standard security 10x = Enhanced security 0xx = High security
BTSWP	BOOTSWP Instruction Enable/Disable bit 1 = BOOTSWP instruction is disabled 0 = BOOTSWP instruction is enabled
BSEQ<11:0>	Boot Sequence Number bits (Dual Partition modes only) Relative value defining which partition will be active after device Reset; the partition containing a lower boot number will be active.
IBSEQ<11:0>	Inverse Boot Sequence Number bits (Dual Partition modes only) The one's complement of BSEQ<11:0>; must be calculated by the user and written for device programming. If BSEQx and IBSEQx are not complements of each other, the Boot Sequence Number is considered to be invalid.
AIVTDIS(1)	Alternate Interrupt Vector Table bit 1 = Alternate Interrupt Vector Table is disabled 0 = Alternate Interrupt Vector Table is enabled if INTCON2<8> = 1
IESO	Two-Speed Oscillator Start-up Enable bit 1 = Starts up device with FRC, then automatically switches to the user-selected oscillator source when ready 0 = Starts up device with the user-selected oscillator source
PWMLOCK	PWMx Lock Enable bit 1 = Certain PWMx registers may only be written after a key sequence 0 = PWMx registers may be written without a key sequence

Note 1: The Boot Segment must be present to use the Alternate Interrupt Vector Table.

TABLE 24-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier Working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier Working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 Working registers ∈ {W0...W15}
Wnd	One of 16 Destination Working registers ∈ {W0...W15}
Wns	One of 16 Source Working registers ∈ {W0...W15}
WREG	W0 (Working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7}

TABLE 26-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5(5,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7
DI60b	IICH	**Input High Injection Current**	0	—	+5(6,7,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins(7)
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and control pins)**	-20(9)	—	+20(9)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL | + | IICH |) ≤ ∑IICT

Note 1: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See the **"Pin Diagrams"** section for the 5V tolerant I/O pins.

5: VIL Source < (VSS – 0.3). Characterized but not tested.

6: VIH Source > (VDD + 0.3) for pins that are not 5V tolerant only.

7: Digital 5V tolerant pins do not have internal high-side diodes to VDD and cannot tolerate any "positive" input injection current.

8: Injection Currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 26-40: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(3)**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	µs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(1)	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25		µs	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode(1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	**(Note 2)**

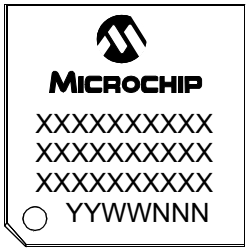
Note 1: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: Typical value for this parameter is 130 ns.

3: These parameters are characterized but not tested in manufacturing.

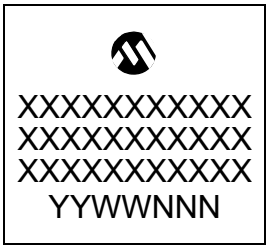
28.1 Package Marking Information (Continued)

44-Lead TQFP (10x10x1 mm)



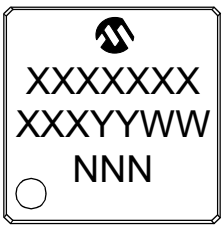
Example

44-Lead QFN (8x8 mm)



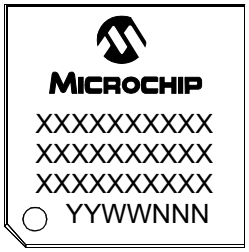
Example

48-Lead TQFP (7x7x1.0 mm)



Example

64-Lead TQFP (10x10x1 mm)



Example

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