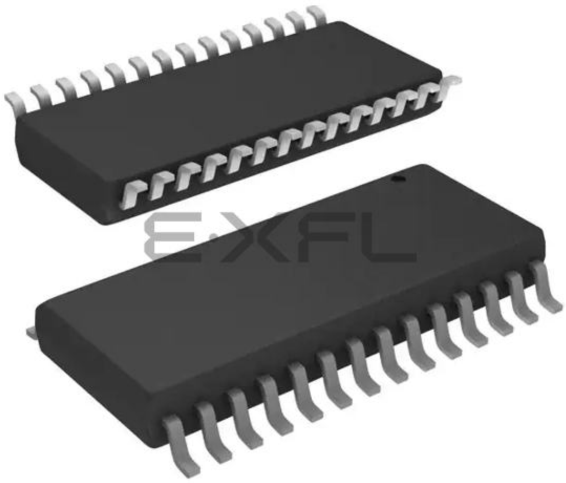
# Microchip Technology - DSPIC33EP64GS502T-E/SO Datasheet



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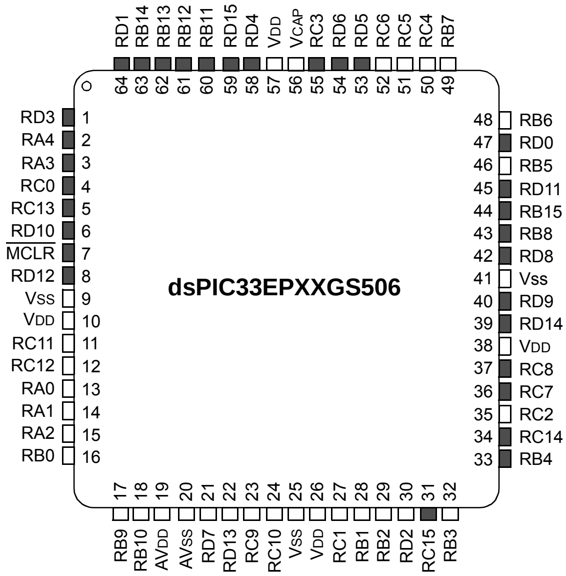
### Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 12x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs502t-e-so |

## Pin Diagrams (Continued)

**64-Pin TQFP**




| Pin | Pin Function | Pin | Pin Function |
|---|---|---|---|
| 1 | PWM4L/RD3 | 33 | PGEC2/ADTRG31/**RP36**/RB4 |
| 2 | PWM1H/RA4 | 34 | **RP62**/RC14 |
| 3 | PWM1L/RA3 | 35 | AN9/CMP4D/EXTREF1/**RP50**/RC2 |
| 4 | FLT12/**RP48**/RC0 | 36 | ASDA1/**RP55**/RC7 |
| 5 | FLT11/**RP61**/RC13 | 37 | ASCL1/**RP56**/RC8 |
| 6 | FLT10/RD10 | 38 | VDD |
| 7 | $\overline{\text{MCLR}}$ | 39 | RD14 |
| 8 | FLT9/T5CK/RD12 | 40 | RD9 |
| 9 | VSS | 41 | VSS |
| 10 | VDD | 42 | RD8 |
| 11 | AN12/ISRC1/**RP59**/RC11 | 43 | PGED3/SDA2/FLT31/**RP40**/RB8 |
| 12 | AN14/PGA2N3/**RP60**/RC12 | 44 | PGEC3/SCL2/**RP47**/RB15 |
| 13 | AN0/PGA1P1/CMP1A/RA0 | 45 | INT4/RD11 |
| 14 | AN1/PGA1P2/PGA2P1/CMP1B/RA1 | 46 | TDO/AN19/PGA2N2/**RP37**/RB5 |
| 15 | AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2 | 47 | T4CK/RD0 |
| 16 | AN3/PGA2P3/CMP1D/CMP2B/**RP32**/RB0 | 48 | PGED1/TDI/AN20/SCL1/**RP38**/RB6 |
| 17 | AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9 | 49 | PGEC1/AN21/SDA1/**RP39**/RB7 |
| 18 | AN5/CMP2D/CMP3B/ISRC3/**RP42**/RB10 | 50 | AN1ALT/**RP52**/RC4 |
| 19 | AVDD | 51 | AN0ALT/**RP53**/RC5 |
| 20 | AVSS | 52 | AN17/**RP54**/RC6 |
| 21 | AN15/RD7 | 53 | RD5 |
| 22 | AN13/DACOUT2/RD13 | 54 | PWM5H/RD6 |
| 23 | AN11/PGA1N3/**RP57**/RC9 | 55 | PWM5L/**RP51**/RC3 |
| 24 | AN10/PGA1P4/EXTREF2/**RP58**/RC10 | 56 | VCAP |
| 25 | VSS | 57 | VDD |
| 26 | VDD | 58 | RD4 |
| 27 | AN8/PGA2P4/CMP4C/**RP49**/RC1 | 59 | RD15 |
| 28 | OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1 | 60 | TMS/PWM3H/**RP43**/RB11 |
| 29 | OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/**RP34**/RB2 | 61 | TCK/PWM3L/**RP44**/RB12 |
| 30 | AN16/RD2 | 62 | PWM2H/**RP45**/RB13 |
| 31 | ASDA2/**RP63**/RC15 | 63 | PWM2L/**RP46**/RB14 |
| 32 | PGED2/AN18/DACOUT1/ASCL2/INT0/RP35/RB3 | 64 | PWM4H/RD1 |

**Legend:** **Shaded pins** are up to 5 VDC tolerant.
**RPn** represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name(1) | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| $\overline{\text{MCLR}}$ | I/P | ST | No | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| AVDD | P | P | No | Positive supply for analog modules. This pin must be connected at all times. |
| AVSS | P | P | No | Ground reference for analog modules. This pin must be connected at all times. |
| VDD | P | — | No | Positive supply for peripheral logic and I/O pins. |
| VCAP | P | — | No | CPU logic filter capacitor connection. |
| VSS | P | — | No | Ground reference for logic and I/O pins. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**1:** Not all pins are available in all packages variants. See the **"Pin Diagrams"** section for pin availability.

**2:** These pins are dedicated on 64-pin devices.

### REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

| | | |
|---|---|---|
| bit 2 | **SFA:** Stack Frame Active Status bit<br>1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG<br>0 = Stack frame is not active; W14 and W15 address the base Data Space | |
| bit 1 | **RND:** Rounding Mode Select bit<br>1 = Biased (conventional) rounding is enabled<br>0 = Unbiased (convergent) rounding is enabled | |
| bit 0 | **IF:** Integer or Fractional Multiplier Mode Select bit<br>1 = Integer mode is enabled for DSP multiply<br>0 = Fractional mode is enabled for DSP multiply | |

**Note 1:** This bit is always read as ‘0’.

**2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

### REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER

| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | CCTXI2 | CCTXI1 | CCTXI0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | MCTXI2 | MCTXI1 | MCTXI0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

| | |
|---|---|
| bit 15-11 | **Unimplemented:** Read as ‘0’ |
| bit 10-8 | **CCTXI<2:0>:** Current (W Register) Context Identifier bits<br>111 = Reserved<br>•<br>•<br>•<br>011 = Reserved<br>010 = Alternate Working Register Set 2 is currently in use<br>001 = Alternate Working Register Set 1 is currently in use<br>000 = Default register set is currently in use |
| bit 7-3 | **Unimplemented:** Read as ‘0’ |
| bit 2-0 | **MCTXI<2:0>:** Manual (W Register) Context Identifier bits<br>111 = Reserved<br>•<br>•<br>•<br>011 = Reserved<br>010 = Alternate Working Register Set 2 was most recently manually selected<br>001 = Alternate Working Register Set 1 was most recently manually selected<br>000 = Default register set was most recently manually selected |

## 5.6 Control Registers

Five SFRs are used to write and erase the program Flash memory: NVMCON, NVMKEY, NVMADR, NVMADRU and NVMSRCADR/H.

The NVMCON register (Register 5-1) selects the operation to be performed (page erase, word/row program, Inactive Partition erase), initiates the program or erase cycle and is used to determine the Active Partition in Dual Partition modes.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word/row for programming operations, or the selected page for erase operations. The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

For row programming operation, data to be written to program Flash memory is written into data memory space (RAM) at an address defined by the NVMSRCADR register (location of first element in row programming data).

**REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER (CONTINUED)**

bit 8 **URERR:** Row Programming Data Underrun Error bit
1 = Indicates row programming operation has been terminated
0 = No data underrun error is detected

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits(1,3,4)
1111 = Reserved
1110 = User memory Bulk Erase operation
1010 = Reserved
1001 = Reserved
1000 = Boot memory Double-Word Program operation in a Dual Partition Flash mode(7)
0101 = Reserved
0100 = Inactive Partition Memory Erase operation
0011 = Memory Page Erase operation
0010 = Memory Row Program operation
0001 = Memory Double-Word Program operation(5)
0000 = Reserved

**Note 1:** These bits can only be reset on a POR.
**2:** If this bit is set, power consumption will be further reduced ($I_{IDLE}$) and upon exiting Idle mode, there is a delay ($T_{VREG}$) before Flash memory becomes operational.
**3:** All other combinations of NVMOP<3:0> are unimplemented.
**4:** Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.
**5:** Two adjacent words on a 4-word boundary are programmed during execution of this operation.
**6:** Only available on dsPIC33EP64GS50X devices operating in Dual Partition mode. For all other devices, this bit is reserved.
**7:** The specific Boot mode depends on bits<1:0> of the programmed data:
11 = Single Partition Flash mode
10 = Dual Partition Flash mode
01 = Protected Dual Partition Flash mode
00 = Reserved

# 7.0 INTERRUPT CONTROLLER

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS50X family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXGS50X family CPU.

The interrupt controller has the following features:

- Six processor exceptions and software traps
- Seven user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies
- Alternate Interrupt Vector Table (AIVT) for debug support

## 7.1 Interrupt Vector Table

The dsPIC33EPXXGS50X family Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory, starting at location, 000004h. The IVT contains six non-maskable trap vectors and up to 246 sources of interrupts. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

### 7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT), shown in Figure 7-2, is available only when the Boot Segment is defined and the AIVT has been enabled. To enable the Alternate Interrupt Vector Table, the Configuration bit, AIVTDIS in the FSEC register, must be programmed and the AIVTEN bit must be set (INTCON2<8> = 1). When the AIVT is enabled, all interrupt and exception processes use the alternate vectors instead of the default vectors. The AIVT begins at the start of the last page of the Boot Segment, defined by BSLIM<12:0>. The second half of the page is no longer usable space. The Boot Segment must be at least 2 pages to enable the AIVT.

> **Note:** Although the Boot Segment must be enabled in order to enable the AIVT, application code does not need to be present inside of the Boot Segment. The AIVT (and IVT) will inherit the Boot Segment code protection.

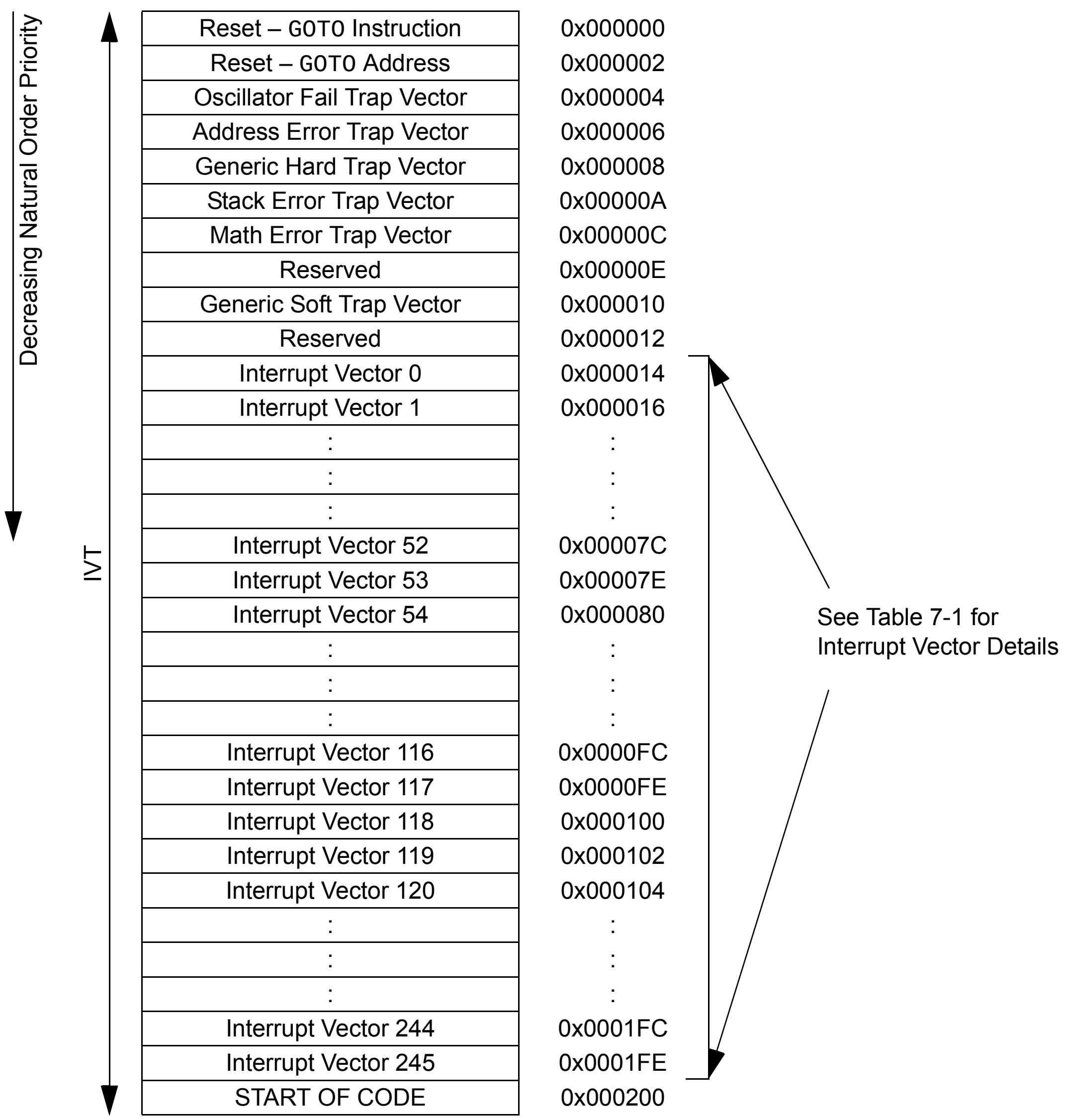
The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time.

## 7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXGS50X family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A `GOTO` instruction at the Reset address can redirect program execution to the appropriate start-up routine.

> **Note:** Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a `RESET` instruction.

**FIGURE 7-1: dsPIC33EPXXGS50X FAMILY INTERRUPT VECTOR TABLE**




**Note:** In Dual Partition modes, each partition has a dedicated Interrupt Vector Table.

## 7.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

### 7.3.1 KEY RESOURCES

- **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 7.4 Interrupt Control and Status Registers

dsPIC33EPXXGS50X family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

### 7.4.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior, contains the Global Interrupt Enable bit (GIE) and the Alternate Interrupt Vector Table Enable bit (AIVTEN).

INTCON3 contains the status flags for the Auxiliary PLL and DO stack overflow status trap sources.

The INTCON4 register contains the Software Generated Hard Trap Status bit (SGHT).

### 7.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

### 7.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

### 7.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt sources can be assigned to one of seven priority levels.

### 7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number (VECNUM<7:0>) and Interrupt Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP<2:0> bits in the first position of IPC0 (IPC0<2:0>).

### 7.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 through Register 7-7 in the following pages.

## 8.0 OSCILLATOR CONFIGURATION

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Oscillator Module"** (DS70005131) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXGS50X family oscillator system provides:

- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Configuration bits for clock source selection
- Auxiliary PLL for ADC and PWM

A simplified diagram of the oscillator system is shown in Figure 8-1.

**REGISTER 8-2: CLKDIV: CLOCK DIVISOR REGISTER**

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ROI | DOZE2(1) | DOZE1(1) | DOZE0(1) | DOZEN(2,3) | FRCDIV2 | FRCDIV1 | FRCDIV0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-1 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PLLPOST1 | PLLPOST0 | — | PLLPRE4 | PLLPRE3 | PLLPRE2 | PLLPRE1 | PLLPRE0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts will clear the DOZEN bit and the processor clock, and the peripheral clock ratio is set to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits(1)
111 = FCY divided by 128
110 = FCY divided by 64
101 = FCY divided by 32
100 = FCY divided by 16
011 = FCY divided by 8 (default)
010 = FCY divided by 4
001 = FCY divided by 2
000 = FCY divided by 1

bit 11 **DOZEN:** Doze Mode Enable bit(2,3)
1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock and peripheral clock ratio is forced to 1:1

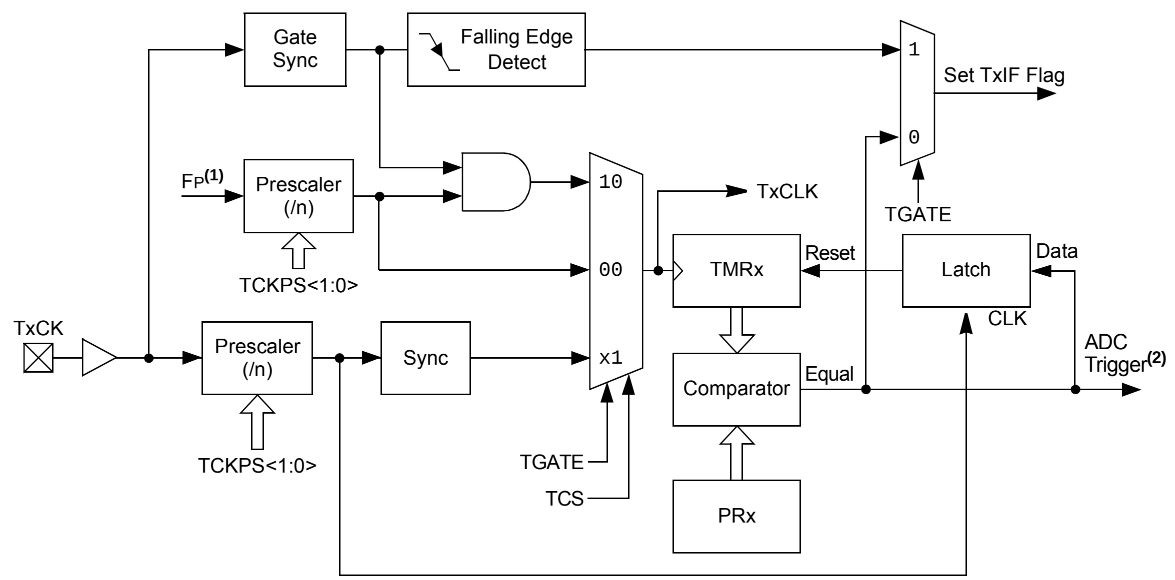
bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits
111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2
000 = FRC divided by 1 (default)

bit 7-6 **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as ‘N2’, PLL postscaler)
11 = Output divided by 8
10 = Reserved
01 = Output divided by 4 (default)
00 = Output divided by 2

bit 5 **Unimplemented:** Read as ‘0’

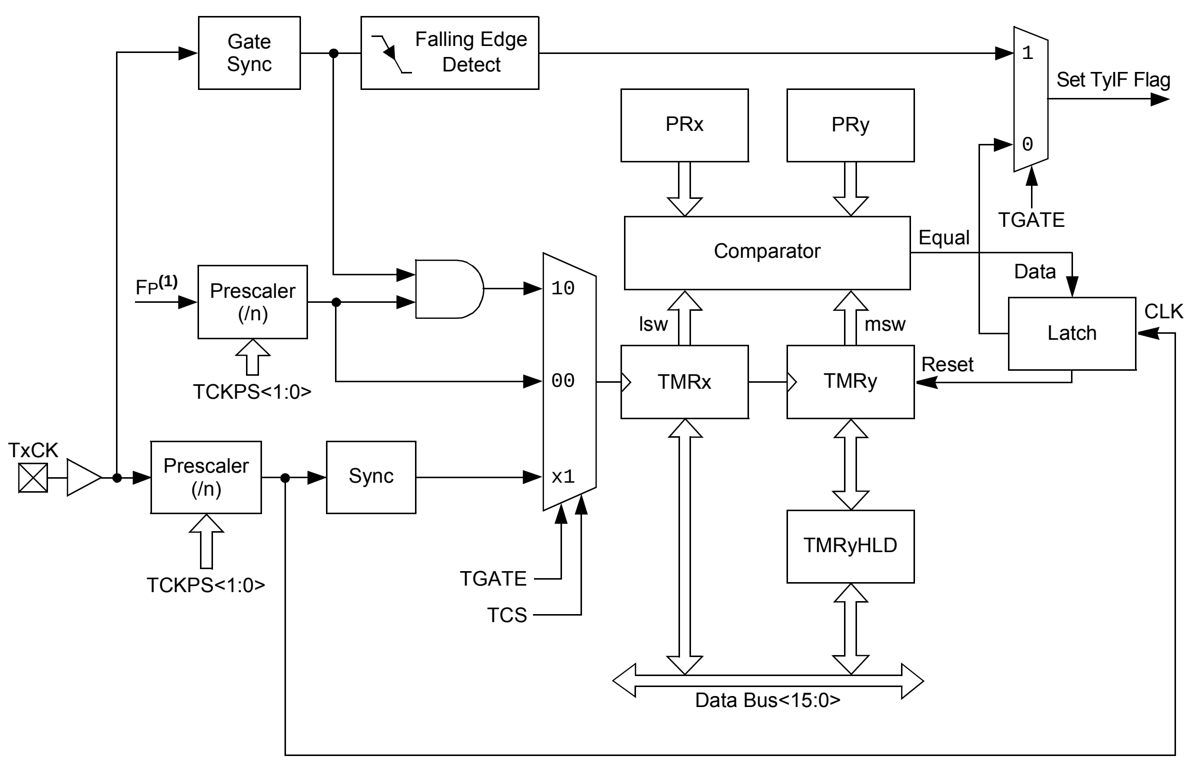
**Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
**2:** This bit is cleared when the ROI bit is set and an interrupt occurs.
**3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

**FIGURE 12-1: TIMERx BLOCK DIAGRAM (x = 2 THROUGH 5)**



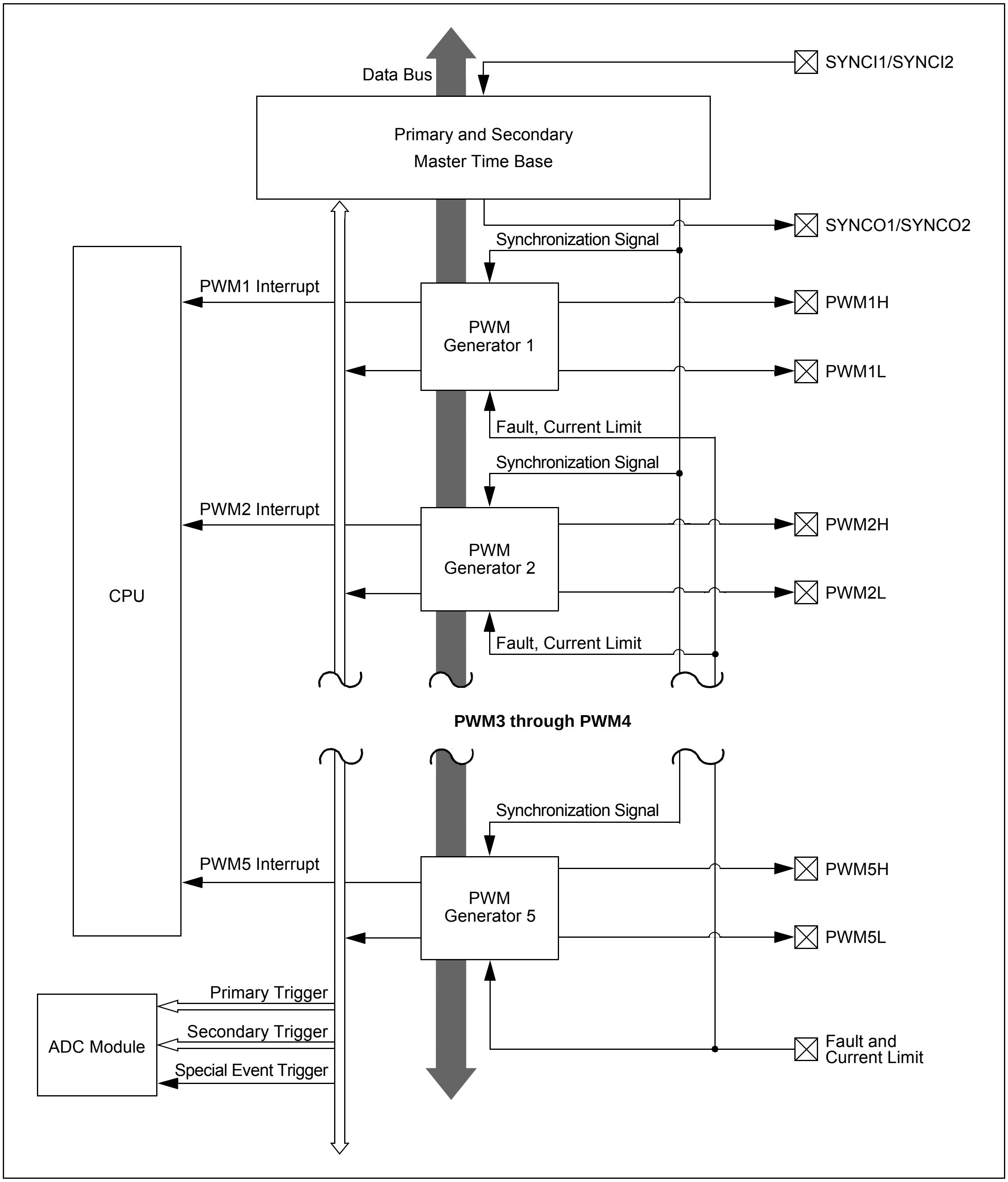

**Note 1:** FP is the peripheral clock.
**2:** The ADC trigger is only available on TMR2.

**FIGURE 12-2: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)**




**Note 1:** Timerx is a Type B timer (x = 2 and 4).
**2:** Timery is a Type C timer (y = 3 and 5).

**FIGURE 15-1: HIGH-SPEED PWM MODULE ARCHITECTURAL DIAGRAM**



### REGISTER 15-26: AUXCONx: PWMx AUXILIARY CONTROL REGISTER (x = 1 to 5)

| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| HRPDIS | HRDDIS | — | — | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSEL0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **HRPDIS:** High-Resolution PWMx Period Disable bit
1 = High-resolution PWMx period is disabled to reduce power consumption
0 = High-resolution PWMx period is enabled

bit 14 **HRDDIS:** High-Resolution PWMx Duty Cycle Disable bit
1 = High-resolution PWMx duty cycle is disabled to reduce power consumption
0 = High-resolution PWMx duty cycle is enabled

bit 13-12 **Unimplemented:** Read as ‘0’

bit 11-8 **BLANKSEL<3:0>:** PWMx State Blank Source Select bits
The selected state blank signal will block the current-limit and/or Fault input signals (if enabled via the BCH and BCL bits in the LEBCONx register).
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM5H is selected as the state blank source
0100 = PWM4H is selected as the state blank source
0011 = PWM3H is selected as the state blank source
0010 = PWM2H is selected as the state blank source
0001 = PWM1H is selected as the state blank source
0000 = No state blanking

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-2 **CHOPSEL<3:0>:** PWMx Chop Clock Source Select bits
The selected signal will enable and disable (chop) the selected PWMx outputs.
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM5H is selected as the chop clock source
0100 = PWM4H is selected as the chop clock source
0011 = PWM3H is selected as the chop clock source
0010 = PWM2H is selected as the chop clock source
0001 = PWM1H is selected as the chop clock source
0000 = Chop clock generator is selected as the chop clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit
1 = PWMxH chopping function is enabled
0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit
1 = PWMxL chopping function is enabled
0 = PWMxL chopping function is disabled

**REGISTER 15-27: PWMCAPx: PWMx PRIMARY TIME BASE CAPTURE REGISTER (x = 1 to 5)**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PWMCAP<12:5>(1,2,3,4) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| PWMCAP<4:0>(1,2,3,4) | | | | | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-3 **PWMCAP<12:0>:** PWMx Primary Time Base Capture Value bits(1,2,3,4)
The value in this register represents the captured PWMx time base value when a leading edge is detected on the current-limit input.

bit 2-0 **Unimplemented:** Read as ‘0’

**Note 1:** The capture feature is only available on a primary output (PWMxH).
**2:** This feature is active only after LEB processing on the current-limit input signal is complete.
**3:** The minimum capture resolution is 8.32 ns.
**4:** This feature can be used when the XPRES bit (PWMCONx<1>) is set to ‘0’.

## 21.1 Module Description

The Programmable Gain Amplifiers are used to amplify small voltages (i.e., voltages across burden/shunt resistors) to improve the signal-to-noise ratio of the measured signal. The PGAx output voltage can be read by any of the four dedicated Sample-and-Hold circuits on the ADC module. The output voltage can also be fed to the comparator module for overcurrent/ voltage protection. Figure 21-2 shows a functional block diagram of the PGAx module. Refer to **Section 19.0 “High-Speed, 12-Bit Analog-to-Digital Converter (ADC)”** and **Section 20.0 “High-Speed Analog Comparator”** for more interconnection details.

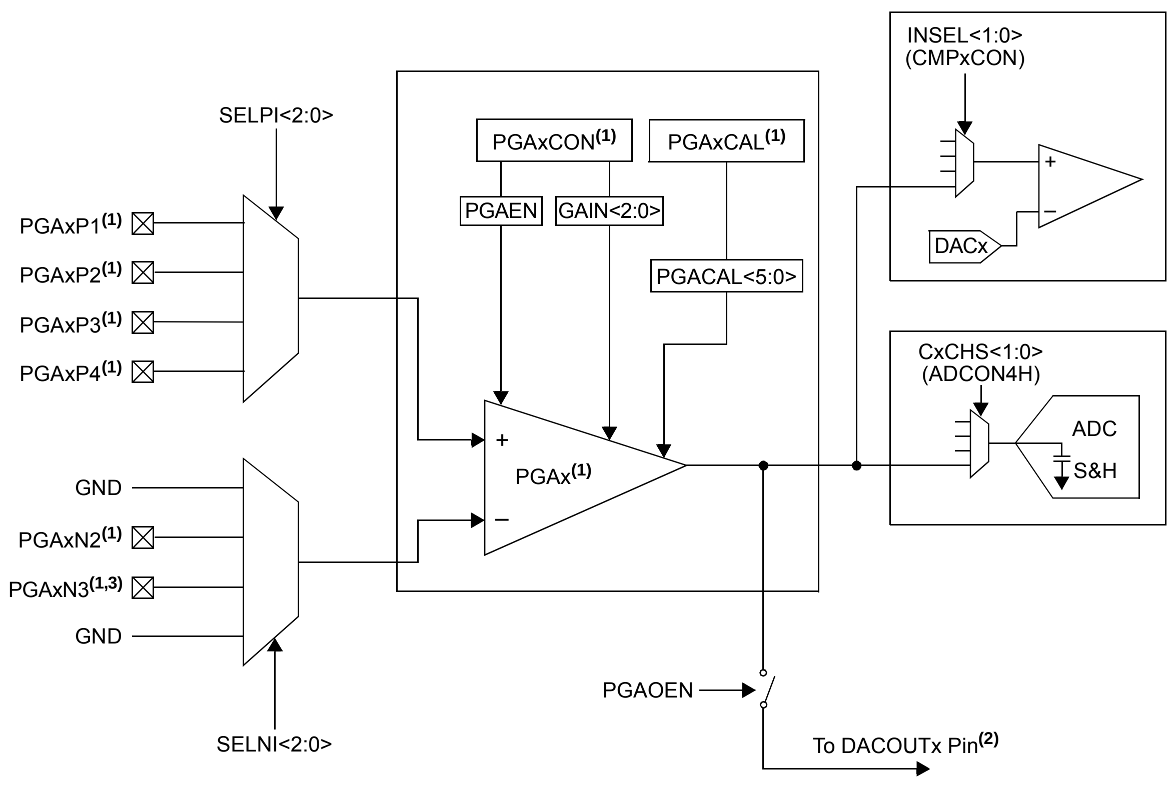
The gain of the PGAx module is selectable via the GAIN<2:0> bits in the PGAxCON register. There are five selectable gains, ranging from 4x to 64x. The SELPI<2:0> and SELNI<2:0> bits in the PGAxCON register select one of four positive/negative inputs to the PGAx module. For single-ended applications, the SELNI<2:0> bits will select the ground as the negative input source. To provide an independent ground reference, PGAxN2 and PGAxN3 pins are available as the negative input source to the PGAx module.

> **Note 1:** Not all PGA positive/negative inputs are available on all devices. Refer to the specific device pinout for available input source pins.

The output voltage of the PGAx module can be connected to the DACOUTx pin by setting the PGAOEN bit in the PGAxCON register. When the PGAOEN bit is enabled, the output voltage of PGA1 is connected to DACOUT1 and PGA2 is connected to DACOUT2. For devices with a single DACOUTx pin, the output voltage of PGA2 can be connected to DACOUT1 by configuring the DBCC Configuration bit in the FDEVOPT register (FDEVOPT<6>).

If both the DACx output voltage and PGAx output voltage are connected to the DACOUTx pin, the resulting output voltage would be a combination of signals. There is no assigned priority between the PGAx module and the DACx module.

**FIGURE 21-2: PGAx FUNCTIONAL BLOCK DIAGRAM**




**Note 1:** x = 1 and 2.
**2:** The DACOUT2 device pin is only available on 64-pin devices.
**3:** The PGAxN3 input is not available on 28-pin devices.

## 25.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

## 25.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

## 25.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 25.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

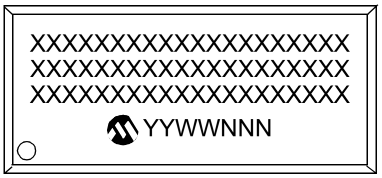
- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

**NOTES:**

# 28.0 PACKAGING INFORMATION

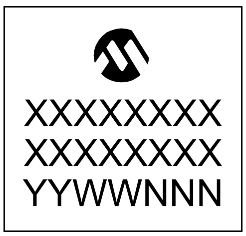
## 28.1 Package Marking Information

28-Lead SOIC (.300”)



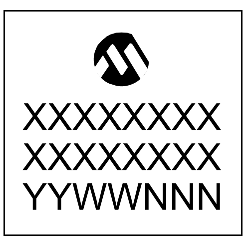

Example


28-Lead UQFN (6x6x0.55 mm)




Example


28-Lead QFN-S (6x6x0.9 mm)




Example

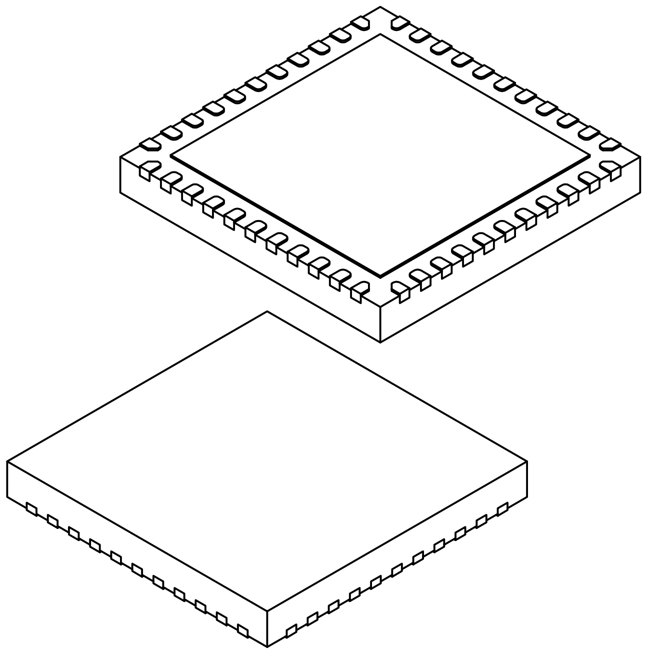

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| | Dimension Limits | MIN | NOM | MAX |
| Number of Pins | N | | 44 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 8.00 BSC | |
| Exposed Pad Width | E2 | 6.25 | 6.45 | 6.60 |
| Overall Length | D | | 8.00 BSC | |
| Exposed Pad Length | D2 | 6.25 | 6.45 | 6.60 |
| Terminal Width | b | 0.20 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103D Sheet 2 of 2