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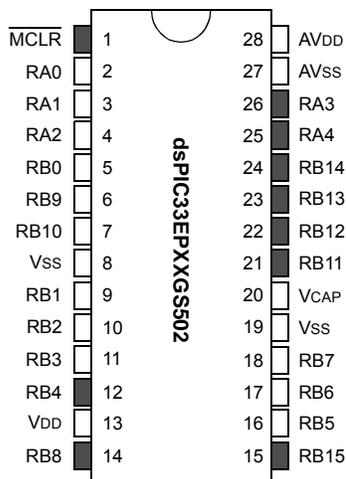
Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs504-e-pt

dsPIC33EPXXGS50X FAMILY

Pin Diagrams

28-Pin SOIC



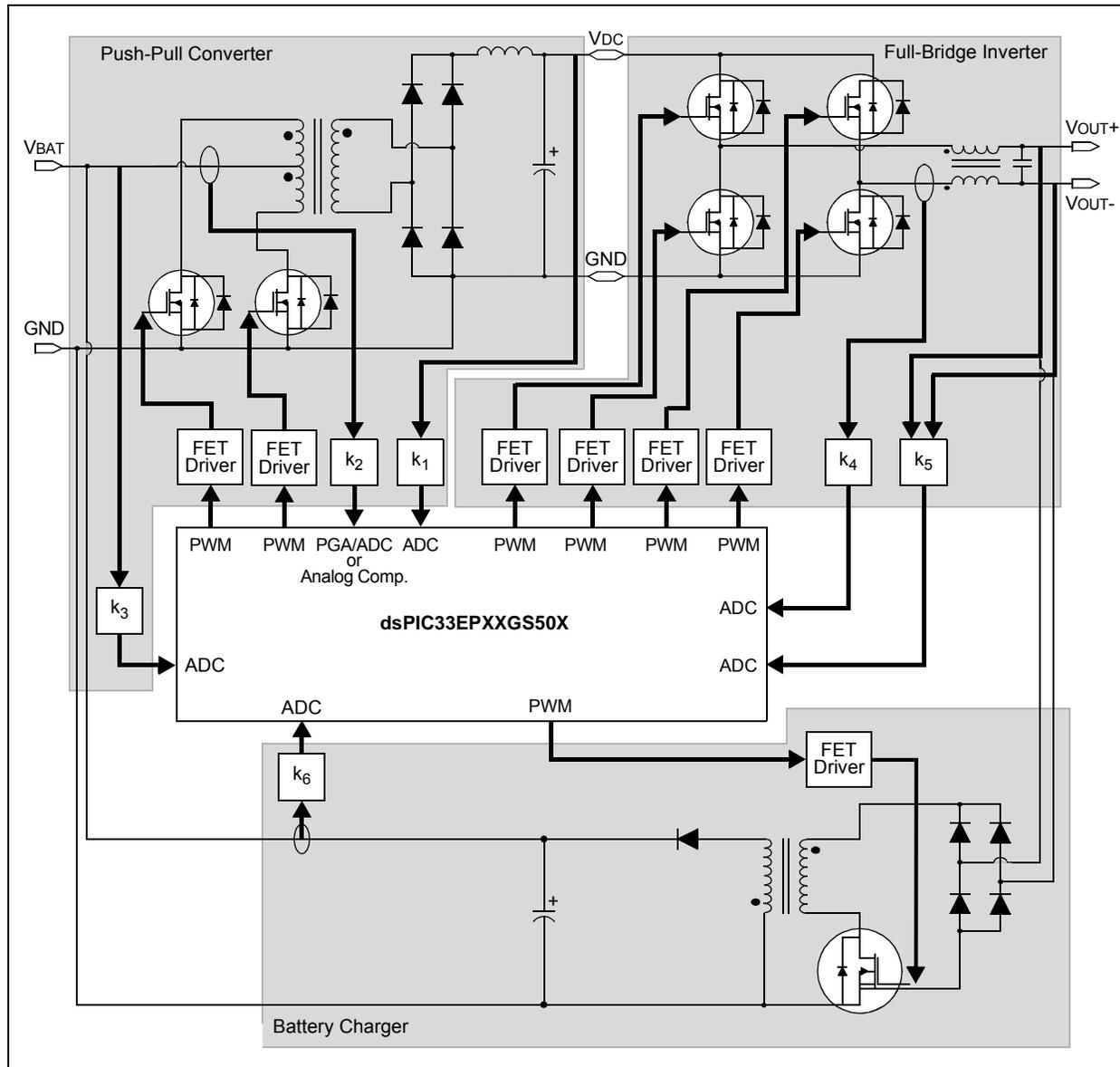
Pin	Pin Function	Pin	Pin Function
1	MCLR	15	PGEC3/SCL2/ RP47 /RB15
2	AN0/PGA1P1/CMP1A/RA0	16	TDO/AN19/PGA2N2/ RP37 /RB5
3	AN1/PGA1P2/PGA2P1/CMP1B/RA1	17	PGED1/TDI/AN20/SCL1/ RP38 /RB6
4	AN2/PGA1P3/PGA2P2/CMP1C/CMP2A/RA2	18	PGEC1/AN21/SDA1/ RP39 /RB7
5	AN3/PGA2P3/CMP1D/CMP2B/ RP32 /RB0	19	Vss
6	AN4/CMP2C/CMP3A/ISRC4/ RP41 /RB9	20	VCAP
7	AN5/CMP2D/CMP3B/ISRC3/ RP42 /RB10	21	TMS/PWM3H/ RP43 /RB11
8	Vss	22	TCK/PWM3L/ RP44 /RB12
9	OSC1/CLKI/AN6/CMP3C/CMP4A/ISRC2/ RP33 /RB1	23	PWM2H/ RP45 /RB13
10	OSC2/CLKO/AN7/PGA1N2/CMP3D/CMP4B/ RP34 /RB2	24	PWM2L/ RP46 /RB14
11	PGED2/AN18/DACOUT1/INT0/ RP35 /RB3	25	PWM1H/RA4
12	PGEC2/ADTRG31/EXTREF1/RP36/RB4	26	PWM1L/RA3
13	VDD	27	AVss
14	PGED3/SDA2/FLT31/RP40/RB8	28	AVDD

Legend: Shaded pins are up to 5 VDC tolerant.

RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

dsPIC33EPXXGS50X FAMILY

FIGURE 2-6: OFF-LINE UPS



dsPIC33EPXXGS50X FAMILY

3.5 Programmer's Model

The programmer's model for the dsPIC33EPXXGS50X family is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXGS50X devices contain control registers for Modulo Addressing, Bit-Reversed Addressing and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Table 3-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

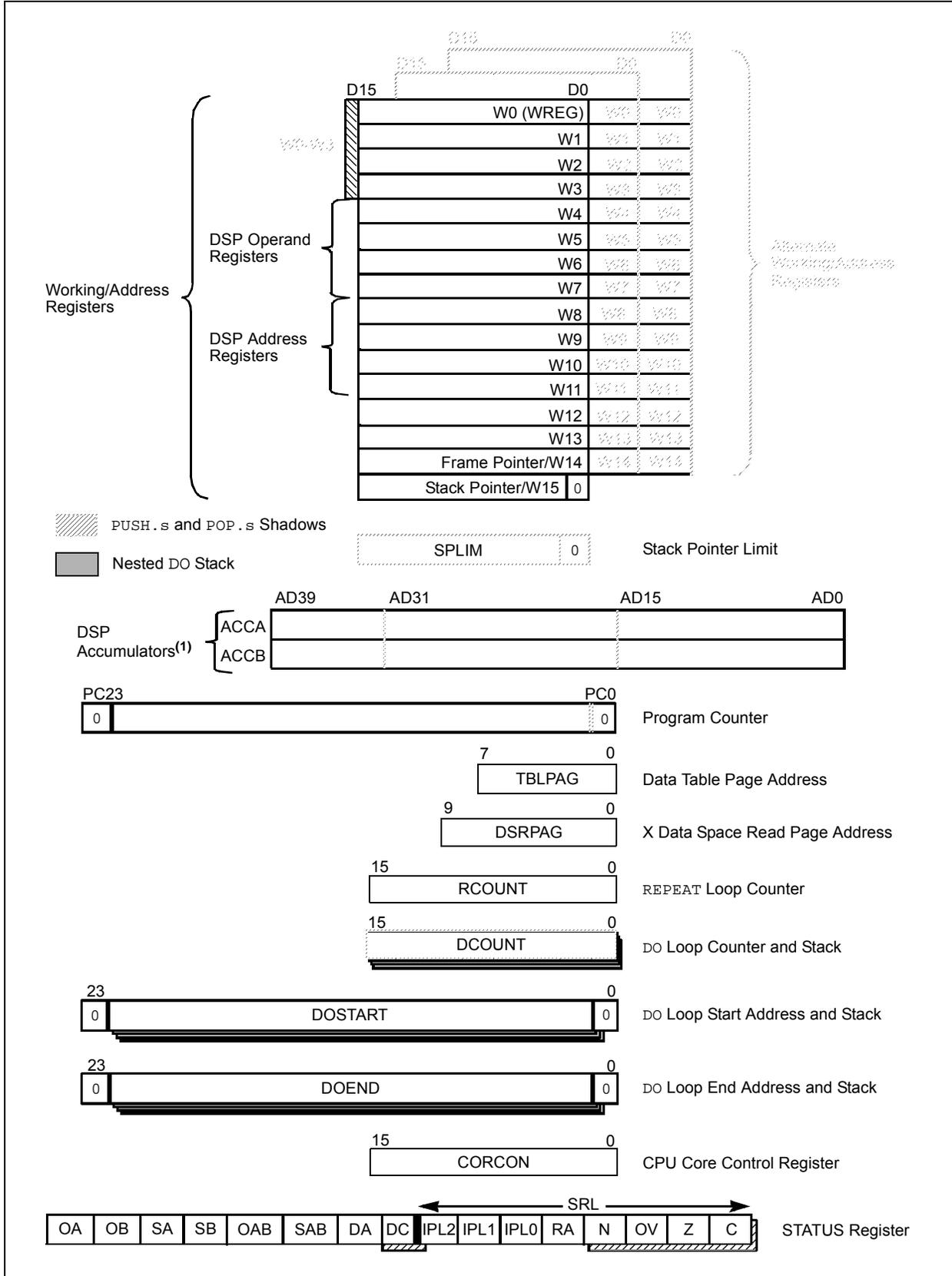
Register(s) Name	Description
W0 through W15 ⁽¹⁾	Working Register Array
W0 through W14 ⁽¹⁾	Alternate 1 Working Register Array
W0 through W14 ⁽¹⁾	Alternate 2 Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
RCOUNT	REPEAT Loop Counter Register
DCOUNT	DO Loop Counter Register
DOSTARTH ⁽²⁾ , DOSTARTL ⁽²⁾	DO Loop Start Address Register (High and Low)
DOENDH, DOENDL	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Note 1: Memory-mapped W0 through W14 represent the value of the register in the currently active CPU context.

2: The DOSTARTH and DOSTARTL registers are read-only.

dsPIC33EPXXGS50X FAMILY

FIGURE 3-2: PROGRAMMER'S MODEL



dsPIC33EPXXGS50X FAMILY

4.5.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible, regardless of the contents of the Data Space Page register. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space in combination with DSRPAG = 0x00. Consequently, DSRPAG is initialized to 0x001 at Reset.

Note 1: DSRPAG should not be used to access Page 0. An EDS access with DSRPAG set to 0x000 will generate an address error trap.

2: Clearing the DSRPAG in software has no effect.

The remaining PSV pages are only accessible using the DSRPAG register in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

4.5.3 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP), and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating the Stack Pointer (for example, creating stack frames).

Note: To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware.

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXGS50X devices and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

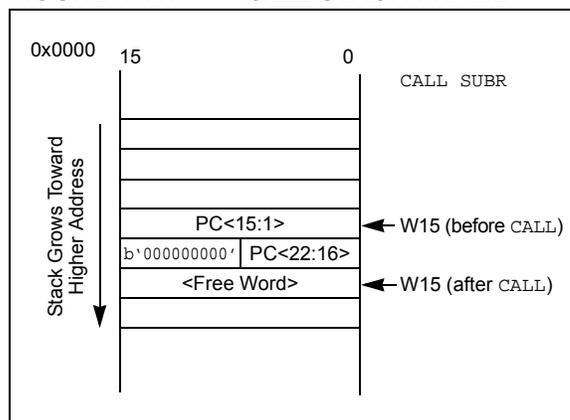
The Software Stack Pointer always points to the first available free word and fills the software stack, working from lower toward higher addresses. Figure 4-11 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-11. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

Note 1: To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore, restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).

2: As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-11: CALL STACK FRAME



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REGISTER 9-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **PWM5MD:** PWM5 Module Disable bit
1 = PWM5 module is disabled
0 = PWM5 module is enabled
- bit 11 **PWM4MD:** PWM4 Module Disable bit
1 = PWM4 module is disabled
0 = PWM4 module is enabled
- bit 10 **PWM3MD:** PWM3 Module Disable bit
1 = PWM3 module is disabled
0 = PWM3 module is enabled
- bit 9 **PWM2MD:** PWM2 Module Disable bit
1 = PWM2 module is disabled
0 = PWM2 module is enabled
- bit 8 **PWM1MD:** PWM1 Module Disable bit
1 = PWM1 module is disabled
0 = PWM1 module is enabled
- bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 10-9: RPINR13: PERIPHERAL PIN SELECT INPUT REGISTER 13

R/W-0							
FLT4R7	FLT4R6	FLT4R5	FLT4R4	FLT4R3	FLT4R2	FLT4R1	FLT4R0
bit 15							bit 8

R/W-0							
FLT3R7	FLT3R6	FLT3R5	FLT3R4	FLT3R3	FLT3R2	FLT3R1	FLT3R0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-8 **FLT4R<7:0>**: Assign PWM Fault 4 (FLT4) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

bit 7-0 **FLT3R<7:0>**: Assign PWM Fault 3 (FLT3) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181

10110100 = Input tied to RP180

•

•

•

00000001 = Input tied to RP1

00000000 = Input tied to Vss

dsPIC33EPXXGS50X FAMILY

REGISTER 10-34: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP61R5	RP61R4	RP61R3	RP61R2	RP61R1	RP61R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP60R5	RP60R4	RP60R3	RP60R2	RP60R1	RP60R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP61R<5:0>:** Peripheral Output Function is Assigned to RP61 Output Pin bits
 (see Table 10-2 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP60R<5:0>:** Peripheral Output Function is Assigned to RP60 Output Pin bits
 (see Table 10-2 for peripheral function numbers)

REGISTER 10-35: RPOR15: PERIPHERAL PIN SELECT OUTPUT REGISTER 15

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP63R5	RP63R4	RP63R3	RP63R2	RP63R1	RP63R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP62R5	RP62R4	RP62R3	RP62R2	RP62R1	RP62R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP63R<5:0>:** Peripheral Output Function is Assigned to RP63 Output Pin bits
 (see Table 10-2 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP62R<5:0>:** Peripheral Output Function is Assigned to RP62 Output Pin bits
 (see Table 10-2 for peripheral function numbers)

dsPIC33EPXXGS50X FAMILY

15.0 HIGH-SPEED PWM

Note: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**High-Speed PWM Module**” (DS70000323) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

The high-speed PWM module on dsPIC33EPXXGS50X devices supports a wide variety of PWM modes and output formats. This PWM module is ideal for power conversion applications, such as:

- AC/DC Converters
- DC/DC Converters
- Power Factor Correction
- Uninterruptible Power Supply (UPS)
- Inverters
- Battery Chargers
- Digital Lighting

15.1 Features Overview

The high-speed PWM module incorporates the following features:

- Five PWMx Generators with Two Outputs per Generator
- Two Master Time Base Modules
- Individual Time Base and Duty Cycle for Each PWM Output
- Duty Cycle, Dead Time, Phase Shift and a Frequency Resolution of 1.04 ns
- Independent Fault and Current-Limit Inputs
- Redundant Output
- True Independent Output
- Center-Aligned PWM mode
- Output Override Control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Dual Trigger from PWMx to Analog-to-Digital Converter (ADC)
- PWMxL and PWMxH Output Pin Swapping
- Independent PWMx Frequency, Duty Cycle and Phase-Shift Changes
- Enhanced Leading-Edge Blanking (LEB) Functionality
- PWM Capture Functionality

Note: Duty cycle, dead time, phase shift and frequency resolution is 8.32 ns in Center-Aligned PWM mode.

Figure 15-1 conceptualizes the PWM module in a simplified block diagram. Figure 15-2 illustrates how the module hardware is partitioned for each PWMx output pair for the Complementary PWM mode.

The PWM module contains five PWM generators. The module has up to 10 PWMx output pins: PWM1H/PWM1L through PWM5H/PWM5L. For complementary outputs, these 10 I/O pins are grouped into high/low pairs.

15.2 Feature Description

The PWM module is designed for applications that require:

- High resolution at high PWM frequencies
- The ability to drive Standard, Edge-Aligned, Center-Aligned Complementary mode and Push-Pull mode outputs
- The ability to create multiphase PWM outputs

Two common, medium power converter topologies are push-pull and half-bridge. These designs require the PWM output signal to be switched between alternate pins, as provided by the Push-Pull PWM mode.

Phase-shifted PWM describes the situation where each PWM generator provides outputs, but the phase relationship between the generator outputs is specifiable and changeable.

Multiphase PWM is often used to improve DC/DC converter load transient response, and reduce the size of output filter capacitors and inductors. Multiple DC/DC converters are often operated in parallel, but phase shifted in time. A single PWM output, operating at 250 kHz, has a period of 4 μ s but an array of four PWM channels, staggered by 1 μ s each, yields an effective switching frequency of 1 MHz. Multiphase PWM applications typically use a fixed-phase relationship.

Variable phase PWM is useful in Zero Voltage Transition (ZVT) power converters. Here, the PWM duty cycle is always 50% and the power flow is controlled by varying the relative phase shift between the two PWM generators.

dsPIC33EPXXGS50X FAMILY

REGISTER 16-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE<2:0>**: Secondary Prescale bits (Master mode)⁽³⁾

111 = Secondary prescale 1:1

110 = Secondary prescale 2:1

•

•

•

000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>**: Primary Prescale bits (Master mode)⁽³⁾

11 = Primary prescale 1:1

10 = Primary prescale 4:1

01 = Primary prescale 16:1

00 = Primary prescale 64:1

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).

2: This bit must be cleared when FRMEN = 1.

3: Do not set both primary and secondary prescalers to the value of 1:1.

dsPIC33EPXXGS50X FAMILY

REGISTER 19-9: ADCON5L: ADC CONTROL REGISTER 5 LOW

R-0, HSC	U-0	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
SHRRDY	—	—	—	C3RDY	C2RDY	C1RDY	C0RDY
bit 15				bit 8			

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SHRPWR	—	—	—	C3PWR	C2PWR	C1PWR	C0PWR
bit 7				bit 0			

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **SHRRDY:** Shared ADC Core Ready Flag bit
1 = ADC core is powered and ready for operation
0 = ADC core is not ready for operation
- bit 14-12 **Unimplemented:** Read as '0'
- bit 11 **C3RDY:** Dedicated ADC Core 3 Ready Flag bit
1 = ADC core is powered and ready for operation
0 = ADC core is not ready for operation
- bit 10 **C2RDY:** Dedicated ADC Core 2 Ready Flag bit
1 = ADC core is powered and ready for operation
0 = ADC core is not ready for operation
- bit 9 **C1RDY:** Dedicated ADC Core 1 Ready Flag bit
1 = ADC core is powered and ready for operation
0 = ADC core is not ready for operation
- bit 8 **C0RDY:** Dedicated ADC Core 0 Ready Flag bit
1 = ADC core is powered and ready for operation
0 = ADC core is not ready for operation
- bit 7 **SHRPWR:** Shared ADC Core x Power Enable bit
1 = ADC Core x is powered
0 = ADC Core x is off
- bit 6-4 **Unimplemented:** Read as '0'
- bit 3 **C3PWR:** Dedicated ADC Core 3 Power Enable bit
1 = ADC core is powered
0 = ADC core is off
- bit 2 **C2PWR:** Dedicated ADC Core 2 Power Enable bit
1 = ADC core is powered
0 = ADC core is off
- bit 1 **C1PWR:** Dedicated ADC Core 1 Power Enable bit
1 = ADC core is powered
0 = ADC core is off
- bit 0 **C0PWR:** Dedicated ADC Core 0 Power Enable bit
1 = ADC core is powered
0 = ADC core is off

dsPIC33EPXXGS50X FAMILY

NOTES:

dsPIC33EPXXGS50X FAMILY

21.1 Module Description

The Programmable Gain Amplifiers are used to amplify small voltages (i.e., voltages across burden/shunt resistors) to improve the signal-to-noise ratio of the measured signal. The PGAx output voltage can be read by any of the four dedicated Sample-and-Hold circuits on the ADC module. The output voltage can also be fed to the comparator module for overcurrent/voltage protection. Figure 21-2 shows a functional block diagram of the PGAx module. Refer to **Section 19.0 “High-Speed, 12-Bit Analog-to-Digital Converter (ADC)”** and **Section 20.0 “High-Speed Analog Comparator”** for more interconnection details.

The gain of the PGAx module is selectable via the GAIN<2:0> bits in the PGAxCON register. There are five selectable gains, ranging from 4x to 64x. The SELPI<2:0> and SELNI<2:0> bits in the PGAxCON register select one of four positive/negative inputs to the PGAx module. For single-ended applications, the SELNI<2:0> bits will select the ground as the negative

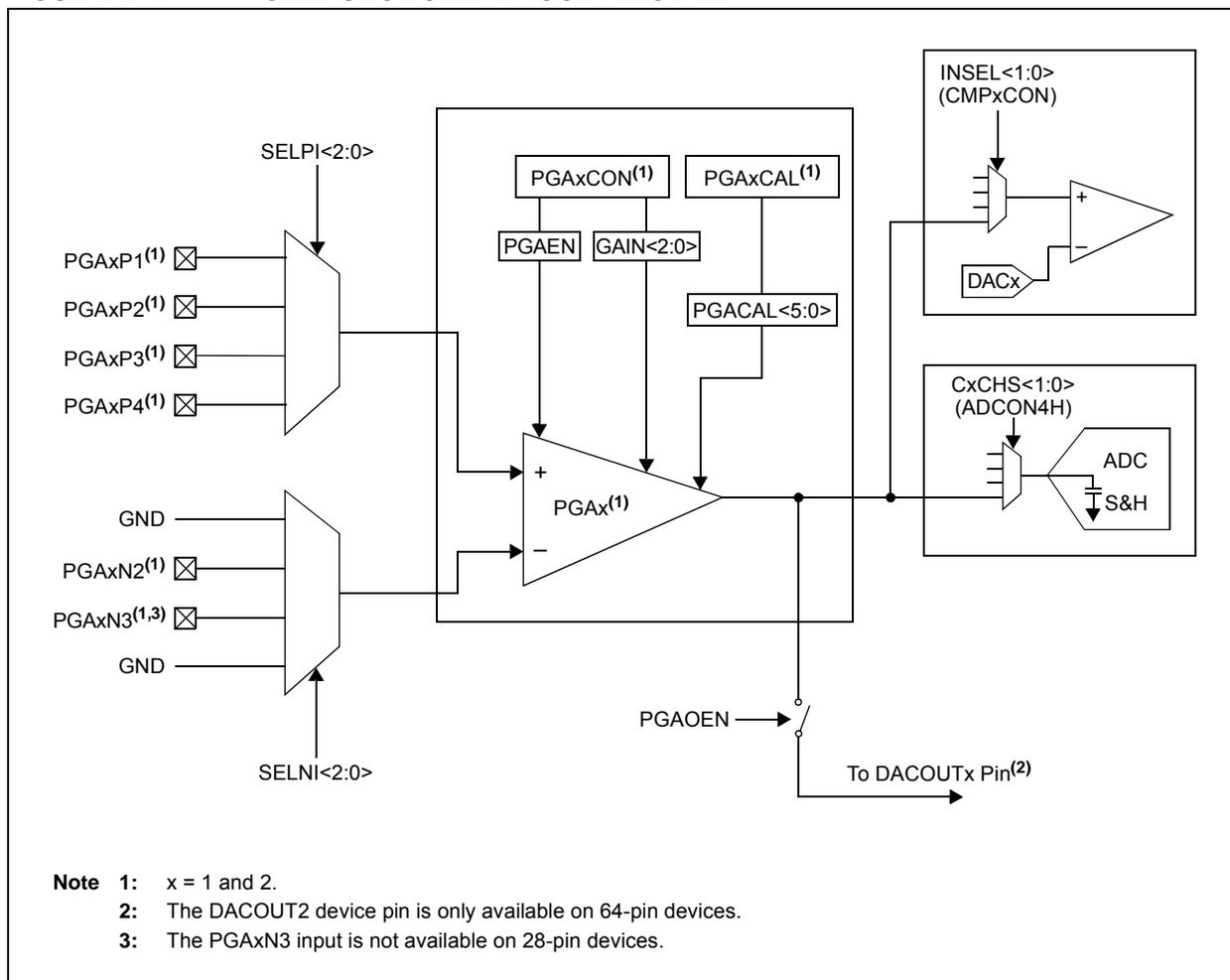
input source. To provide an independent ground reference, PGAxN2 and PGAxN3 pins are available as the negative input source to the PGAx module.

Note 1: Not all PGA positive/negative inputs are available on all devices. Refer to the specific device pinout for available input source pins.

The output voltage of the PGAx module can be connected to the DACOUTx pin by setting the PGOEN bit in the PGAxCON register. When the PGOEN bit is enabled, the output voltage of PGA1 is connected to DACOUT1 and PGA2 is connected to DACOUT2. For devices with a single DACOUTx pin, the output voltage of PGA2 can be connected to DACOUT1 by configuring the DBCC Configuration bit in the FDEVOPT register (FDEVOPT<6>).

If both the DACx output voltage and PGAx output voltage are connected to the DACOUTx pin, the resulting output voltage would be a combination of signals. There is no assigned priority between the PGAx module and the DACx module.

FIGURE 21-2: PGAx FUNCTIONAL BLOCK DIAGRAM



dsPIC33EPXXGS50X FAMILY

22.0 CONSTANT-CURRENT SOURCE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The constant-current source module is a precision current generator and is used in conjunction with the ADC module to measure the resistance of external resistors connected to device pins.

22.1 Features Overview

The constant-current source module offers the following major features:

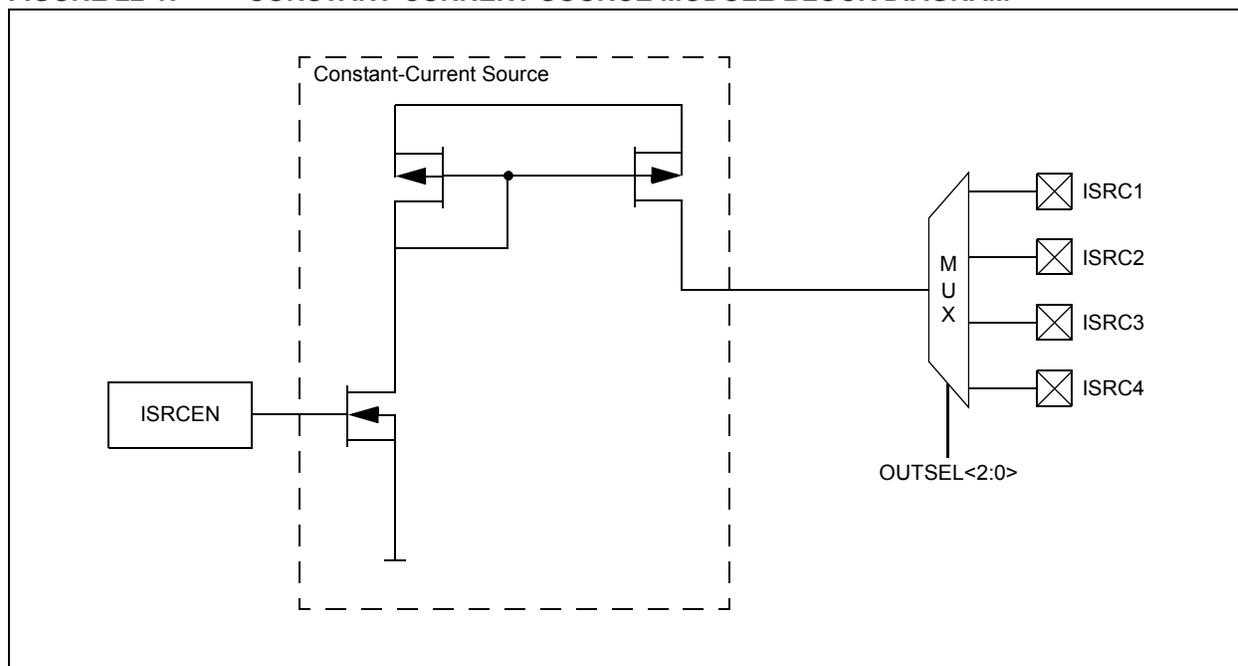
- Constant-Current Generator (10 μ A nominal)
- Internal Selectable Connection to One of Four Pins
- Enable/Disable Bit

22.2 Module Description

Figure 22-1 shows a functional block diagram of the constant-current source module. It consists of a precision current generator with a nominal value of 10 μ A. The module can be enabled and disabled using the ISRCEN bit in the ISRCCON register. The output of the current generator is internally connected to a device pin. The dsPIC33EPXXGS50X family can have up to 4 selectable current source pins. The OUTSEL<2:0> bits in the ISRCCON register allow selection of the target pin.

The current source is calibrated during testing.

FIGURE 22-1: CONSTANT-CURRENT SOURCE MODULE BLOCK DIAGRAM



dsPIC33EPXXGS50X FAMILY

23.6 Watchdog Timer (WDT)

For dsPIC33EPXXGS50X family devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

23.6.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Time-out Period (TWDT), as shown in Parameter SY12 in Table 26-23.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods, ranges from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC_x bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

23.6.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3:2>) needs to be cleared in software after the device wakes up.

23.6.3 ENABLING WDT

The WDT is enabled or disabled by the WDTEN<1:0> Configuration bits in the FWDT Configuration register. When the WDTEN<1:0> Configuration bits have been programmed to '0b11', the WDT is always enabled.

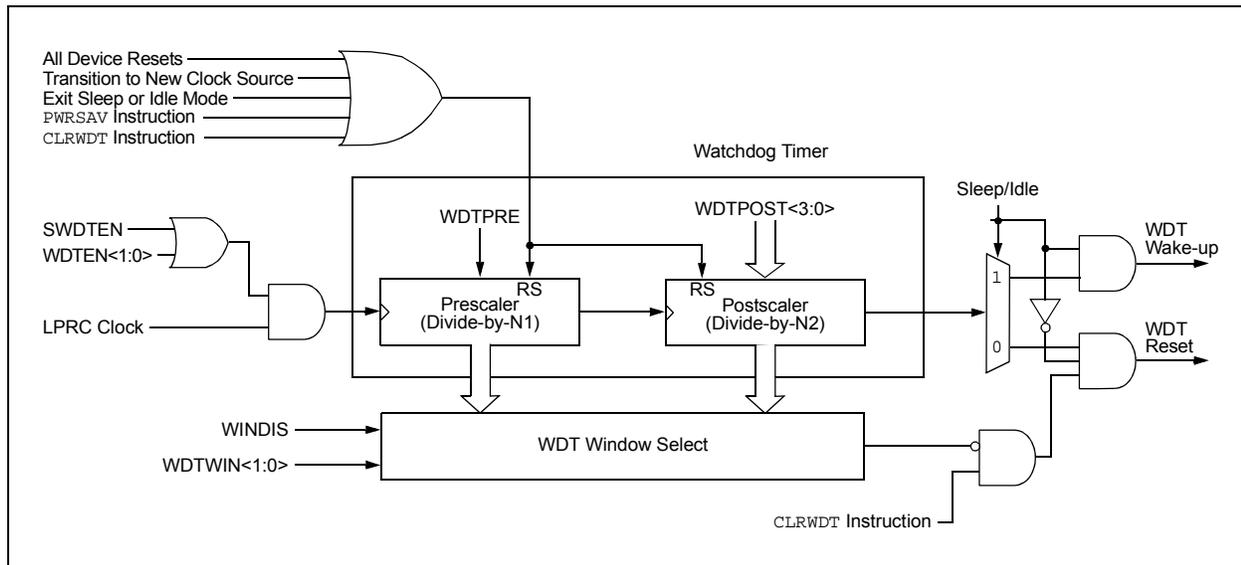
The WDT can be optionally controlled in software when the WDTEN<1:0> Configuration bits have been programmed to '0b10'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disables the WDT during non-critical segments for maximum power savings.

The WDT Time-out flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

23.6.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode, enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<7>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

FIGURE 23-2: WDT BLOCK DIAGRAM



dsPIC33EPXXGS50X FAMILY

FIGURE 26-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS

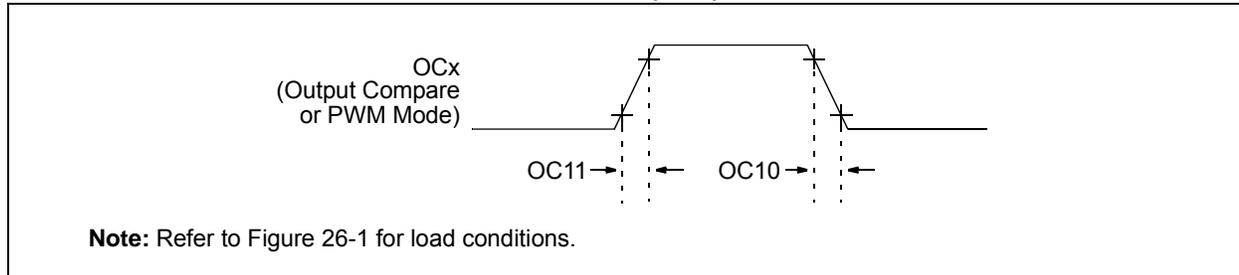


TABLE 26-28: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 26-8: OCx/PWMx MODULE TIMING CHARACTERISTICS

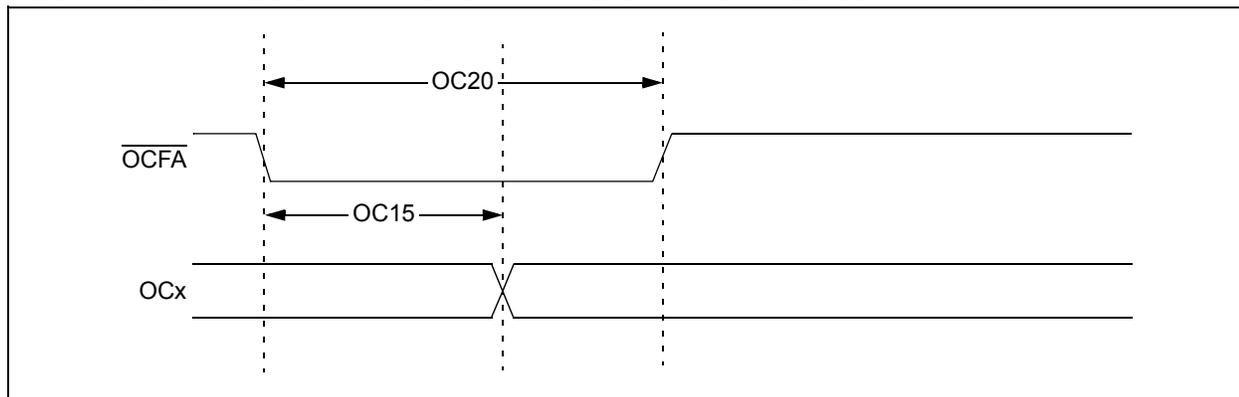


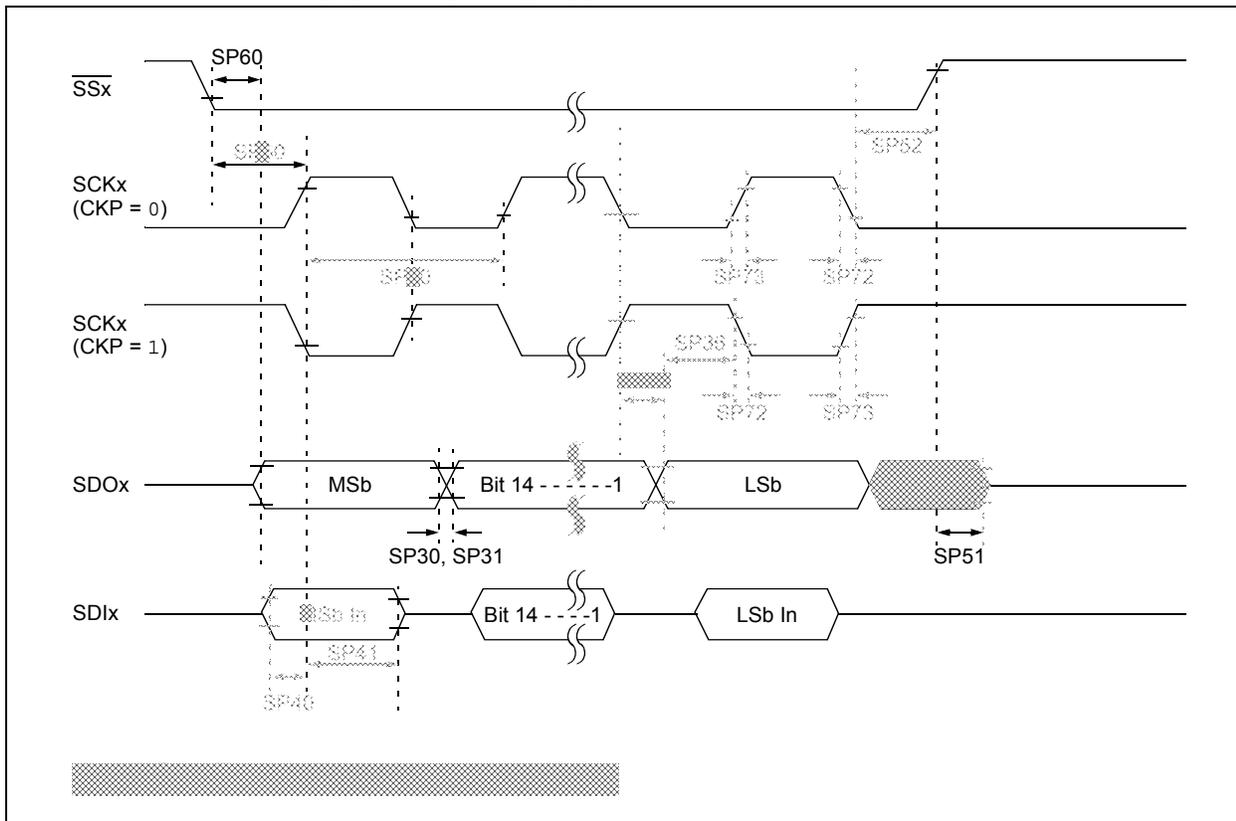
TABLE 26-29: OCx/PWMx MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC15	TFD	Fault Input to PWMx I/O Change	—	—	$T_{CY} + 20$	ns	
OC20	TFLT	Fault Input Pulse Width	$T_{CY} + 20$	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

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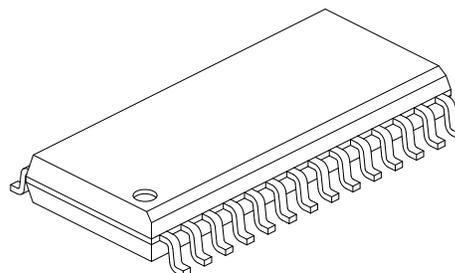
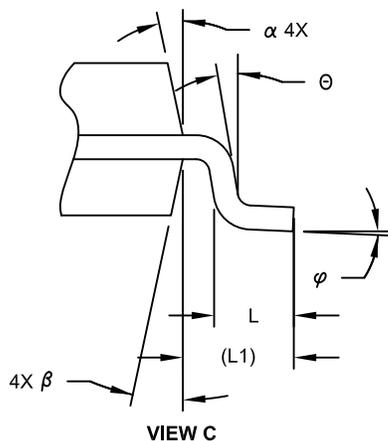
FIGURE 26-15: SPIx SLAVE MODE (FULL-DUPLEX, CKP = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

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NOTES: