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#### Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs504-i-pt

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## Pin Diagrams (Continued)



Legend: Shaded pins are up to 5 VDC tolerant.

RPn represents remappable peripheral functions. See Table 10-1 and Table 10-2 for the complete list of remappable sources.

### REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

hit 7-5	IPI <2.0>. CPI I Interrunt Priority Level Status hits <sup>(1,2)</sup>
DI 7-5	<pre>111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)</pre>
bit 4	RA: REPEAT Loop Active bit
	1 = REPEAT loop is in progress 0 = REPEAT loop is not in progress
bit 3	N: MCU ALU Negative bit
	1 = Result was negative 0 = Result was non-negative (zero or positive)
bit 2	<ul> <li>OV: MCU ALU Overflow bit</li> <li>This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.</li> <li>1 = Overflow occurred for signed arithmetic (in this arithmetic operation)</li> <li>0 = No overflow occurred</li> </ul>
bit 1	Z: MCU ALU Zero bit
	<ul> <li>1 = An operation that affects the Z bit has set it at some time in the past</li> <li>0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)</li> </ul>
bit 0	C: MCU ALU Carry/Borrow bit
	<ul> <li>1 = A carry-out from the Most Significant bit of the result occurred</li> <li>0 = No carry-out from the Most Significant bit of the result occurred</li> </ul>
Note 1:	The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority

- Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
  - 2: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
  - **3:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.



#### FIGURE 4-6: DATA MEMORY MAP FOR dsPIC33EP16GS50X DEVICES

### **REGISTER 7-1:** SR: CPU STATUS REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8
R/W-0 <sup>(3)</sup>	R/W-0 <sup>(3)</sup>	R/W-0 <sup>(3)</sup>	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2 <sup>(2)</sup>	IPL1 <sup>(2)</sup>	IPL0 <sup>(2)</sup>	RA	N	OV	Z	С
bit 7		•					bit 0
l egend.		C = Clearable	hit				

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 IPL<2:0>: CPU Interrupt Priority Level Status bits<sup>(2,3)</sup> 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10)

- 001 = CPU Interrupt Priority Level is 1 (9)
- 000 = CPU Interrupt Priority Level is 0 (8)

**Note 1:** For complete register details, see Register 3-1.

- 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

NOTES:

### 10.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 10-1 through Register 10-19). Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 8-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 10-2 illustrates remappable pin selection for the U1RX input.

#### FIGURE 10-2: REMAPPABLE INPUT FOR U1RX



### 10.4.4.1 Virtual Connections

The dsPIC33EPXXGS50X devices support six virtual RPn pins (RP176-RP181), which are identical in functionality to all other RPn pins, with the exception of pinouts. These six pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP176 and the PWM Fault input can be configured for RP176 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCI1R7	SYNCI1R6	SYNCI1R5	SYNCI1R4	SYNCI1R3	SYNCI1R2	SYNCI1R1	SYNCI1R0
bit 15					•	•	bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—			_	—	—	—
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-8	SYNCI1R<7:	<b>0&gt;:</b> Assign PW	M Synchroniz	ation Input 1 to	the Correspon	ding RPn Pin b	oits
	10110101 =	Input tied to RI	P181				
	10110100 =	Input tied to RF	P180				
	•						
	•						
	•						
	0000001=	Input tied to RI	P1				
	00000000 =	Input tied to Vs	SS				
bit 7-0	Unimplemen	ted: Read as '	0'				

### REGISTER 10-16: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37

### REGISTER 10-20: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	RP33R5	RP33R4	RP33R3	RP33R2	RP33R1	RP33R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP32R5	RP32R4	RP32R3	RP32R2	RP32R1	RP32R0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-14	Unimplemen	ted: Read as '	0'				
bit 13-8	<b>RP33R&lt;5:0&gt;</b> (see Table 10	Peripheral Ou -2 for periphera	Itput Function al function nur	is Assigned to nbers)	RP33 Output F	Pin bits	
bit 7-6	Unimplemen	ted: Read as '	0'				

bit 5-0 **RP32R<5:0>:** Peripheral Output Function is Assigned to RP32 Output Pin bits (see Table 10-2 for peripheral function numbers)

#### REGISTER 10-21: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—		RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	
bit 15							bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	RP34R5	RP34R4	RP34R3	RP34R2	RP34R1	RP34R0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'		
-n = Value at P	-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown							
bit 15-14	Unimplemen	ted: Read as '	0'					
bit 13-8	RP35R<5:0>:	Peripheral Ou	tput Function	is Assianed to	RP35 Output P	in bits		

(see Table 10-2 for peripheral function numbers)

- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 **RP34R<5:0>:** Peripheral Output Function is Assigned to RP34 Output Pin bits (see Table 10-2 for peripheral function numbers)

#### REGISTER 10-24: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0
bit 7						•	bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-14	Unimplemen	ted: Read as '	0'				
bit 13-8	<b>RP41R&lt;5:0&gt;</b> (see Table 10	Peripheral Ou -2 for periphera	Itput Function al function nur	is Assigned to nbers)	RP41 Output F	Pin bits	

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 10-2 for peripheral function numbers)

#### REGISTER 10-25: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at POR (1' = Bit is set (0' = Bit is cleared x = Bit is unknown						nown	
bit 15-14	Unimplemen	ted: Read as '	n'				

bit 13-8 **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 10-2 for peripheral function numbers)

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 10-2 for peripheral function numbers)

## 11.0 TIMER1

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be Operated in Asynchronous Counter mode from an External Clock Source
- The External Clock Input (T1CK) can Optionally be Synchronized to the Internal Device Clock and the Clock Synchronization is Performed after the Prescaler
- A block diagram of Timer1 is shown in Figure 11-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- · Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FcY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit settings for different operating modes are provided in Table 11-1.

Mode	TCS	TGATE	TSYNC
Timer	0	0	х
Gated Timer	0	1	х
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

## TABLE 11-1: TIMER MODE SETTINGS





#### R/W-0 R/W-0 U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 **HRPDIS HRDDIS** \_\_\_ BLANKSEL3 BLANKSEL2 BLANKSEL1 **BLANKSEL0** \_ bit 15 bit 8 R/W-0 U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 CHOPSEL3 CHOPSEL2 CHOPSEL1 CHOPSEL0 CHOPHEN CHOPLEN bit 7 bit 0 Leaend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 HRPDIS: High-Resolution PWMx Period Disable bit 1 = High-resolution PWMx period is disabled to reduce power consumption 0 = High-resolution PWMx period is enabled bit 14 HRDDIS: High-Resolution PWMx Duty Cycle Disable bit 1 = High-resolution PWMx duty cycle is disabled to reduce power consumption 0 = High-resolution PWMx duty cycle is enabled bit 13-12 Unimplemented: Read as '0' bit 11-8 BLANKSEL<3:0>: PWMx State Blank Source Select bits The selected state blank signal will block the current-limit and/or Fault input signals (if enabled via the BCH and BCL bits in the LEBCONx register). 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0101 = PWM5H is selected as the state blank source 0100 = PWM4H is selected as the state blank source 0011 = PWM3H is selected as the state blank source 0010 = PWM2H is selected as the state blank source 0001 = PWM1H is selected as the state blank source 0000 = No state blanking bit 7-6 Unimplemented: Read as '0' bit 5-2 CHOPSEL<3:0>: PWMx Chop Clock Source Select bits The selected signal will enable and disable (chop) the selected PWMx outputs. 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0101 = PWM5H is selected as the chop clock source 0100 = PWM4H is selected as the chop clock source 0011 = PWM3H is selected as the chop clock source 0010 = PWM2H is selected as the chop clock source 0001 = PWM1H is selected as the chop clock source 0000 = Chop clock generator is selected as the chop clock source bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit 1 = PWMxH chopping function is enabled 0 = PWMxH chopping function is disabled bit 0 CHOPLEN: PWMxL Output Chopping Enable bit 1 = PWMxL chopping function is enabled 0 = PWMxL chopping function is disabled

**REGISTER 15-26:** AUXCONx: PWMx AUXILIARY CONTROL REGISTER (x = 1 to 5)

## 19.0 HIGH-SPEED, 12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "12-Bit High-Speed, Multiple SARs A/D Converter (ADC)" (DS70005213) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

dsPIC33EPXXGS50X devices have a high-speed, 12-bit Analog-to-Digital Converter (ADC) that features a low conversion latency, high resolution and oversampling capabilities to improve performance in AC/DC, DC/DC power converters.

## **19.1 Features Overview**

The High Speed, 12-Bit Multiple SARs Analog-to-Digital Converter (ADC) includes the following features:

- Five ADC Cores: Four Dedicated Cores and One Shared (Common) Core
- User-Configurable Resolution of up to 12 Bits for each Core
- Up to 3.25 Msps Conversion Rate per Channel at 12-Bit Resolution
- Low-Latency Conversion
- Up to 22 Analog Input Channels, with a Separate 16-Bit Conversion Result Register for each Input
- Conversion Result can be Formatted as Unsigned or Signed Data, on a per Channel Basis, for All Channels
- Single-Ended and Pseudodifferential Conversions are available on All ADC Cores

- Simultaneous Sampling of up to 5 Analog Inputs
- Channel Scan Capability
- Multiple Conversion Trigger Options for each Core, including:
  - PWM1 through PWM5 (primary and secondary triggers, and current-limit event trigger)
  - PWM Special Event Trigger
  - Timer1/Timer2 period match
  - Output Compare 1 and event trigger
  - External pin trigger event (ADTRG31)
  - Software trigger
- Two Integrated Digital Comparators with Dedicated Interrupts:
  - Multiple comparison options
  - Assignable to specific analog inputs
- Two Oversampling Filters with Dedicated Interrupts:
  - Provide increased resolution
  - Assignable to a specific analog input

The module consists of five independent SAR ADC cores. Simplified block diagrams of the Multiple SARs 12-Bit ADC are shown in Figure 19-1, Figure 19-2 and Figure 19-3.

The analog inputs (channels) are connected through multiplexers and switches to the Sample-and-Hold (S&H) circuit of each ADC core. The core uses the channel information (the output format, the measurement mode and the input number) to process the analog sample. When conversion is complete, the result is stored in the result buffer for the specific analog input, and passed to the digital filter and digital comparator if they were configured to use data from this particular channel.

The ADC module can sample up to five inputs at a time (four inputs from the dedicated SAR cores and one from the shared SAR core). If multiple ADC inputs request conversion on the shared core, the module will convert them in a sequential manner, starting with the lowest order input.

The ADC provides each analog input the ability to specify its own trigger source. This capability allows the ADC to sample and convert analog inputs that are associated with PWM generators operating on independent time bases.

### **REGISTER 19-11:** ADCOREXL: DEDICATED ADC CORE x CONTROL REGISTER LOW (x = 0 to 3)

r							
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	_	—	_	—	—	SAMO	C<9:8>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SAM	C<7:0>			
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable I	oit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown					nown		

bit 15-10 Unimplemented: Read as '0'

## 20.0 HIGH-SPEED ANALOG COMPARATOR

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed Analog Comparator Module" (DS70005128) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The high-speed analog comparator module monitors current and/or voltage transients that may be too fast for the CPU and ADC to capture.

### 20.1 Features Overview

The SMPS comparator module offers the following major features:

- Four Rail-to-Rail Analog Comparators
- Dedicated 12-Bit DAC for each Analog Comparator
- Up to Six Selectable Input Sources per Comparator:
  - Four external inputs
  - Two internal inputs from the PGAx module
- Programmable Comparator Hysteresis
- Programmable Output Polarity
- Up to Two DAC Outputs to Device Pins
- Multiple Voltage References for the DAC:
   External References (EXTREF1 or
  - EXTREF2) - AVDD
- Interrupt Generation Capability
- Functional Support for PWMx:
  - PWMx duty cycle control
  - PWMx period control
  - PWMx Fault detected

### REGISTER 21-1: PGAxCON: PGAx CONTROL REGISTER (CONTINUED)

- bit 2-0 GAIN<2:0>: PGAx Gain Selection bits
  - 111 = Reserved
  - 110 = Gain of 64x
  - 101 = Gain of 32x
  - 100 = Gain of 16x
  - 011 = Gain of 8x
  - 010 = Gain of 4x
  - 001 = Reserved
  - 000 = Reserved

### REGISTER 21-2: PGAxCAL: PGAx CALIBRATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			PGAC	CAL<5:0>		
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unk	nown

bit 15-6 Unimplemented: Read as '0'

bit 5-0 **PGACAL<5:0>:** PGAx Offset Calibration bits

The calibration values for PGA1 and PGA2 must be copied from Flash addresses, 0x800E48 and 0x800E4C, respectively, into these bits before the module is enabled. Refer to the calibration data address table (Table 23-3) in **Section 23.0 "Special Features**" for more information.

### REGISTER 23-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
			DEVID<	<23:16>			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVID	<15:8>			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVID	)<7:0>			
bit 7							bit 0
Legend:	R = Read-Only bit			U = Unimplen	nented bit		

bit 23-0 DEVID<23:0>: Device Identifier bits

#### REGISTER 23-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R
			DEVREV	/<23:16>			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVRE	/<15:8>			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVRE	V<7:0>			
bit 7							bit 0
Legend:	R = Read-only bit			U = Unimpler	nented bit		

bit 23-0 DEVREV<23:0>: Device Revision bits

## 24.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EP instruction set is almost identical to that of the dsPIC30F and dsPIC33F.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- · Bit-oriented operations
- · Literal operations
- DSP operations
- Control operations

Table 24-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 24-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register 'Wb' without any address modifier
- The second source operand, which is typically a register 'Ws' with or without an address modifier
- The destination of the result, which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- · The file register specified by the value 'f'
- The destination, which could be either the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/ shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register 'Wb' without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- · The accumulator write back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the table read and table write instructions

## TABLE 24-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier Working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier Working register pair for DSP instructions $\in$ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 Working registers ∈ {W0W15}
Wnd	One of 16 Destination Working registers ∈ {W0W15}
Wns	One of 16 Source Working registers ∈ {W0W15}
WREG	W0 (Working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}

#### TABLE 26-43: ADC MODULE SPECIFICATIONS

АС СНА	ARACTERIS	STICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.}\\ \mbox{(unless otherwise stated)}^{(5)}\\ \mbox{Operating temperature} & -40^{\circ}C \leq TA\\ & -40^{\circ}C \leq TA \end{array}$			ions: 3.0V to 3.6V $^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $^{\circ}C \le TA \le +125^{\circ}C$ for Extended	
Param No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
	-		Device	Supply	-		
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 3.0		Lesser of: VDD + 0.3 or 3.6	V	The difference between AVDD supply and VDD supply must not exceed ±300 mV at all times, including during device power-up
AD02	AVss	Module Vss Supply	Vss	—	Vss + 0.3	V	
		<b>-</b>	Referenc	e Inputs			
AD06	VREFL	Reference Voltage Low	_	AVss	—	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.7		AVDD	V	(Note 3)
AD08	IREF	Reference Input Current	—	5	10	μA	ADC operating or in standby
	1	1	Analog	g Input	1		
AD12	VINH-VINL	Full-Scale Input Span	AVss		AVdd	V	
AD14	VIN	Absolute Input Voltage	AVss – 0.3		AVDD + 0.3	V	
AD17	Rin	Recommended Impedance of Analog Voltage Source	_	100	—	Ω	For minimum sampling time <b>(Note 1)</b>
AD66	Vbg	Internal Voltage Reference Source	—	1.2	_	V	
		ADC Ac	curacy: Pseu	do-Differe	ential Input		
AD20a	Nr	Resolution		12		bits	
AD21a	INL	Integral Nonlinearity	> -3		< 3	LSb	AVss = 0V, AVDD = 3.3V
AD22a	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	AVss = 0V, AVDD = 3.3V (Note 2)
AD23a	Gerr	Gain Error (Dedicated Core)	> 5	13	< 20	LSb	AVss = 0V, AVdd = 3.3V
		Gain Error (Shared Core)	> -1	5	< 10	LSb	
AD24a	EOFF	Offset Error (Dedicated Core)	> 2	7	< 12	LSb	AVss = 0V, AVdd = 3.3V
		Offset Error (Shared Core)	> -2	3	< 8	LSb	
AD25a		Monotonicity					Guaranteed

Note 1: These parameters are not characterized or tested in manufacturing.

2: No missing codes, limits based on characterization results.

3: These parameters are characterized but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

**5:** The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

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