Microchip Technology - DSPIC33EP64GS505-E/PT Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 19x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP Exposed Pad
Supplier Device Package	48-TQFP-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs505-e-pt

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXGS50X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXGS50X family requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins
  regardless if ADC module is not used (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP
  (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins
  used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins
  when external oscillator source is used (see **Section 2.6 "External Oscillator Pins"**)

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG
0 = Stack frame is not active; W14 and W15 address the base Data Space

bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is always read as '0'.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	CCTXI2	CCTXI1	CCTXI0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	MCTXI2	MCTXI1	MCTXI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

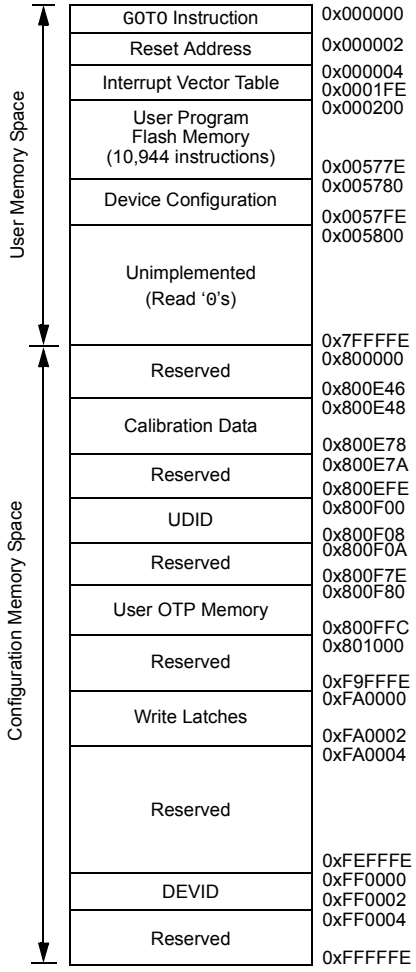
bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **CCTXI<2:0>:** Current (W Register) Context Identifier bits
111 = Reserved
•
•
•
011 = Reserved
010 = Alternate Working Register Set 2 is currently in use
001 = Alternate Working Register Set 1 is currently in use
000 = Default register set is currently in use

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **MCTXI<2:0>:** Manual (W Register) Context Identifier bits
111 = Reserved
•
•
•
011 = Reserved
010 = Alternate Working Register Set 2 was most recently manually selected
001 = Alternate Working Register Set 1 was most recently manually selected
000 = Default register set was most recently manually selected

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP32GS50X DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-2: CPU CORE REGISTER MAP (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DOENDL	003E	D0 Loop End Address Register Low (DOENDL<15:1>)															—	0000
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	D0 Loop End Address Register High (DOENDH<5:0>)						0000
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000
CORCON	0044	VAR	—	US1	US0	EDT	DL2	DL1	DL0	SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020
MODCON	0046	XMODEN	YMODEN	—	—	BWM3	BWM2	BWM1	BWM0	YWM3	YWM2	YWM1	YWM0	XWM3	XWM2	XWM1	XWM0	0000
XMODSRT	0048	X Mode Start Address Register (XMODSRT<15:1>)															—	0000
XMODEND	004A	X Mode End Address Register (XMODEND<15:1>)															—	0001
YMODSRT	004C	Y Mode Start Address Register (YMODSRT<15:1>)															—	0000
YMODEND	004E	Y Mode End Address Register (YMODEND<15:1>)															—	0001
XBREV	0050	BREN	XBREV<14:0>															0000
DISICNT	0052	—	—	DISICNT<13:0>														0000
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG<7:0>								0000
CTXTSTAT	005A	—	—	—	—	—	CCTXI2	CCTXI1	CCTXI0	—	—	—	—	—	MCTXI2	MCTXI1	MCTXI0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The contents of this register should never be modified. The DSWPAG must always point to the first page.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	NVMIF	—	ADCIF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	—	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	—	—	—	—	INT1IF	CNIF	AC1IF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	—	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	PSEMIF	—	—	INT4IF	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	—	—	—	—	PSESIF	—	—	—	—	—	—	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—		—	—	—	—	—	—	—	0000
IFS6	080C	ADCAN1IF	ADCAN0IF	—	—	—	—	AC4IF	AC3IF	AC2IF	—	—	—	—	PWM5IF	PWM4IF	PWM3IF	0000
IFS7	080E	—	—	—	—	—	—	—	—	—	—	ADCAN7IF	ADCAN6IF	ADCAN5IF	ADCAN4IF	ADCAN3IF	ADCAN2IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	ADCAN16IF(1)	ADCAN15IF(1)	ADCAN14IF(2)	ADCAN13IF(1)	ADCAN12IF(2)	ADCAN11IF(2)	ADCAN10IF(2)	ADCAN9IF(2)	ADCAN8IF(2)	—	—	—	—	—	—	—	0000
IFS10	0814	—	I2C2BCIF	I2C1BCIF	—	—	—	—	—	—	—	—	ADCAN21IF	ADCAN20IF	ADCAN19IF	ADCAN18IF	ADCAN17IF(2)	0000
IFS11	0816	—	—	—	—	—	—	—	—	—	—	—	ADFLTR1IF	ADFLTR0IF	ADCMP1IF	ADCMP0IF	—	0000
IEC0	0820	NVMIE	—	ADCIE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	—	—	—	—	INT1IE	CNIE	AC1IF	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	—	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	PSEMIE	—	—	INT4IE	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	—	—	—	—	PSESIE	—	—	—	—	—	—	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	ADCAN1IE	ADCAN0IE	—	—	—	—	AC4IE	AC3IE	AC2IE	—	—	—	—	PWM5IE	PWM4IE	PWM3IE	0000
IEC7	082E	—	—	—	—	—	—	—	—	—	—	ADCAN7IE	ADCAN6IE	ADCAN5IE	ADCAN4IE	ADCAN3IE	ADCAN2IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	ADCAN16IE(1)	ADCAN15IE(1)	ADCAN14IE(2)	ADCAN13IE(1)	ADCAN12IE(2)	ADCAN11IE(2)	ADCAN10IE(2)	ADCAN9IE(2)	ADCAN8IE(2)	—	—	—	—	—	—	—	0000
IEC10	0834	—	I2C2BCIE	I2C1BCIE	—	—	—	—	—	—	—	—	ADCAN21IE	ADCAN20IE	ADCAN19IE	ADCAN18IE	ADCAN17IE(2)	0000
IEC11	0836	—	—	—	—	—	—	—	—	—	—	—	ADFLTR1IE	ADFLTR0IE	ADCMP1IE	ADCMP0IE	—	0000
IPC0	0840	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	0842	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	—	—	—	4440
IPC2	0844	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	0846	—	NVMIP2	NVMIP1	NVMIP0	—	—	—	—	—	ADCIP2	ADCIP1	ADCIP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4044
IPC4	0848	—	CNIP2	CNIP1	CNIP0	—	AC1IP2	AC1IP1	AC1IP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP2	INT1IP1	INT1IP0	0004
IPC6	084C	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	—	—	—	4440
IPC7	084E	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP2	SPI2IP1	SPI2IP0	—	SPI2EIP2	SPI2EIP1	SPI2EIP0	0044
IPC9	0852	—	—	—	—	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	—	—	—	0440

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Only available on dsPIC33EPXXGS506 devices.

2: Only available on dsPIC33EPXXGS504/505 and dsPIC33EPXXGS506 devices.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER(1) (CONTINUED)

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit(3)
1 = FSCM has detected a clock failure
0 = FSCM has not detected a clock failure

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Requests oscillator switch to the selection specified by the NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence.

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and will trigger an oscillator failure trap.

REGISTER 10-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1CTSR7	U1CTSR6	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1RXR7	U1RXR6	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **U1CTSR<7:0>:** Assign UART1 Clear-to-Send ($\overline{U1CTS}$) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

bit 7-0 **U1RXR<7:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

REGISTER 10-14: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK2INR7	SCK2INR6	SCK2INR5	SCK2INR4	SCK2INR3	SCK2INR2	SCK2INR1	SCK2INR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI2R7	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **SCK2INR<7:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

bit 7-0 **SDI2R<7:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

REGISTER 10-19: RPINR43: PERIPHERAL PIN SELECT INPUT REGISTER 43

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT8R7	FLT8R6	FLT8R5	FLT8R4	FLT8R3	FLT8R2	FLT8R1	FLT8R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT7R7	FLT7R6	FLT7R5	FLT7R4	FLT7R3	FLT7R2	FLT7R1	FLT7R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **FLT8R<7:0>:** Assign PWM Fault 8 (FLT8) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

bit 7-0 **FLT7R<7:0>:** Assign PWM Fault 7 (FLT7) to the Corresponding RPn Pin bits

10110101 = Input tied to RP181
10110100 = Input tied to RP180
•
•
•
00000001 = Input tied to RP1
00000000 = Input tied to Vss

NOTES:

13.2 Input Capture Registers

REGISTER 13-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R-0, HC, HS	R-0, HC, HS	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture x Stop in Idle Control bit
1 = Input capture will halt in CPU Idle mode
0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture x Timer Select bits
111 = Peripheral clock (FP) is the clock source of the ICx
110 = Reserved
101 = Reserved
100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)
011 = T5CLK is the clock source of the ICx
010 = T4CLK is the clock source of the ICx
001 = T2CLK is the clock source of the ICx
000 = T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
1 = Input capture buffer overflow has occurred
0 = No input capture buffer overflow has occurred

bit 3 **ICBNE:** Input Capture x Buffer Not Empty Status bit (read-only)
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture x Mode Select bits
111 = Input Capture x functions as an interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
110 = Unused (module is disabled)
101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
011 = Capture mode, every rising edge (Simple Capture mode)
010 = Capture mode, every falling edge (Simple Capture mode)
001 = Capture mode, every rising and falling edge (Edge Detect mode, ICI<1:0>, is not used in this mode)
000 = Input Capture x is turned off

REGISTER 15-20: IOCONx: PWMx I/O CONTROL REGISTER (x = 1 to 5) (CONTINUED)

bit 3-2 **CLDAT<1:0>:** State for PWMxH and PWMxL Pins if CLMOD is Enabled bits(2)
IFLTMOD (FCLCONx<15>) = 0: Normal Fault Mode:
If current limit is active, then CLDAT1 provides the state for the PWMxH pin.
If current limit is active, then CLDAT0 provides the state for the PWMxL pin.
IFLTMOD (FCLCONx<15>) = 1: Independent Fault Mode:
CLDAT<1:0> bits are ignored.

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to the PWMxL pins; PWMxL output signal is connected to the PWMxH pins
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0 **OSYNC:** Output Override Synchronization bit
1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx time base
0 = Output overrides via the OVRDAT<1:0> bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: State represents the active/inactive state of the PWMx depending on the POLH and POLL bits settings.

REGISTER 15-21: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER (x = 1 to 5)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<12:5>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
TRGCMP<4:0>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **TRGCMP<12:0>:** Trigger Compare Value bits
When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

bit 2-0 **Unimplemented:** Read as '0'

REGISTER 17-1: I2CxCONL: I2Cx CONTROL REGISTER LOW (CONTINUED)

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; hardware is clear at the end of the master Acknowledge sequence
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C; hardware is clear at the end of the eighth bit of the master receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on SDAx and SCLx pins; hardware is clear at the end of the master Stop sequence
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Repeated Start sequence
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Start sequence
0 = Start condition is not in progress

REGISTER 17-3: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	R-0, HSC	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	'0' = Bit is cleared	x = Bit is unknown
-n = Value at POR	'1' = Bit is set	U = Unimplemented bit, read as '0'	

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I^2C master, applicable to master transmit operation)
1 = NACK was received from slave
0 = ACK was received from slave
Hardware is set or clear at the end of a slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^2C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (I^2C Slave mode only)
1 = I^2C bus is an Acknowledge sequence, set on the 8th falling edge of SCLx
0 = Not an Acknowledge sequence, cleared on the 9th rising edge of SCLx

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No bus collision detected
Hardware is set at detection of a bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when address matches the general call address. Hardware is clear at Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.

bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^2C module is busy
0 = No collision
Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register was still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (I^2C Slave mode only)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

REGISTER 18-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1: Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

REGISTER 19-7: ADCON4L: ADC CONTROL REGISTER 4 LOW

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SYNCTRG3	SYNCTRG2	SYNCTRG1	SYNCTRG0
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SAMC3EN	SAMC2EN	SAMC1EN	SAMC0EN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11 **SYNCTRG3:** Dedicated ADC Core 3 Trigger Synchronization bit
1 = All triggers are synchronized with the core source clock (TCORESRC)
0 = The ADC core triggers are not synchronized

bit 10 **SYNCTRG2:** Dedicated ADC Core 2 Trigger Synchronization bit
1 = All triggers are synchronized with the core source clock (TCORESRC)
0 = The ADC core triggers are not synchronized

bit 9 **SYNCTRG1:** Dedicated ADC Core 1 Trigger Synchronization bit
1 = All triggers are synchronized with the core source clock (TCORESRC)
0 = The ADC core triggers are not synchronized

bit 8 **SYNCTRG0:** Dedicated ADC Core 0 Trigger Synchronization bit
1 = All triggers are synchronized with the core source clock (TCORESRC)
0 = The ADC core triggers are not synchronized

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3 **SAMC3EN:** Dedicated ADC Core 3 Conversion Delay Enable bit
1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCORE3L register
0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle

bit 2 **SAMC2EN:** Dedicated ADC Core 2 Conversion Delay Enable bit
1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCORE2L register
0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle

bit 1 **SAMC1EN:** Dedicated ADC Core 1 Conversion Delay Enable bit
1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCORE1L register
0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle

bit 0 **SAMC0EN:** Dedicated ADC Core 0 Conversion Delay Enable bit
1 = After trigger, the conversion will be delayed and the ADC core will continue sampling during the time specified by the SAMC<9:0> bits in the ADCORE0L register
0 = After trigger, the sampling will be stopped immediately and the conversion will be started on the next core clock cycle

21.1 Module Description

The Programmable Gain Amplifiers are used to amplify small voltages (i.e., voltages across burden/shunt resistors) to improve the signal-to-noise ratio of the measured signal. The PGAx output voltage can be read by any of the four dedicated Sample-and-Hold circuits on the ADC module. The output voltage can also be fed to the comparator module for overcurrent/ voltage protection. Figure 21-2 shows a functional block diagram of the PGAx module. Refer to **Section 19.0 "High-Speed, 12-Bit Analog-to-Digital Converter (ADC)"** and **Section 20.0 "High-Speed Analog Comparator"** for more interconnection details.

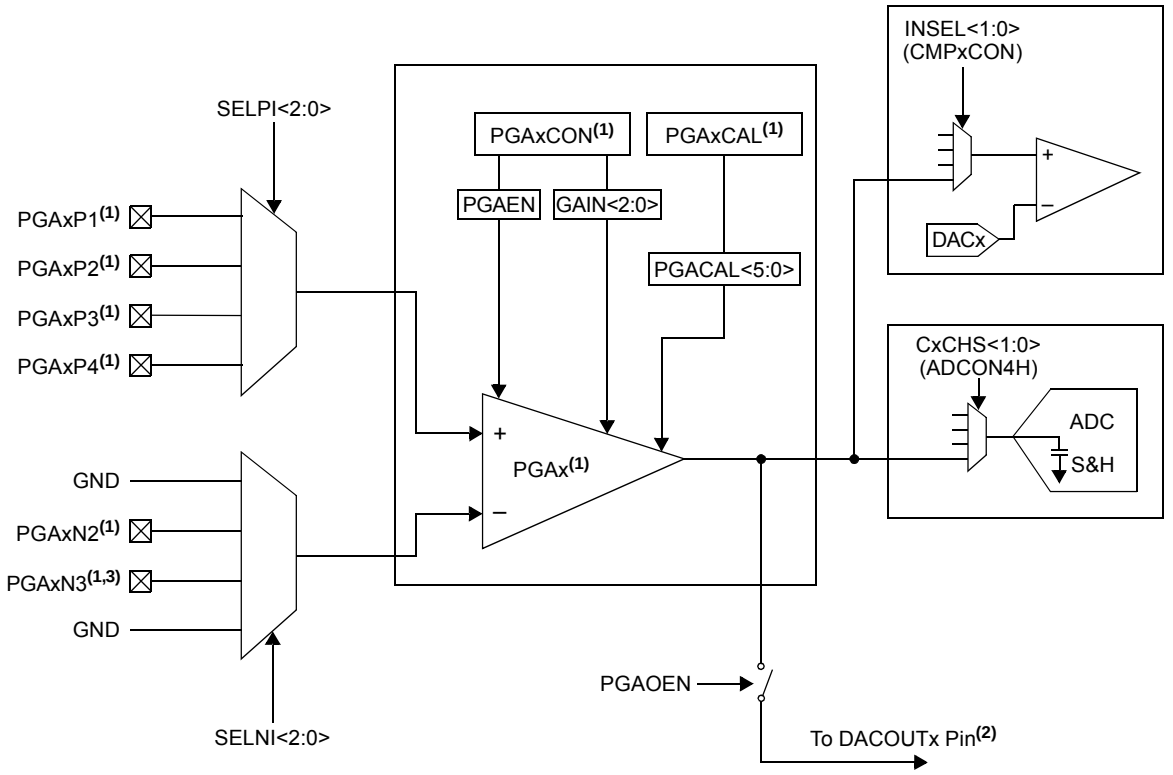
The gain of the PGAx module is selectable via the GAIN<2:0> bits in the PGAxCON register. There are five selectable gains, ranging from 4x to 64x. The SELPI<2:0> and SELNI<2:0> bits in the PGAxCON register select one of four positive/negative inputs to the PGAx module. For single-ended applications, the SELNI<2:0> bits will select the ground as the negative input source. To provide an independent ground reference, PGAxN2 and PGAxN3 pins are available as the negative input source to the PGAx module.

Note 1:	Not all PGA positive/negative inputs are available on all devices. Refer to the specific device pinout for available input source pins.

The output voltage of the PGAx module can be connected to the DACOUTx pin by setting the PGAOEN bit in the PGAxCON register. When the PGAOEN bit is enabled, the output voltage of PGA1 is connected to DACOUT1 and PGA2 is connected to DACOUT2. For devices with a single DACOUTx pin, the output voltage of PGA2 can be connected to DACOUT1 by configuring the DBCC Configuration bit in the FDEVOPT register (FDEVOPT<6>).

If both the DACx output voltage and PGAx output voltage are connected to the DACOUTx pin, the resulting output voltage would be a combination of signals. There is no assigned priority between the PGAx module and the DACx module.

FIGURE 21-2: PGAx FUNCTIONAL BLOCK DIAGRAM



Note 1: x = 1 and 2.
2: The DACOUT2 device pin is only available on 64-pin devices.
3: The PGAxN3 input is not available on 28-pin devices.

TABLE 26-38: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCKx Input Frequency	—	—	11	MHz	**(Note 3)**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH, TscL2ssH	$\overline{SSx}$ ↑ After SCKx Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**

Note 1: These parameters are characterized but not tested in manufacturing.

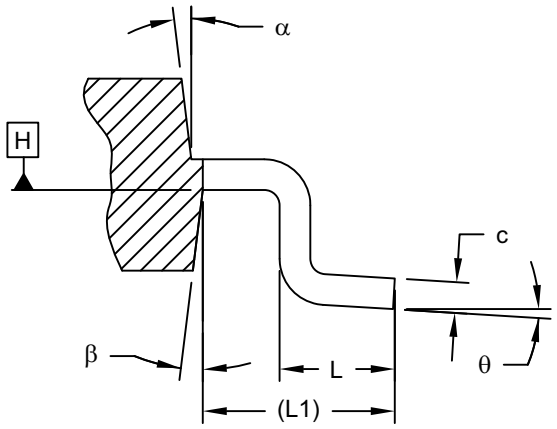
2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

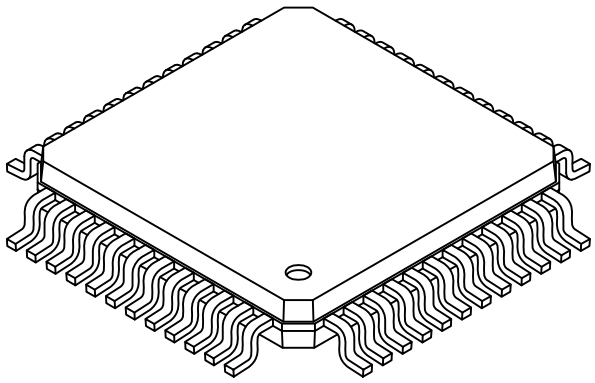
3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

48-Lead Thin Quad Flatpack (Y8) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Lead Thickness	c	0.09	-	0.16
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A-B and D to be determined at center line between leads where leads exit plastic body at datum plane H

Microchip Technology Drawing C04-300-Y8 Rev A Sheet 2 of 2

REFOCON (Reference Oscillator Control) 113
RPINR0 (Peripheral Pin Select Input 0)..... 134
RPINR1 (Peripheral Pin Select Input 1)..... 134
RPINR11 (Peripheral Pin Select Input 11)..... 139
RPINR12 (Peripheral Pin Select Input 12)..... 140
RPINR13 (Peripheral Pin Select Input 13)..... 141
RPINR18 (Peripheral Pin Select Input 18)..... 142
RPINR19 (Peripheral Pin Select Input 19)..... 143
RPINR2 (Peripheral Pin Select Input 2)..... 135
RPINR20 (Peripheral Pin Select Input 20)..... 144
RPINR21 (Peripheral Pin Select Input 21)..... 145
RPINR22 (Peripheral Pin Select Input 22)..... 146
RPINR23 (Peripheral Pin Select Input 23)..... 147
RPINR3 (Peripheral Pin Select Input 3)..... 136
RPINR37 (Peripheral Pin Select Input 37)..... 148
RPINR38 (Peripheral Pin Select Input 38)..... 149
RPINR42 (Peripheral Pin Select Input 42)..... 150
RPINR43 (Peripheral Pin Select Input 43)..... 151
RPINR7 (Peripheral Pin Select Input 7)..... 137
RPINR8 (Peripheral Pin Select Input 8)..... 138
RPOR0 (Peripheral Pin Select Output 0)..... 152
RPOR1 (Peripheral Pin Select Output 1)..... 152
RPOR10 (Peripheral Pin Select Output 10)..... 157
RPOR11 (Peripheral Pin Select Output 11)..... 157
RPOR12 (Peripheral Pin Select Output 12)..... 158
RPOR13 (Peripheral Pin Select Output 13)..... 158
RPOR14 (Peripheral Pin Select Output 14)..... 159
RPOR15 (Peripheral Pin Select Output 15)..... 159
RPOR16 (Peripheral Pin Select Output 16)..... 160
RPOR17 (Peripheral Pin Select Output 17)..... 160
RPOR18 (Peripheral Pin Select Output 18)..... 161
RPOR2 (Peripheral Pin Select Output 2)..... 153
RPOR3 (Peripheral Pin Select Output 3)..... 153
RPOR4 (Peripheral Pin Select Output 4)..... 154
RPOR5 (Peripheral Pin Select Output 5)..... 154
RPOR6 (Peripheral Pin Select Output 6)..... 155
RPOR7 (Peripheral Pin Select Output 7)..... 155
RPOR8 (Peripheral Pin Select Output 8)..... 156
RPOR9 (Peripheral Pin Select Output 9)..... 156
SDCx (PWMx Secondary Duty Cycle)..... 194
SEVTCMP (PWMx Special Event Compare)..... 187
SPHASEx (PWMx Secondary Phase-Shift)..... 196
SPIxCON1 (SPIx Control 1)..... 211
SPIxCON2 (SPIx Control 2)..... 213
SPIxSTAT (SPIx Status and Control)..... 209
SR (CPU STATUS)..... 26, 95
SSEVTCMP (PWMx Secondary Special Event Compare)..... 190
STCON (PWMx Secondary Master Time Base Control)..... 188
STCON2 (PWMx Secondary Clock Divider Select 2)..... 189
STPER (PWMx Secondary Master Time Base Period)..... 189
STRIGx (PWMx Secondary Trigger Compare Value)..... 202
T1CON (Timer1 Control)..... 165
TRGCONx (PWMx Trigger Control)..... 198
TRIGx (PWMx Primary Trigger Compare Value)..... 200
TxCON (Timer2/4 Control)..... 169
TyCON (Timer3/5 Control)..... 170
UxMODE (UARTx Mode)..... 225
UxSTA (UARTx Status and Control)..... 227
Resets 85
Brown-out Reset (BOR)..... 85
Configuration Mismatch Reset (CM) 85
Illegal Condition Reset (IOPUWR) 85
Illegal Opcode 85
Security 85
Uninitialized W Register 85
Master Clear (MCLR) Pin Reset..... 85
Power-on Reset (POR)..... 85
RESET Instruction (SWR) 85
Resources 86
Trap Conflict Reset (TRAPR) 85
Watchdog Timer Time-out Reset (WDTO) 85
Revision History..... 377

S

Serial Peripheral Interface (SPI)..... 207
Serial Peripheral Interface. *See* SPI.
Software Simulator
MPLAB X SIM..... 301
Special Features of the CPU 277
SPI
Control Registers..... 209
Helpful Tips..... 208
Resources 208

T

Thermal Operating Conditions..... 304
Thermal Packaging Characteristics..... 304
Third-Party Development Tools..... 302
Timer1 163
Control Register..... 165
Mode Settings..... 163
Resources 164
Timer2/3 and Timer4/5 167
Control Registers..... 169
Resources 167
Timing Diagrams
BOR and Master Clear Reset Characteristics..... 319
External Clock 316
High-Speed PWMx Fault Characteristics 325
High-Speed PWMx Module Characteristics 325
I/O Characteristics..... 319
I2Cx Bus Data (Master Mode)..... 338
I2Cx Bus Data (Slave Mode)..... 340
I2Cx Bus Start/Stop Bits (Master Mode)..... 338
I2Cx Bus Start/Stop Bits (Slave Mode)..... 340
Input Capture x (ICx) Characteristics 323
OCx/PWMx Characteristics..... 324
Output Compare x (OCx) Characteristics..... 324
SPIx Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1)..... 329
SPIx Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1)..... 328
SPIx Master Mode (Half-Duplex, Transmit Only, CKE = 0) 326
SPIx Master Mode (Half-Duplex, Transmit Only, CKE = 1) 327
SPIx Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0)..... 336
SPIx Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0)..... 334
SPIx Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0)..... 330