Lattice Semiconductor Corporation - LIA-MD6000-6KMG80E Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1484
Number of Logic Elements/Cells	5936
Total RAM Bits	184320
Number of I/O	37
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	80-TFBGA
Supplier Device Package	80-ckfBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lia-md6000-6kmg80e

Contents

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CSI	Camera Serial Interface
DSI	Display Serial Interface
EBR	Embedded Block RAM
ECLK	Edge Clock
FPD	Flat Panel Display
I^2C	Inter-Integrated Circuit
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
NVCM	Non-Volatile Configuration Memory
OTP	One Time Programmable
PCLK	Primary Clock
PFU	Programmable Functional Unit
PLL	Phase Locked Loops
PMU	Power Management Unit
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface

2. Product Feature Summary

Table 2.1 lists CrossLink Automotive device information and package.

Table 2.1. CrossLink Automotive Feature Summary

Device	CrossLink Automotive
LUTs	5936
sysMEM Blocks (9 kb)	20
Embedded Memory (kb)	180
Distributed RAM Bits (kb)	47
General Purpose PLL	1
NVCM	Yes
Embedded I^2C	2
Oscillator (10 KHz)	1
Oscillator (48 MHz)	1
Hardened MIPI D-PHY	2*
Package	**I/O**
80 ctfBGA (6.5 x 6.5 mm^2, 1 mm)	36

***Note**: Additional D-PHY Rx interfaces are available using programmable I/O.

3.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Figure 3.4 shows the block diagram for the MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge. This solution bridges the MIPI DSI output from the application processor to a single or dual channel FPD-Link/OpenLDI LVDS display input.

Table 3.4 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting both RGB666 and RGB888, variable number of LVDS data lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02003, MIPI DSI to OpenLDI/FPD-Link/LVDS Interface Bridge Soft IP User Guide.

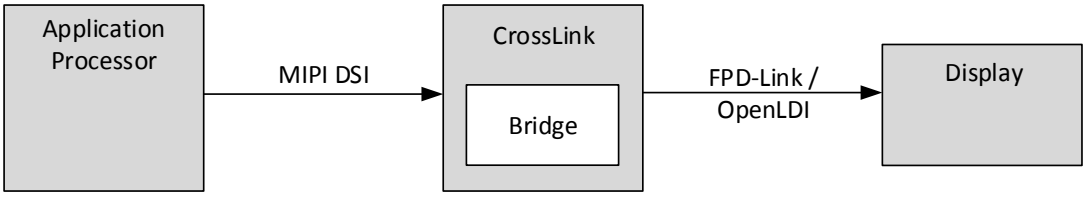


Figure 3.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Table 3.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Bridge
Output Type	1080p60, 24-bit RGB 2 Channels (2 x 4 Data Lanes and 2 x 1 Clock Lane) @ 74.25MHz FPD-Link Clock
Additional System Functions	Display Configuration Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	TBD mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~30% of LUT4; ~30% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

3.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Figure 3.6 shows the block diagram for the CMOS to MIPI CSI-2 Image Sensor Interface Bridge. This solution bridges the CMOS parallel output from an image sensor to a CSI-2 input of an application processor.

Table 3.6 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

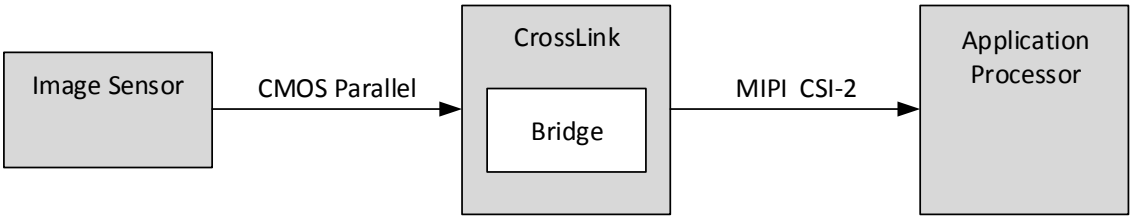


Figure 3.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Table 3.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 12-bit RAW CMOS Parallel @ 74.25 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 12-bit RAW 4-Lane MIPI D-PHY @ ~450 Mb/s per lane
Additional System Functions	I^2C for Camera Configuration GPIO for image sensor reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~75 mW
Device I/O Used	16 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

3.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge

Figure 3.8 shows the block diagram for the MIPI DSI to CMOS display interface bridge. This solution bridges the MIPI DSI output from the application processor to CMOS parallel display input.

Table 3.8 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting multiple pixel formats and data rates up to 1.5 Gb/s per lane input and up to 150 MHz CMOS parallel output. For details, refer to FPGA-IPUG-02004, MIPI D-PHY to CMOS Interface Bridge Soft IP User Guide.

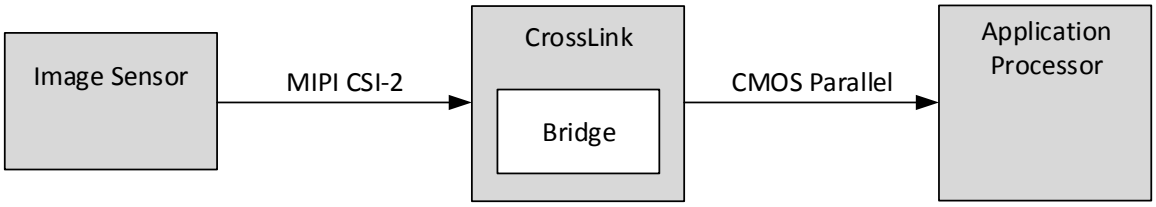


Figure 3.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge

Table 3.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	1080p60, RAW12 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, RAW12 CMOS Parallel @ 74.25 MHz
Additional System Functions	I^2C for Camera Configuration GPIO for image sensor reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	60 mW
Device I/O Used	16 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	15% of LUT4; ~15% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

4. Architecture Overview

CrossLink Automotive is designed as a flexible, chip-to-chip bridging solution which supports a wide variety of applications, including those described in Application Examples section on page 8.

CrossLink Automotive provides three key building blocks for these bridging applications:

- Up to two embedded Hard D-PHY blocks
- Two banks of flexible programmable I/O supporting a variety of standards including D-PHY Rx, subLVDS, SLVS, LVDS, and CMOS
- A programmable logic core providing the LUTs, memory, and system resources to implement a wide range of bridging operations

In addition to these blocks, CrossLink Automotive also provides key system resources including a Power Management Unit, flexible configuration interface, additional CMOS GPIO, and user I^2C blocks.

The block diagram for the device is shown in Figure 4.1.

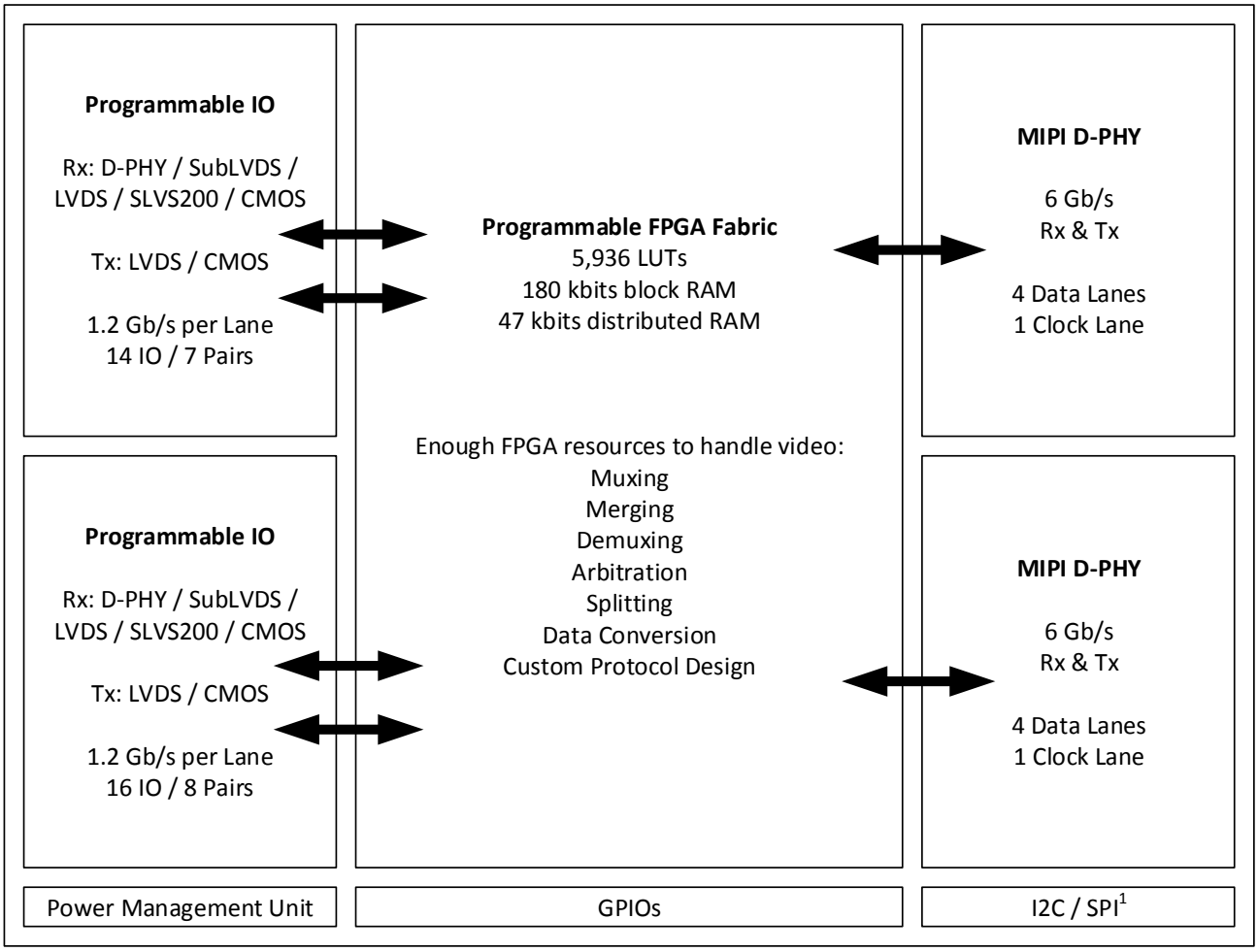


Figure 4.1. CrossLink Automotive Device Block Diagram

Note: I^2C and SPI configuration modes are supported. User mode hardened I^2C is also supported.

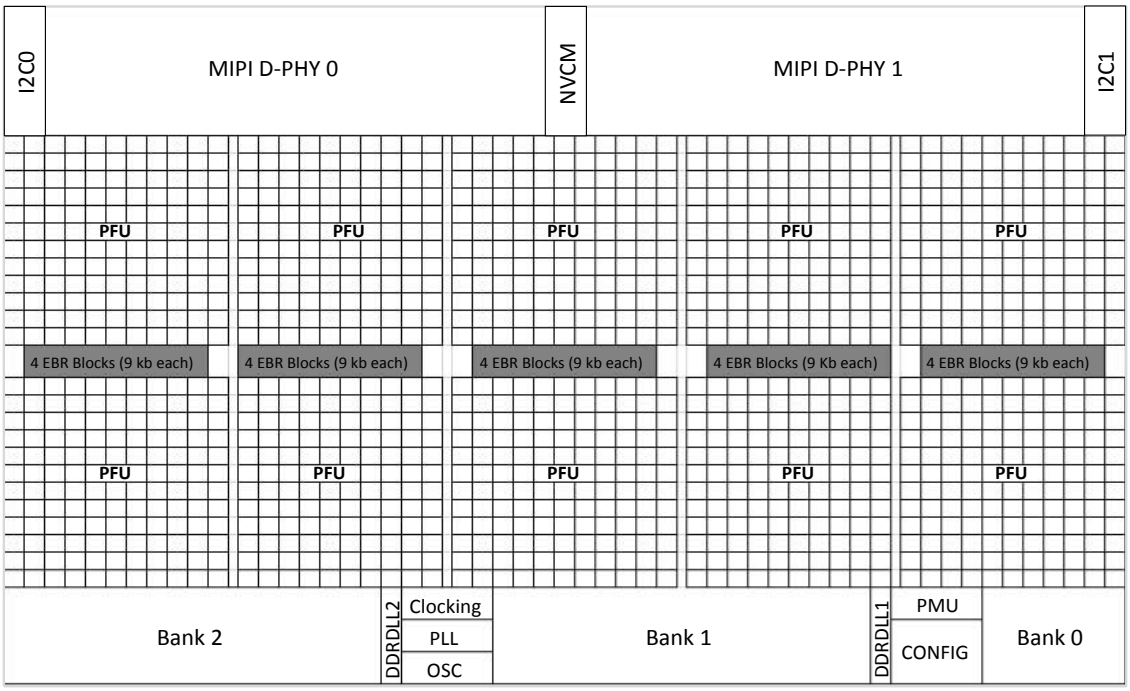


Figure 4.2. CrossLink Automotive Device Simplified Block Diagram (Top Level)

4.3.2. Clocking Overview

The CrossLink Automotive device family provides resources to support a wide range of clocking requirements for programmable video bridging. These resources are listed below. For details, refer to FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide.

- sysCLOCK PLL
  - Flexible Frequency Synthesis (See Table 5.15 for input frequency range and output frequency range.)
  - Dynamically selectable Clock Input
  - Four Clock Outputs
    - Independent, dynamic enable control
    - Programmable phase adjustment
  - Standby Input
  - Lock Output
- Clock Distribution Network
  - Eight Primary Clocks
    - Dedicated Clock input pins (PCLK)
    - Source from PLL, Clock Divider, Hard D-PHY blocks or On-chip Oscillator
  - Four Edge Clocks for high-speed DDR interfaces
    - 2 per Programmable I/O bank
    - Source from PCLK pins, PLL or DLL blocks
    - Programmable Clock divider per Edge Clock
    - Delay primitives for 90 degree phase shifting of clock/data (DDRDLL, DLLDEL)
  - Dynamic Clock Control
    - Fabric control to disable clock nets for power savings
  - Dynamic Clock Select
    - Smart clock multiplexer with two independent inputs and glitchless output support
- Two On-Chip Oscillators
  - Always-on Low Frequency (LFCLKOUT) with nominal frequency of 10 kHz
  - High-Frequency (HFCLKOUT) with nominal frequency of 48 MHz, programmable output dividers, and dynamic enable control

4.3.3. Embedded Block RAM Overview

CrossLink Automotive devices also contain sysMEM Embedded Block RAM (EBR). The EBR consists of a 9 kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Supported modes and other general information on the EBR are listed below. For details, refer to FPGA-TN-02017, LIFMD Memory Usage Guide.

- Support for different memory configurations
  - Single Port
  - True Dual Port
  - Pseudo Dual Port
  - ROM
  - FIFO (logic wrapper added automatically by design tools)
- Flexible customization features
  - Initialization of RAM/ROM
  - Memory cascading (handled automatically by design tools)
  - Optional parity bit support
  - Byte-enable
  - Multiple block size options
  - RAM modes support optional Write Through or Read-Before-Write modes

4.4. System Resources

4.4.1. CMOS GPIO (Bank 0)

CrossLink Automotive provides dedicated CMOS GPIO on Bank 0 of the device. These GPIO do not include differential signaling support. A summary of the features associated with these GPIOs is listed below:

- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12
  - LVTTL33
- Tri-state control for output
- Input/output register blocks
- Open-drain option and programmable input hysteresis
- Internal pull-up resistors with configurable values of 3.3 kΩ, 6.8 kΩ, 10 kΩ

4.4.2. Power Management Unit

The embedded Power Management Unit (PMU) allows low-power Sleep State of the device. Figure 4.3 on the next page shows the block diagram of the PMU IP.

When instantiated in the design, PMU is always on, and uses the low-speed clock from oscillator of the device to perform its operations.

The typical use case for the PMU is through a user implemented state machine that controls the sleep and wake up of the device. The state machine implemented in the FPGA fabric identifies when the device needs to go into sleep mode, issues the command through PMU's FPGA fabric interface, assigns the parameters for sleep (time to wake up and so on) and issues Sleep command.

The device can be woken up externally using the PMU Wake-Up (USRWKUP) pin, or from the PMU Watch Dog Timer expiry or from I2C0 (address decoding detection or FIFO full in one of hardened I^2C).

4.4.3. Device Configuration

The CrossLink Automotive SRAM can be configured as follows:

- Internal Non Volatile Configuration Memory (NVCM)
  - NVCM can be programmed using either the SPI or I^2C port
- Standard Serial Peripheral Interface (Master SPI Mode) Interface to external SPI Flash
- System microprocessor to drive a serial Slave SPI port (SSPI mode)
- System microprocessor to drive a serial Slave I^2C port

For more information, refer to FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide. In addition to the flexible configuration modes, the CrossLink Automotive configuration engine supports the following special features:

- TransFR (Transparent Field Reconfiguration) allowing users to update logic in field without interrupting system operation by freezing I/O states during configuration
- Dual-Boot Support for primary and golden bitstreams provides automatic recovery from configuration failures
- Security and One-Time Programmable (OTP) modes protect bitstream integrity and prevent readback
- 64-bit unique TraceID per device

4.4.4. User I^2C IP

CrossLink Automotive devices have two I^2C IP cores that can be configured either as an I^2C master or as an I^2C slave. The I2C0 core has pre-assigned pins, and supports PMU wakeup over I^2C. The pins for the I2C1 interface are not pre-assigned – user can use any General Purpose I/O pins.

The I^2C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I^2C, refer to FPGA-TN-02019, LIFMD I2C Hardened IP Usage Guide.

5.3. Preliminary Power Supply Ramp Rates

Table 5.3. Preliminary Power Supply Ramp Rates

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies except $V_{CCAUX25VPP}$	0.6	10	V/ms

Note: Assumes monotonic ramp rates.

5.4. Preliminary Power-On-Reset Voltage Levels

Table 5.4. Preliminary Power-On-Reset Voltage Levels

Symbol	Parameter		Typ	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (Monitoring V_{CC}, V_{CCIO0}, and $V_{CCAUX25VPP}$)	V_{CC}	0.685	V
		V_{CCIO0}	1.078	V
		$V_{CCAUX25VPP}$	TBD	V

Notes:

1. These POR ramp up trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. Only V_{CCIO0} has a Power-On-Reset ramp up trip point. All other VCCIOs do not have Power-On-Reset ramp up detection.
3. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and $V_{CCAUX25VPP}$ supplies.
4. Configuration starts after V_{CC}, V_{CCIO0} and $V_{CCAUX25VPP}$ reach V_{PORUP}. For details, see $t_{REFRESH}$ time in Table 5.22 on page 36.
5. Ensure all other VCCIO banks are active with valid input logic levels to properly control any critical output logic states.

5.5. ESD Performance

Refer to the LIFMD Product Family Qualification Summary for complete qualification data, including ESD performance.

5.6. Preliminary DC Electrical Characteristics

Over recommended operating conditions.

Table 5.5. Preliminary DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	$0 \le V_{IN} \le V_{CCIO}$	—	—	±10	µA
I_{PU}[4]	Internal Pull-Up Current	V_{CCIO} = 1.2 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−2.7	—	−31	µA
		V_{CCIO} = 1.8 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−3	—	−31	µA
		V_{CCIO} = 2.5 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−8	—	−72	µA
		V_{CCIO} = 3.3 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−11	—	−128	µA
C1[2]	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	TBD	—	pF
C2[2]	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	TBD	—	pF
V_{HYST}[3]	Hysteresis for Single-Ended Inputs	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	200	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A = 25 °C, f = 1.0 MHz.
3. Hysteresis is not available for V_{CCIO} = 1.2 V.
4. Weak pull-up setting. Programmable pull-up resistors on Bank 0 will see higher current. Refer to FPGA-TN-02016, CrossLink sysI/O Usage Guide for details on programmable pull-up resistors.

5.7. Preliminary CrossLink Automotive Supply Current (Standby)

Over recommended operating conditions.

Table 5.6. Preliminary CrossLink Automotive Supply Current (Standby)

Symbol	Parameter	Typ	Unit
Normal Operation			
I_{CC}	Core Power Supply Current	4.5	mA
I_{CCPLL}	PLL Power Supply Current	0.05	mA
$I_{CCAUX25VPP}$	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	0.5	mA
I_{CCIO}	Bank Power Supply Current (per Bank)	0.5	mA
Sleep Operation			
I_{CC}	Core Power Supply Current	0.6	mA

Notes:

1. For further information on supply current, see the References section on page 44.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0 Hz.
4. Normal operation pattern represents a “blank” configuration data file. Sleep operation includes
5. T_J = 25 °C, power supplies at nominal voltage.
6. To determine the CrossLink Automotive peak start-up current, use the Power Calculator tool in the Lattice Diamond Design Software.

5.8. Preliminary MIPI D-PHY Supply Current

Over recommended operating conditions.

Table 5.7. Preliminary MIPI D-PHY Supply Current[1]

Symbol	Description	Typ	Unit
Standby (Power Down)			
I_{CCA_DPHYx}	VCCA_DPHY Power Supply Current (per Channel) PHY	10	µA
I_{CCPLL_DPHYx}	PLL Supply voltage for D-PHY	5	µA
I_{CCMU_DPHYx}	VCCA_DPHY1 and VCCPLL_DPHY1	15	µA

Notes:

1. For further information on supply current, see the References section on page 44.
2. T_J = 25 °C, power supplies at nominal voltage.

5.9. Preliminary Power Management Unit (PMU) Timing

Table 5.8. Preliminary PMU Timing

Symbol	Parameter	Max	Unit
$t_{PMUWAKE}$	Time for PMU to wake from Sleep mode	1	ms

Note: For details on PMU usage, refer to FPGA-TN-02018, Power Management and Calculation for CrossLink Devices.

5.12. Preliminary sysI/O Differential Electrical Characteristics

5.12.1. Preliminary LVDS/subLVDS/SLVS

Over recommended operating conditions.

Table 5.11. LVDS/subLVDS*/SLVS*

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INPM}	Input Voltage	—	0.00	—	2.40	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two inputs	±100	—	—	mV
$V_{THD(subLVDS)}$	Differential Input Threshold	Difference between the two inputs	±90	—	—	mV
I_{IN}	Input Current	Power On	—	—	±10	µA
		Power Off (standby)	—	—	±10	µA
V_{OH}	Output High Voltage for V_{OP} or VOM	RT = 100 Ω	—	1.43	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ω	0.90	1.08	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), RT = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, RT = 100 Ω	1.13	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V driver outputs shorted to each other	—	—	12	mA

***Note**: Inputs only.

5.12.3. Preliminary CrossLink Automotive Maximum I/O Buffer Speed

Over recommended operating conditions.

Table 5.13. Preliminary CrossLink Automotive Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V	600	MHz
SUBLVDS	SUBLVDS, V_{CCIO} = 2.5 V	600	MHz
MIPI D-PHY (HS Mode)[6]	MIPI D-PHY	600	MHz
SLVS	SLVS, VCCIO=2.5V	600	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	250	MHz
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	250	MHz
LVCMOS25D	Differential LVCMOS, V_{CCIO} = 2.5 V	250	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	250	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	155	MHz
LVCMOS12	LVCMOS 1.2, V_{CCIO} = 1.2 V	70	MHz
Maximum Output Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V	600	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	250	MHz
LVCMOS33	LVCMOS, 3.3 V	250	MHz
LVCMOS33D	Differential LVCMOS, 3.3 V	250	MHz
LVCMOS25	LVCMOS, 2.5 V	250	MHz
LVCMOS25D	Differential LVCMOS, 2.5 V	250	MHz
LVCMOS18	LVCMOS, 1.8 V	155	MHz
LVCMOS12	LVCMOS, VCCIO = 1.2 V	70	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Table 5.23 on page 37.
4. Actual system operation may vary depending on user logic implementation.
5. Maximum data rate equals two times the clock rate when utilizing DDR.
6. This is the maximum MIPI D-PHY input rate on the programmable I/O banks 1 and 2. The hardened MIPI D-PHY input and output rates are described in MIPI D-PHY Performance section on page 35.

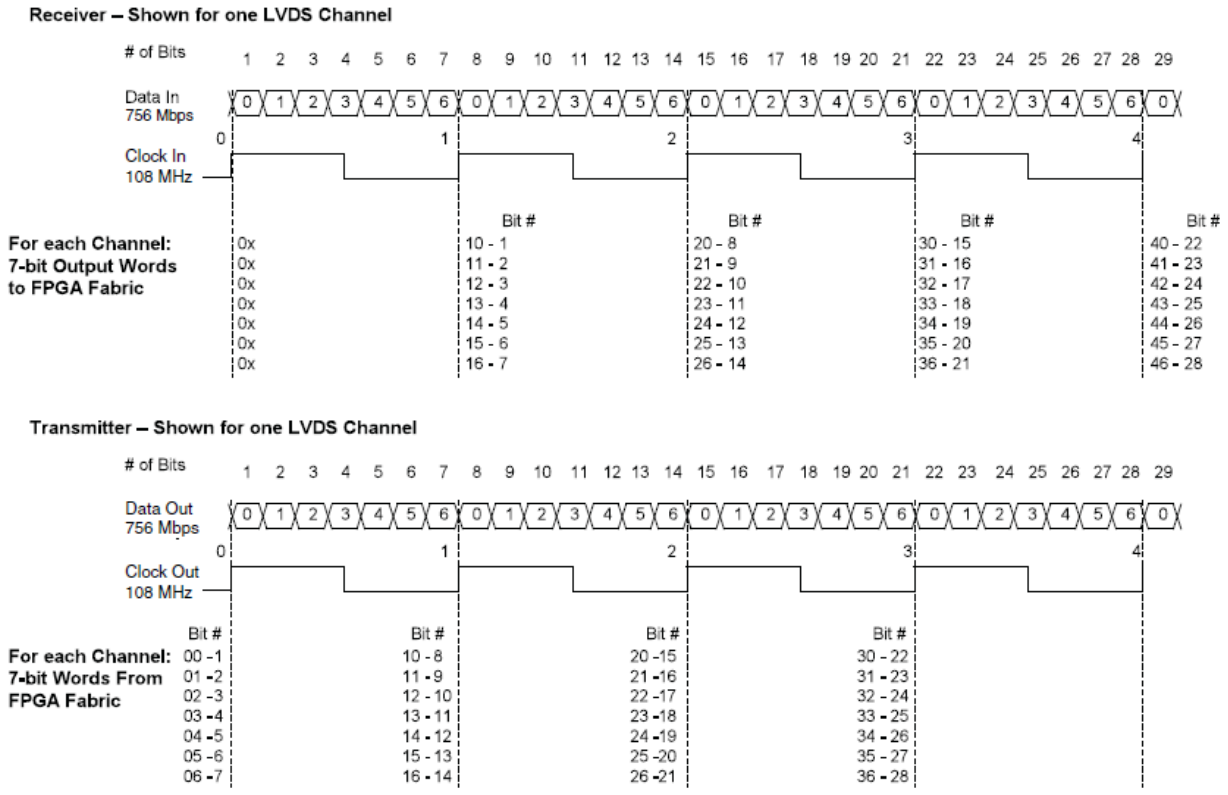


Figure 5.5. DDRX71, DDRX141 Video Timing Waveforms

5.14. MIPI D-PHY Performance

Table 5.16. 1500 Mb/s MIPI_DPHY_X8_RX/TX Timing Table (1500 Mb/s > MIPI D-PHY Data Rate > 1200 Mb/s)

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX8}	Input Data Setup before CLK	0.1387	—	ns
t_{HO_MIPIX8}	Input Data Hold after CLK	0.1387	—	ns
t_{DVB_MIPIX8}	Output Data Valid before CLK Output	0.2080	—	ns
t_{DVA_MIPIX8}	Output Data Valid after CLK Output	0.2080	—	ns

Table 5.17. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s)

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX4}	Input Data Setup before CLK	0.1733	—	ns
t_{HO_MIPIX4}	Input Data Hold after CLK	0.1733	—	ns
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.2060	—	ns
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.2060	—	ns

Table 5.18. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s)

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX4}	Input Data Setup before CLK	0.1560	—	ns
t_{HO_MIPIX4}	Input Data Hold after CLK	0.1560	—	ns
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.3640	—	ns
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.3640	—	ns

5.15. Preliminary Internal Oscillators (HFOSC, LFOSC)

Table 5.19. Preliminary Internal Oscillators

Parameter	Parameter Description	Min	Typ	Max	Unit
f_{CLKHF}	HFOSC CLKK Clock Frequency	43.2	48	52.8	MHz
f_{CLKLF}	LFOSC CLKK Clock Frequency	9	10	11	kHz
DCH_{CLKHF}	HFOSC Duty Cycle (Clock High Period)	45	—	55	%
DCH_{CLKLF}	LFOSC Duty Cycle (Clock High Period)	45	—	55	%

5.16. Preliminary User I^2C[1]

Table 5.20. Preliminary User I^2C[1]

Symbol	Parameter	STD Mode		FAST Mode		FAST Mode Plus		Units
		Min	Max	Min	Max	Min	Max	
f_{scl}	SCL Clock Frequency	—	100	—	400	—	1000[2]	kHz

Notes:

1. Refer to the I^2C Specification for timing requirements.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I.C bus. Internal pull up may not be sufficient to support the maximum speed.

6. Pinout Information

6.1. ctfBGA80 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
A2	DPHY1_DN0	DPHY1_DN0	—	Comp_OF_DPHY1_DP0
A3	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A4	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
A5	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
A6	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A7	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
A8	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
A9	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
A10	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
B1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
B2	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B3	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
B4	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
B5	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
B6	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B7	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
B8	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
B9	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
B10	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
C1	GND	GND	—	—
C2	GNDA_DPHY1	DPHY1	—	—
C9	GNDA_DPHY0	DPHY0	—	—
C10	GND	GND	—	—
D1	PB48	0	PCLKT0_1/USER_SCL	—
D2	VCCPLL_DPHY1	DPHY1	—	—
D4	VCCA_DPHY1	DPHY1	—	—
D5	VCCAUX25VPP	VCCAUX	—	—
D6	GNDPLL_DPHYX	GND	—	—
D7	VCCPLL_DPHY0	DPHY0	—	—
D9	PB16A	2	PCLKT2_0	True_OF_PB16B
D10	PB16B	2	PCLKC2_0	Comp_OF_PB16A
E1	PB34A	1	GR_PCLK1_0	True_OF_PB34B
E2	PB34B	1	—	Comp_OF_PB34A
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCC	VCC	—	—
E7	VCCA_DPHY0	DPHY0	—	—
E9	PB12A	2	GPLLT2_0	True_OF_PB12B
E10	PB12B	2	GPLLC2_0	Comp_OF_PB12A

6.2. Dual Function Pin Descriptions

The following table describes the dual functions available to certain pins on the CrossLink Automotive device. These pins may alternatively be used as general purpose I/O when the described dual function is not enabled.

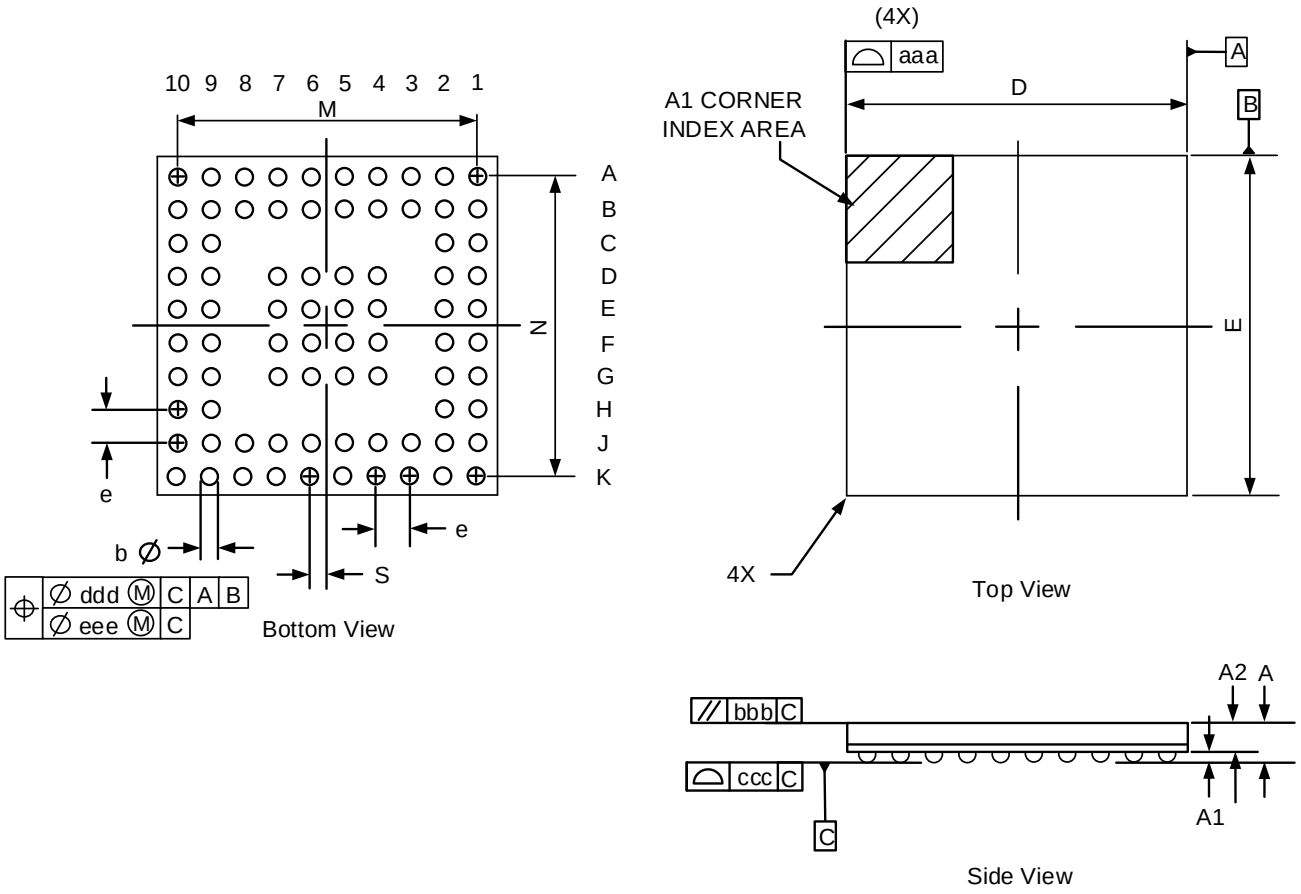
Signal Name	I/O	Description
General Purpose		
USER_SCL	I/O	User Slave I2C0 clock input and Master I²C0 clock output. Enables PMU wake-up via I2C0.
USER_SDA	I/O	User Slave I2C0 data input and Master I²C0 data output. Enables PMU wakeup via I2C0.
PMU_WKUPN	—	This pin wakes the PMU from sleep mode when toggled low.
Clock Functions		
GPLL2_0[T, C]_IN	I	General Purpose PLL (GPLL) input pads: T = true and C = complement. These pins can be used to input a reference clock directly to the General Purpose PLL. These pins do not provide direct access to the primary clock network
GR_PCLK[Bank]0	I	These pins provide a short General Routing path to the primary clock network. Refer to FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide for details.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins provide direct access to the primary and edge clock networks.
MIPI_CLK[T/C][Bank]_0	I/O	MIPI D-PHY Reference CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins can be used to input a reference clock directly to the D-PHY PLLs. These pins do not provide direct access to the primary clock network
Configuration		
CDONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. Holding CDONE delays configuration.
SPI_SCK	I	Input Configuration Clock for configuring CrossLink Automotive in Slave SPI mode (SSPI).
MCK	O	Output Configuration Clock for configuring CrossLink Automotive in Master SPI mode (MSPI).
SPI_SS	I	Input Chip Select for configuring CrossLink Automotive in Slave SPI mode (SSPI).
CSN	O	Output Chip Select for configuring CrossLink Automotive in Master SPI mode (MSPI).
MOSI	I/O	Data Output when configuring CrossLink Automotive in Master SPI mode (MSPI), data input when configuring CrossLink Automotive in Slave SPI mode (SSPI).
MISO	I/O	Data Input when configuring CrossLink Automotive in Master SPI mode (MSPI), data output when configuring CrossLink Automotive in Slave SPI mode (SSPI).
SCL	I/O	Slave I²C clock I/O when configuring CrossLink Automotive in I²C mode
SDA	I/O	Slave I²C data I/O when configuring CrossLink Automotive in I²C mode

6.3. Dedicated Function Pin Descriptions

Signal Name	I/O	Description
Configuration		
CRESET_B	I	Configuration Reset, active LOW.
MIPI D-PHY		
DPHY[num]_CK[P/N]	I/O	MIPI D-PHY Clock [num] = D-PHY 0 or 1, P = Positive, N = Negative.
DPHY[num]_D[P/N][lane]	I/O	MIPI D-PHY Data [num] = D-PHY 0 or 1, P = Positive, N = Negative, Lane = data lane in the D-PHY block 0, 1, 2 or 3.

7. Package Information

Figure 7.1 shows the package dimensions of the 80-ball ctfBGA package.



Item	Min	Typ	Max
A	—	—	1.00
A1	0.11	—	—
A2	0.61	—	—
D/E	6.50 BSC		
M/N	5.85 BSC		
S	0.325 BSC		
b	0.20	0.25	0.30

Item	Min	Typ	Max
e	0.65 BSC		
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.15		
eee	0.05		

Figure 7.1. 80-Ball ctfBGA Package Diagram

7TH Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com