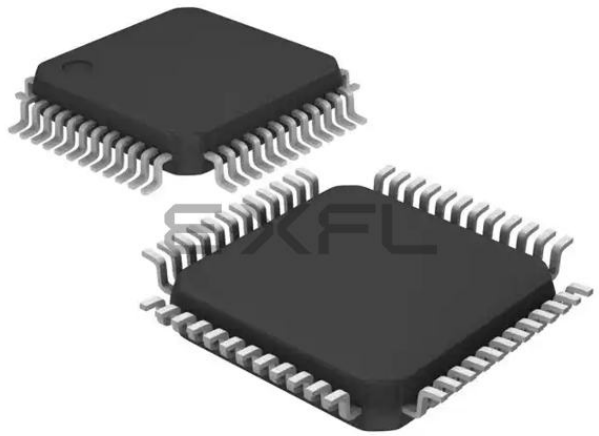

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVR, PWM, RTC, UCID
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc126le4ae

LIST OF FIGURES

- With 8 levels: 4.3 V/ 3.7V/ 2.7V/ 2.2V
- Supports Brown-out Interrupt and Reset option

- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Power consumption

Chip power down current < 10 uA with RAM data retention.
V_{BAT} power domain operating current <1.5 uA

- Operating Temperature: -40℃~105℃
- Packages
  - All Green package (RoHS)

LQFP 100-pin
LQFP 64-pin(7mmx7mm)
LQFP 48-pin

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
			ACMP0_P0	A	MFP5	Analog comparator 0 positive input 0 pin.
			SC1_DAT	I/O	MFP6	Smart Card 1 data pin.
			EBI_AD4	I/O	MFP7	EBI address/data bus bit 4.
4	5	7	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
5	6	8	PD.0	I/O	MFP0	General purpose digital I/O pin.
			SPI0_I2SMCLK	I/O	MFP1	SPI0 I2S master clock output pin
			SPI1_I2SMCLK	I/O	MFP2	SPI1 I2S master clock output pin
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			USCI2_CTL0	I/O	MFP4	USCI2 control 0 pin.
			ACMP1_N	A	MFP5	Analog comparator 1 negative input pin.
			SC1_CLK	O	MFP6	Smart Card 1 clock pin.
			INT3	I	MFP8	External interrupt 3 input pin.
6	7	9	AV_{SS}	P	MFP0	Ground pin for analog circuit.
		10	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
		11	V_{SS}	P	MFP0	Ground pin for digital circuit.
		12	PC.8	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH16	A	MFP1	ADC0 channel 16 analog input.
			UART0_nRTS	O	MFP3	UART0 request to Send output pin.
	8	13	PD.8	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH17	A	MFP1	ADC0 channel 17 analog input.
			UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
			USCI2_CTL1	I/O	MFP4	USCI2 control 1 pin.
			TM2	I/O	MFP6	Timer2 event counter input/toggle output pin.
			EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
	9	14	PD.9	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH18	A	MFP1	ADC0 channel 18 analog input.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			USCI2_CTL0	I/O	MFP4	USCI2 control 0 pin.
			ACMP1_P3	A	MFP5	Analog comparator 1 positive input 3 pin.
			TM3	I/O	MFP6	Timer3 event counter input/toggle output pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
7	10	15	PD.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH19	A	MFP1	ADC0 channel 19 analog input.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
			SPI1_SS	I/O	MFP2	SPI1 slave select pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
			PWM1_CH0	I/O	MFP6	PWM1 channel 0 output/capture input.
			EBI_ADR16	O	MFP7	EBI address bus bit 16.
	18	29	PD.13	I/O	MFP0	General purpose digital I/O pin.
			USCI1_DAT1	I/O	MFP1	USCI1 data 1 pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			PWM1_CH1	I/O	MFP6	PWM1 channel 1 output/capture input.
			EBI_ADR17	O	MFP7	EBI address bus bit 17.
	19	30	PD.14	I/O	MFP0	General purpose digital I/O pin.
			USCI1_DAT0	I/O	MFP1	USCI1 data 0 pin.
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
			UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
			PWM1_CH2	I/O	MFP6	PWM1 channel 2 output/capture input.
			EBI_ADR18	O	MFP7	EBI address bus bit 18.
	20	31	PD.15	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CLK	I/O	MFP1	USCI1 clock pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			UART0_nRTS	O	MFP3	UART0 request to Send output pin.
			PWM1_CH3	I/O	MFP6	PWM1 channel 3 output/capture input.
			EBI_ADR19	O	MFP7	EBI address bus bit 19.
14	21	32	PD.7	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CTL1	I/O	MFP1	USCI1 control 1 pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			PWM0_SYNC_IN	I	MFP3	PWM0 counter synchronous trigger input pin.
			TM1	I/O	MFP4	Timer1 event counter input/toggle output pin.
			ACMP0_O	O	MFP5	Analog comparator 0 output pin.
			PWM0_CH5	I/O	MFP6	PWM0 channel 5 output/capture input.
			EBI_nRD	O	MFP7	EBI read enable output pin.
15	22	33	PF.3	I/O	MFP0	General purpose digital I/O pin.
			XT1_OUT	O	MFP1	External 4~24 MHz (high speed) crystal output pin.
			I2C1_SCL	I/O	MFP3	I2C1 clock pin.
16	23	34	PF.4	I/O	MFP0	General purpose digital I/O pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
45	58	92	PB.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
			VDET_P1	A	MFP2	Voltage detector positive input 1 pin.
			UART2_TXD	O	MFP3	UART2 data transmitter output pin.
			TM3	I/O	MFP4	Timer3 event counter input/toggle output pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
			PWM0_SYNC_OUT	O	MFP6	PWM0 counter synchronous trigger output pin.
			EBI_nWRH	O	MFP7	EBI high byte write enable output pin
			USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
46	59	93	PB.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
			UART1_RXD	I	MFP4	UART1 data receiver input pin.
			SC0_nCD	I	MFP5	Smart Card 0 card detect pin.
			TM_BRAKE0	I	MFP6	Timer Brake 0 input pin.
			EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
			USCI0_DAT0	I/O	MFP8	USCI0 data 0 pin.
			TM2_EXT	I/O	MFP10	Timer2 external capture input/toggle output pin.
47	60	94	PB.3	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
			UART1_TXD	O	MFP4	UART1 data transmitter output pin.
			TM_BRAKE1	I	MFP6	Timer Brake 1 input pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
			USCI0_DAT1	I/O	MFP8	USCI0 data 1 pin.
			TM0_EXT	I/O	MFP10	Timer0 external capture input/toggle output pin.
48	61	95	PB.4	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
			SPI0_SS	I/O	MFP2	SPI0 slave select pin.
			SPI1_SS	I/O	MFP3	SPI1 slave select pin.
			UART1_nCTS	I	MFP4	UART1 clear to Send input pin.
			ACMP0_N	A	MFP5	Analog comparator 0 negative input pin.

4.3.2 GPIO Multi-function Pin Summary

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GP0_MFPL[3:0]=0x0.

PA.9 MFP5 means SYS_GP0_MFPH[7:4]=0x5.

Group	Pin Name	GPIO	MFP*	Type	Description
ACMP0	ACMP0_N	PB.4	MFP5	A	Analog comparator 0 negative input pin.
	ACMP0_O	PD.6	MFP5	O	Analog comparator 0 output pin.
		PD.7	MFP5	O	
	ACMP0_P0	PB.7	MFP5	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	PB.6	MFP5	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	PB.5	MFP5	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	PB.15	MFP5	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	PC.0	MFP5	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	PD.0	MFP5	A	Analog comparator 1 negative input pin.
	ACMP1_O	PC.2	MFP5	O	Analog comparator 1 output pin.
		PC.6	MFP5	O	
	ACMP1_P0	PD.3	MFP5	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	PD.2	MFP5	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	PD.1	MFP5	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	PD.9	MFP5	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	PC.1	MFP5	I	Analog comparator 1 window latch input pin
ADC0	ADC0_CH0	PB.0	MFP1	A	ADC0 channel 0 analog input.
	ADC0_CH1	PB.1	MFP1	A	ADC0 channel 1 analog input.
	ADC0_CH2	PB.2	MFP1	A	ADC0 channel 2 analog input.
	ADC0_CH3	PB.3	MFP1	A	ADC0 channel 3 analog input.
	ADC0_CH4	PB.4	MFP1	A	ADC0 channel 4 analog input.
	ADC0_CH5	PB.8	MFP1	A	ADC0 channel 5 analog input.
	ADC0_CH6	PB.9	MFP1	A	ADC0 channel 6 analog input.
	ADC0_CH7	PB.10	MFP1	A	ADC0 channel 7 analog input.
	ADC0_CH8	PB.11	MFP1	A	ADC0 channel 8 analog input.
	ADC0_CH9	PE.2	MFP1	A	ADC0 channel 9 analog input.
	ADC0_CH10	PB.13	MFP1	A	ADC0 channel 10 analog input.
	ADC0_CH11	PB.14	MFP1	A	ADC0 channel 11 analog input.
	ADC0_CH12	PB.15	MFP1	A	ADC0 channel 12 analog input.
	ADC0_CH13	PB.5	MFP1	A	ADC0 channel 13 analog input.
	ADC0_CH14	PB.6	MFP1	A	ADC0 channel 14 analog input.

Group	Pin Name	GPIO	MFP*	Type	Description
		PE.11	MFP1	I/O	
		PE.12	MFP6	I/O	
	SPI1_SS	PD.6	MFP2	I/O	SPI1 slave select pin.
		PD.12	MFP2	I/O	
		PA.4	MFP2	I/O	
		PE.12	MFP1	I/O	
		PE.13	MFP6	I/O	
		PB.4	MFP3	I/O	
TM0	TM0	PD.1	MFP6	I/O	Timer0 event counter input/toggle output pin.
		PD.4	MFP6	I/O	
		PE.8	MFP3	I/O	
	TM0_EXT	PD.2	MFP3	I/O	Timer0 external capture input/toggle output pin.
		PA.7	MFP3	I/O	
		PE.10	MFP8	I/O	
		PB.3	MFP10	I/O	
\TM1	TM1	PD.5	MFP6	I/O	Timer1 event counter input/toggle output pin.
		PD.7	MFP4	I/O	
		PA.8	MFP8	I/O	
		PE.9	MFP3	I/O	
	TM1_EXT	PD.3	MFP3	I/O	Timer1 external capture input/toggle output pin.
		PA.6	MFP3	I/O	
		PE.11	MFP8	I/O	
		PB.0	MFP10	I/O	
		PB.4	MFP10	I/O	
TM2	TM2	PD.8	MFP6	I/O	Timer2 event counter input/toggle output pin.
		PD.3	MFP1	I/O	
		PD.10	MFP4	I/O	
		PA.14	MFP6	I/O	
		PA.9	MFP8	I/O	
		PB.0	MFP4	I/O	
	TM2_EXT	PE.0	MFP4	I/O	Timer2 external capture input/toggle output pin.
		PA.5	MFP3	I/O	
		PE.12	MFP8	I/O	
		PB.2	MFP10	I/O	

Group	Pin Name	GPIO	MFP*	Type	Description
TM3	TM3	PD.9	MFP6	I/O	Timer3 event counter input/toggle output pin.
		PD.11	MFP4	I/O	
		PA.15	MFP6	I/O	
		PB.1	MFP4	I/O	
	TM3_EXT	PA.4	MFP3	I/O	Timer3 external capture input/toggle output pin.
		PE.1	MFP3	I/O	
		PE.13	MFP8	I/O	
TM	TM_BRAKE0	PA.8	MFP6	I	Timer Brake 0 input pin.
		PB.2	MFP6	I	
	TM_BRAKE1	PA.9	MFP6	I	Timer Brake 1 input pin.
		PA.7	MFP6	I	
		PB.3	MFP6	I	
	TM_BRAKE2	PA.6	MFP6	I	Timer Brake 2 input pin.
		PA.12	MFP6	I	
		PB.8	MFP5	I	
	TM_BRAKE3	PA.5	MFP6	I	Timer Brake 3 input pin.
		PA.13	MFP6	I	
		PE.2	MFP5	I	
UART0	UART0_RXD	PD.0	MFP3	I	UART0 data receiver input pin.
		PD.9	MFP3	I	
		PD.6	MFP3	I	
		PD.13	MFP3	I	
		PE.6	MFP3	I	
		PA.3	MFP2	I	
	UART0_TXD	PD.1	MFP3	O	UART0 data transmitter output pin.
		PD.12	MFP3	O	
		PE.7	MFP3	O	
		PA.2	MFP2	O	
	UART0_nCTS	PD.8	MFP3	I	UART0 clear to Send input pin.
		PD.14	MFP3	I	
		PA.2	MFP3	I	
	UART0_nRTS	PC.8	MFP3	O	UART0 request to Send output pin.
		PD.15	MFP3	O	
		PA.3	MFP3	O	

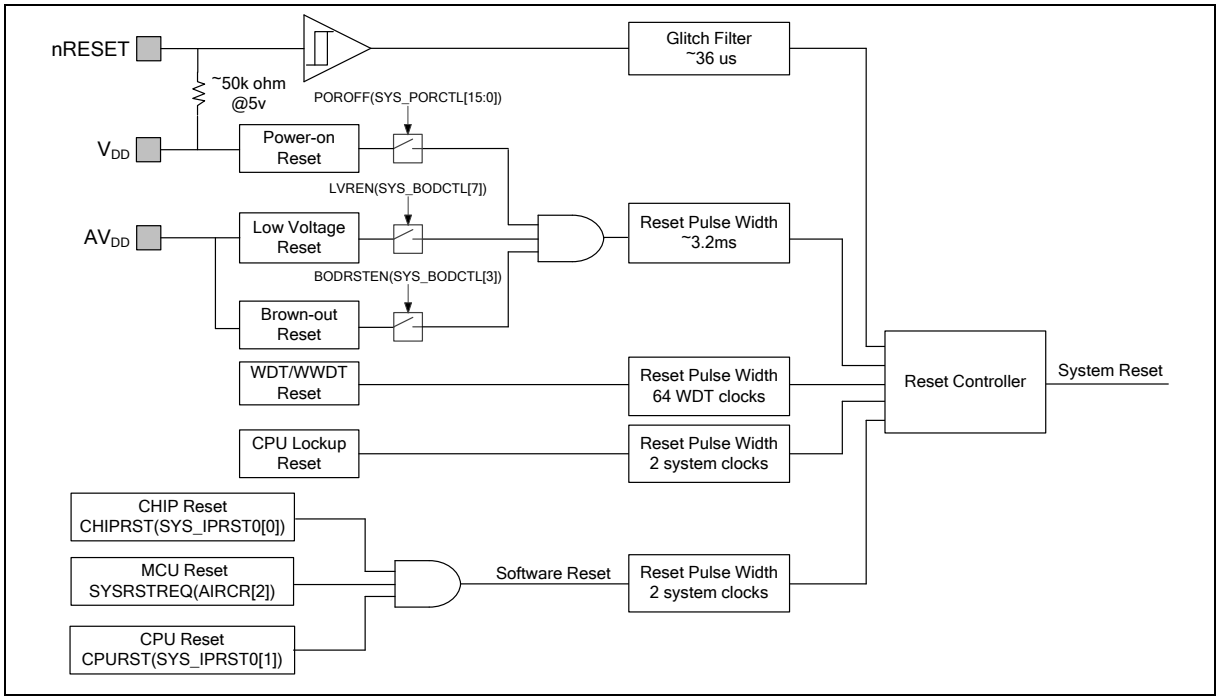


Figure 6.2-1 System Reset Sources

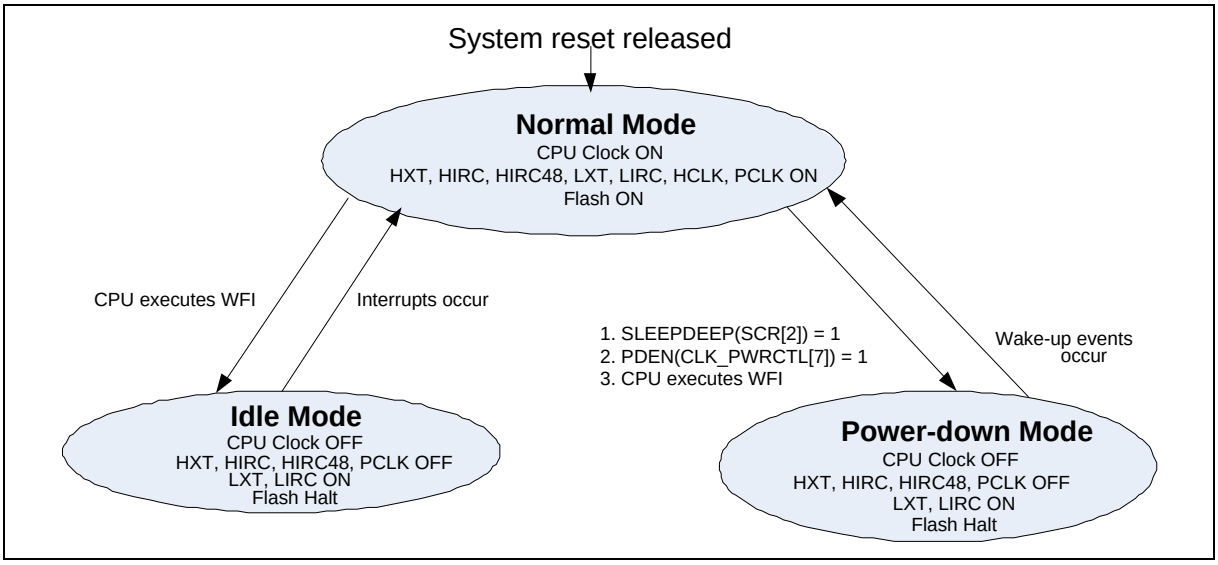


Figure 6.2-6 NuMicro® NUC126 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in normal mode.
2. LIRC (10 kHz OSC) ON or OFF depends on S/W setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~20 MHz XTL)	ON	ON	Halt
HIRC (22.1184 MHz OSC)	ON	ON	Halt
HIRC48 (48 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]

6.2.6 SRAM Memory Orginization

The NUC126 supports embedded SRAM with total 20 Kbytes size in one bank.

- Supports total 20 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

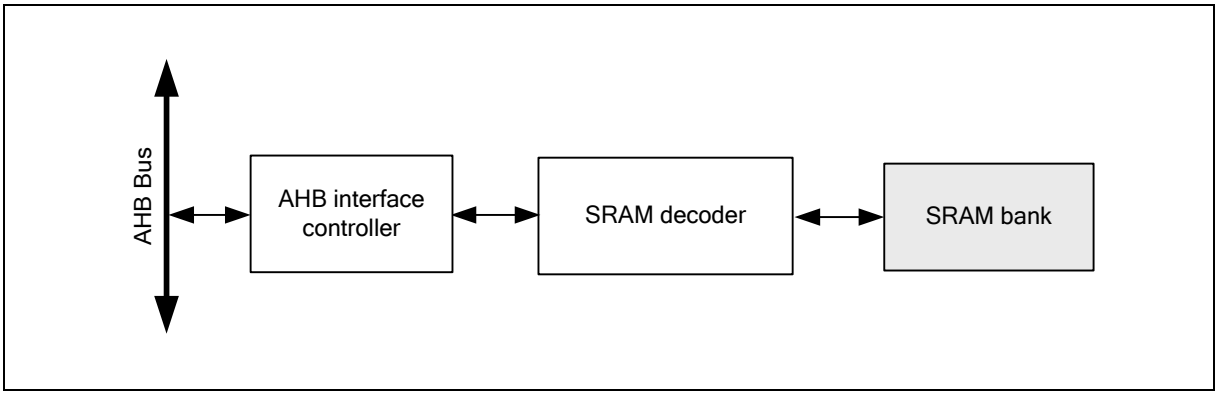


Figure 6.2-8 SRAM Block Diagram

Figure 6.2-9 shows the SRAM organization of NUC126. There is one SRAM bank in the NUC126 and addressed to 20 Kbytes. The address space is from 0x2000_0000 to 0x2000_4FFF. The address between 0x2000_5000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ)	16 ~ 47	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-6 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BOD_INT	Brown-out low voltage detected interrupt
17	1	WDT_INT	Window Watchdog Timer interrupt
18	2	EINT024	External interrupt from PA.0/PC.0/PD.2/PE.0/PE.4 pin
19	3	EINT135	External interrupt from PB.0/PC.0/ PD.0/PD.3/PE.5/PF.0 pin
20	4	GPAB_INT	External signal interrupt from PA[15:0]/PB[13:0]
21	5	GPCDEF_INT	External interrupt from PC[15:0]/PD[15:0]/PE[13:0]/PF[7:0]
22	6	PWM0_INT	PWM0 interrupt
23	7	PWM1_INT	PWM1 interrupt
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART02_INT	UART0 and UART2 interrupt
29	13	UART1_INT	UART1 interrupt
30	14	SPI0_INT	SPI0 interrupt
31	15	SPI1_INT	SPI1 interrupt
32	16		Reserved
33	17		Reserved
34	18	I2C0_INT	I^2C0 interrupt
35	19	I2C1_INT	I^2C1 interrupt
36	20		Reserved
37	21		Reserved
38	22	USCI_INT	USCI0, USCI1 and USCI2 interrupt
39	23	USBD_INT	USB Device interrupt
40	24	SC_INT	SC0 and SC1 interrupt
41	25	ACMP01_INT	Analog Comparator interrupt

6.6 Analog-to-Digital Converter (ADC)

6.6.1 Overview

The NUC126 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with twenty input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC/PD.2), timer0~3 overflow pulse trigger and PWM trigger.

6.6.2 Features

- Analog input voltage range: 0 ~ AV_{DD}.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 20 single-end analog input channels or 10 differential analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Up to 800k SPS sampling rate
- Configurable ADC internal sampling time
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - PWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and Battery power (V_{BAT})
- Support PDMA transfer mode.

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel (V_{TEMP}) is selected to convert, the sampling rate needs to be less than 300k SPS for accurate result.

Note3: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300k SPS.

6.16 Serial Peripheral Interface (SPI)

6.16.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NUC126 series contains up to two sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device.

This controller also supports the PDMA function to access the data buffer. The SPI controller also support I^2S mode to connect external audio CODEC.

6.16.2 Features

- SPI Mode
  - Up to two sets of SPI controllers
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Support receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports PDMA transfer

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD}-V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} – 0.3	V_{DD} + 0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}	I_{DD}	-	120	mA
Maximum Current out of V_{SS}	I_{SS}	-	120	mA
Maximum Current sunk by a I/O Pin	I_{IO}	-	35	mA
Maximum Current Sourced by a I/O Pin		-	35	mA
Maximum Current Sunk by Total I/O Pins		-	100	mA
Maximum Current Sourced by Total I/O Pins		-	100	mA

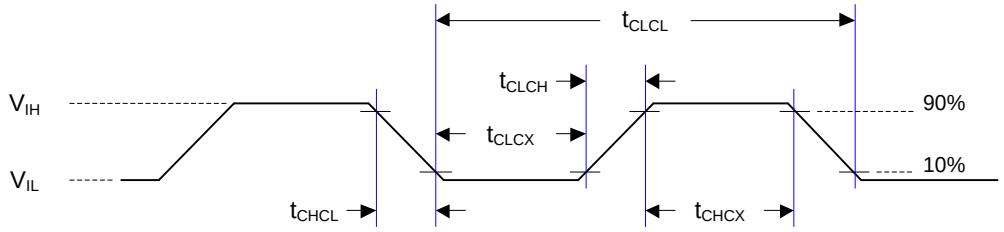
Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNIT						
Normal Run Mode HCLK =32.768 kHz while(1){}executed from flash V_{LDO}=1.8 V						5.5 V	32.768 kHz	X	X	V	
	I_{DD38}	-	123	-	uA	5.5 V	32.768 kHz	X	X	X	
	I_{DD39}	-	123	-	uA	3.3 V	32.768 kHz	X	X	V	
	I_{DD40}	-	109	-	uA	3.3 V	32.768 kHz	X	X	X	
Operating Current Normal Run Mode HCLK =10 kHz while(1){}executed from flash V_{LDO}=1.8 V	I_{DD41}	-	121	-	uA	V_{DD}	LXT	LIRC	PLL	All digital module	
						5.5 V	X	10 kHz	X	V	
	I_{DD42}	-	117	-	uA	5.5 V	X	10 kHz	X	X	
	I_{DD43}	-	107	-	uA	3.3 V	X	10 kHz	X	V	
	I_{DD44}	-	102	-	uA	3.3 V	X	10 kHz	X	X	
Operating Current Idle Mode HCLK =72 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE1}	-	47	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	V	V
	I_{IDLE2}	-	9	-	mA	5.5 V	12 MHz	X	X	V	X
	I_{IDLE3}	-	47	-	mA	3.3 V	12 MHz	X	X	V	V
	I_{IDLE4}	-	9	-	mA	3.3 V	12 MHz	X	X	V	X
Operating Current Idle Mode HCLK =72 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE5}	-	47	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	V	V	V
	I_{IDLE6}	-	9.5	-	mA	5.5 V	X	X	V	V	X
	I_{IDLE7}	-	47	-	mA	3.3 V	X	X	V	V	V
	I_{IDLE8}	-	9.5	-	mA	3.3 V	X	X	V	V	X
Operating Current Idle Mode HCLK =48 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE9}	-	27	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	12 MHz	X	X	V	V
	I_{IDLE10}	-	5.5	-	mA	5.5 V	12 MHz	X	X	V	X
	I_{IDLE11}	-	27	-	mA	3.3 V	12 MHz	X	X	V	V
	I_{IDLE12}	-	5.5	-	mA	3.3 V	12 MHz	X	X	V	X
Operating Current Idle Mode HCLK =48 MHz while(1){}executed from flash V_{LDO}=1.8 V	I_{IDLE13}	-	TBD	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	X	X	V	X	V
	I_{IDLE14}	-	TBD	-	mA	5.5 V	X	X	V	X	X
	I_{IDLE15}	-	TBD	-	mA	3.3 V	X	X	V	X	V
	I_{IDLE16}	-	TBD	-	mA	3.3 V	X	X	V	X	X
Operating Current Idle Mode HCLK =24 MHz	I_{IDLE17}	-	12.5	-	mA	V_{DD}	HXT	HIRC	HIRC48	PLL	All digital module
						5.5 V	24 MHz	X	X	X	V

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Crystal (HXT) Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	10	-	-	nS	
Clock Low Time	t_{CLCX}	10	-	-	nS	
Clock Rise Time	t_{CLCH}	2	-	15	nS	
Clock Fall Time	t_{CHCL}	2	-	15	nS	
Input High Voltage	V_{IH}	$0.7V_{DD}$	-	V_{DD}	V	
Input Low Voltage	V_{IL}	0	-	$0.3V_{DD}$	V	



Note: Duty cycle is 50%.

8.3.2 External 4~24 MHz High Speed Crystal (HXT) Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{HXT}	4	-	24	MHz	V_{DD} = 2.5 ~ 5.5V
Temperature	T_{HXT}	-40	-	+105	°C	
Operating current	I_{HXT}	-	TBD	-	mA	V_{DD} = 5.5V @ 12MHz
		-	0.4	-	mA	V_{DD} = 3.3V @ 12MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
4MHz ~ 24 MHz	20pF	20pF	without

8.3.4 External 32.768 kHz Low Speed Crystal (LXT) Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}	-	32.768	-	kHz	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V
Temperature	T_{LXT}	-40	-	+105	°C	
Operating current	I_{LXT}		0.7		µA	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V

8.3.4.1 Typical Crystal Application Circuits

CRYSTAL	C3	C4	R2
32.768 kHz	20pF	20pF	without

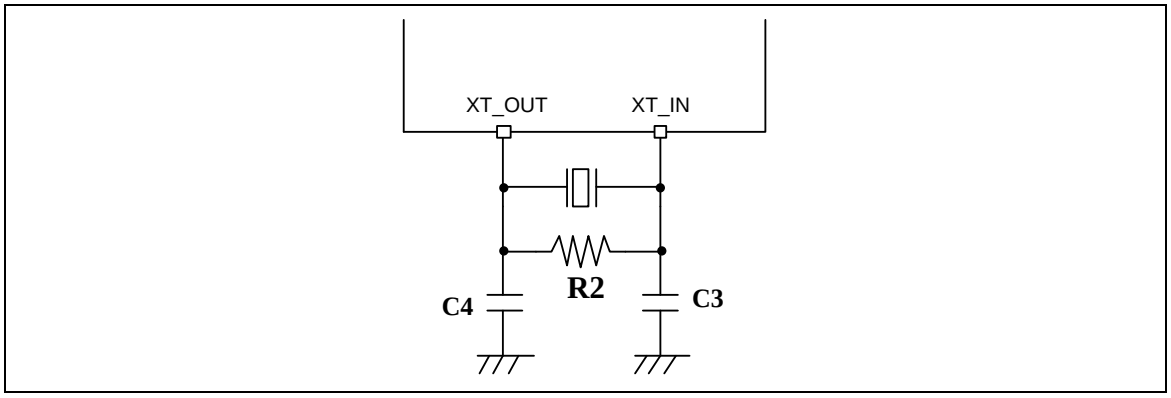


Figure 8.3-2 Typical Crystal Application Circuit

8.3.5 Internal 48 MHz High Speed RC Oscillator (HIRC48)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Center Frequency	f_{HRC}	-	48	-	MHz	T_A = 25°C, V_{DD} = 3.3V
Calibrated Internal Oscillator Frequency		-1	-	+1	%	T_A = 25°C, V_{DD} = 2.5 ~ 5.5V
		-2	-	+2	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V
		-0.25	-	+0.25	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V Auto trimmed by LXT
Operating current	I_{HRC}	-	440	-	μA	

8.3.6 Internal 22.1184 MHz High Speed RC Oscillator (HIRC)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Center Frequency	f_{HRC}	-	22.1184	-	MHz	T_A = 25°C, V_{DD} = 3.3V
Calibrated Internal Oscillator Frequency		-1	-	+1	%	T_A = 25°C, V_{DD} = 2.5 ~ 5.5V
		-2	-	+2	%	-40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V
		-0.25	-	+0.25	%	-40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V Auto trimmed by LXT
Operating current	I_{HRC}	-	470	-	μA	

8.3.7 Internal 10 kHz Low Speed RC Oscillator (LIRC)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Center Frequency	F_{LRC}	-	10	-	kHz	T_A = 25°C, VDD = 3.3V
Calibrated Internal Oscillator Frequency		-30	-	+30	%	T_A = 25 °C, VDD = 2.5 ~ 5.5V