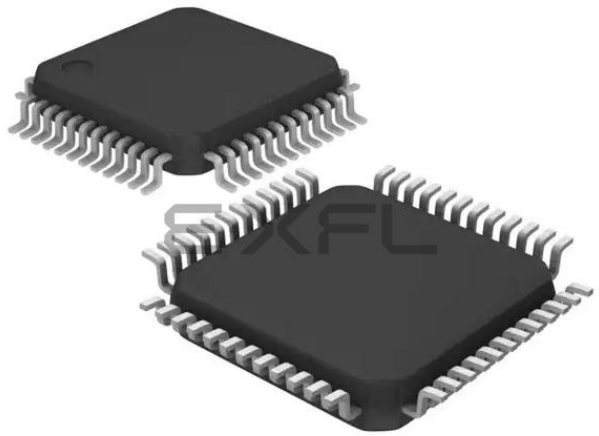

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVR, PWM, RTC, UCID
Number of I/O	35
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc126lg4ae

- Built-in 22.1184 MHz high speed RC oscillator for system operation (Frequency variation < 2% at -40°C ~ +105°C)
- Built-in 48 MHz internal high speed RC oscillator for USB device operation(Frequency variation < 2% at -40°C ~ +105°C)

Built-in 10 kHz low speed RC oscillator for Watchdog Timer and Wake-up operation
Built-in 4~24 MHz high speed crystal oscillator for precise timing operation
Built-in 32.768 kHz low speed crystal oscillator for Real Time Clock
Supports PLL up to 144 MHz for high resolution PWM operation
Supports dynamically calibrating the HIRC48 to 48 MHz ±0.25% by external 32.768K crystal oscillator (LXT)
Supports dynamically calibrating the HIRC to 22.1184Mhz by external 32.768K crystal oscillator (LXT)
Supports clock on-the-fly switch

- Supports clock failure detection for system clock
- Supports auto clock switch once clock failure detected
- Supports exception (NMI) generated once a clock failure detected
- Supports divided clock output

● GPIO

Four I/O modes
TTL/Schmitt trigger input selectable
I/O pin configured as interrupt source with edge/level trigger setting
Supports high driver and high sink current I/O (up to 20 mA at 5V)
Supports software selectable slew rate control
Supports up to 81/49/35 GPIOs for LQFP100/64/48 respectively

● Timer/PWM

Supports 4 sets of Timers/PWM

Timer Mode	PWM Mode
TM_CNT_OUT	PWM_CH0
TM_EXT	PWM_CH1 (Complementary)

Timer Mode

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function to count the event from external pin
- Supports input capture function to capture or reset counter value
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC and PDMA function
- Supports Inter-Timer trigger mode

PWM Mode

- Supports maximum clock frequency up to 50MHz
- Supports independent mode for 4 sets of independent PWM output channel
- Supports complementary mode for 4 sets of complementary paired PWM output channel with 12-bit Dead-time generator
- Supports 12-bit pre-scalar from 1 to 4096

- With 8 levels: 4.3 V/ 3.7V/ 2.7V/ 2.2V
- Supports Brown-out Interrupt and Reset option

- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Power consumption

Chip power down current < 10 uA with RAM data retention.
V_{BAT} power domain operating current <1.5 uA

- Operating Temperature: -40℃~105℃
- Packages
  - All Green package (RoHS)

LQFP 100-pin
LQFP 64-pin(7mmx7mm)
LQFP 48-pin

Group	Pin Name	GPIO	MFP*	Type	Description
		PE.8	MFP4	I/O	
	I2C1_SDA	PF.4	MFP3	I/O	I2C1 data input/output pin.
		PC.10	MFP3	I/O	
		PE.0	MFP3	I/O	
		PC.5	MFP3	I/O	
		PE.5	MFP3	I/O	
		PA.9	MFP2	I/O	
		PE.9	MFP4	I/O	
ICE	ICE_CLK	PE.6	MFP1	I	Serial wired debugger clock pin.
	ICE_DAT	PE.7	MFP1	O	Serial wired debugger data pin.
INT0	INT0	PD.2	MFP8	I	External interrupt 0 input pin.
		PE.4	MFP8	I	
		PA.0	MFP8	I	
INT1	INT1	PD.3	MFP8	I	External interrupt 1 input pin.
		PE.5	MFP8	I	
		PB.0	MFP8	I	
INT2	INT2	PC.0	MFP8	I	External interrupt 2 input pin.
INT3	INT3	PD.0	MFP8	I	External interrupt 3 input pin.
INT4	INT4	PE.0	MFP8	I	External interrupt 4 input pin.
INT5	INT5	PF.0	MFP8	I	External interrupt 5 input pin.
PWM0	PWM0_BRAKE0	PD.2	MFP6	I	PWM0 Brake 0 input pin.
		PD.4	MFP5	I	
		PA.8	MFP7	I	
	PWM0_BRAKE1	PD.3	MFP6	I	PWM0 Brake 1 input pin.
		PD.5	MFP5	I	
	PWM0_CH0	PC.0	MFP6	I/O	PWM0 channel 0 output/capture input.
		PE.0	MFP6	I/O	
	PWM0_CH1	PC.1	MFP6	I/O	PWM0 channel 1 output/capture input.
		PE.1	MFP6	I/O	
	PWM0_CH2	PC.2	MFP6	I/O	PWM0 channel 2 output/capture input.
		PB.8	MFP6	I/O	
		PE.2	MFP6	I/O	
	PWM0_CH3	PE.3	MFP6	I/O	PWM0 channel 3 output/capture input.
		PC.3	MFP6	I/O	

Group	Pin Name	GPIO	MFP*	Type	Description
		PA.1	MFP5	I/O	
	SC0_PWR	PC.3	MFP1	O	Smart Card 0 power pin.
		PE.4	MFP5	O	
		PE.8	MFP5	O	
		PA.3	MFP5	O	
		PA.8	MFP4	O	
	SC0_RST	PC.2	MFP1	O	Smart Card 0 reset pin.
		PE.5	MFP5	O	
		PE.9	MFP5	O	
		PA.2	MFP5	O	
		PB.1	MFP5	O	
		PA.9	MFP4	O	
	SC0_nCD	PC.4	MFP1	I	Smart Card 0 card detect pin.
		PE.0	MFP5	I	
		PE.1	MFP5	I	
		PB.2	MFP5	I	
SC1	SC1_CLK	PD.0	MFP6	O	Smart Card 1 clock pin.
	SC1_DAT	PB.7	MFP6	I/O	Smart Card 1 data pin.
	SC1_PWR	PB.6	MFP6	O	Smart Card 1 power pin.
		PA.9	MFP5	O	
	SC1_RST	PB.5	MFP6	O	Smart Card 1 reset pin.
		PA.8	MFP5	O	
	SC1_nCD	PB.4	MFP6	I	Smart Card 1 card detect pin.
SPI0	SPI0_CLK	PB.7	MFP2	I/O	SPI0 serial clock pin.
		PC.12	MFP2	I/O	
		PC.0	MFP2	I/O	
		PE.0	MFP2	I/O	
		PE.13	MFP2	I/O	
		PB.2	MFP2	I/O	
	SPI0_I2SMCLK	PD.0	MFP1	I/O	SPI0 I2S master clock output pin
		PD.3	MFP2	I/O	
		PD.7	MFP2	I/O	
		PC.9	MFP2	I/O	
		PC.5	MFP2	I/O	

Group	Pin Name	GPIO	MFP*	Type	Description
		PD.9	MFP4	I/O	
		PF.1	MFP5	I/O	
		PC.12	MFP4	I/O	
	USCI2_CTL1	PB.7	MFP4	I/O	USCI2 control 1 pin.
		PD.8	MFP4	I/O	
		PF.0	MFP5	I/O	
		PC.9	MFP4	I/O	
	USCI2_DAT0	PD.2	MFP4	I/O	USCI2 data 0 pin.
		PD.10	MFP5	I/O	
		PC.13	MFP4	I/O	
	USCI2_DAT1	PD.3	MFP4	I/O	USCI2 data 1 pin.
		PD.11	MFP5	I/O	
		PC.10	MFP4	I/O	
VDET	VDET_P0	PB.0	MFP2	A	Voltage detector positive input 0 pin.
	VDET_P1	PB.1	MFP2	A	Voltage detector positive input 1 pin.
X32	X32_IN	PF.1	MFP1	I	External 32.768 kHz crystal input pin.
	X32_OUT	PF.0	MFP1	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PF.4	MFP1	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	PF.3	MFP1	O	External 4~24 MHz (high speed) crystal output pin.

Table 4.3-1 NUC126 GPIO Multi-function Table

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2.5 System Memory Map

The NUC126 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-5. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NUC126 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 KB)
0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256 KB)
0x0004_0000 – 0x0005_FFFF	Reserved	Reserved
0x0006_0000 – 0x0007_FFFF	Reserved	Reserved
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20 KB)
0x2000_4000 – 0x2000_BFFF	Reserved	Reserved
0x2000_C000 – 0x2000_FFFF	Reserved	Reserved
0x6000_0000 – 0x601F_FFFF	EXTMEM_BA	External Memory Space for EBI Interface (2 MB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	EBI Control Registers
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware Divider Registers
0x5001_8000 – 0x5001_FFFF	CRC_BA	CRC Generator Registers
Peripheral Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	Reserved	Reserved
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x4007_0000 – 0x4007_3FFF	USCI0_BA	USCI0 Control Registers

6.2.10 Voltage Detector (VDET)

This chip supports low power comparator to detect external voltage. User can control Bandgap active interval and comparator active interval to achieve low power detection purpose. There is no debounce function in Power-down mode since no HCLK available in Power-down mode.

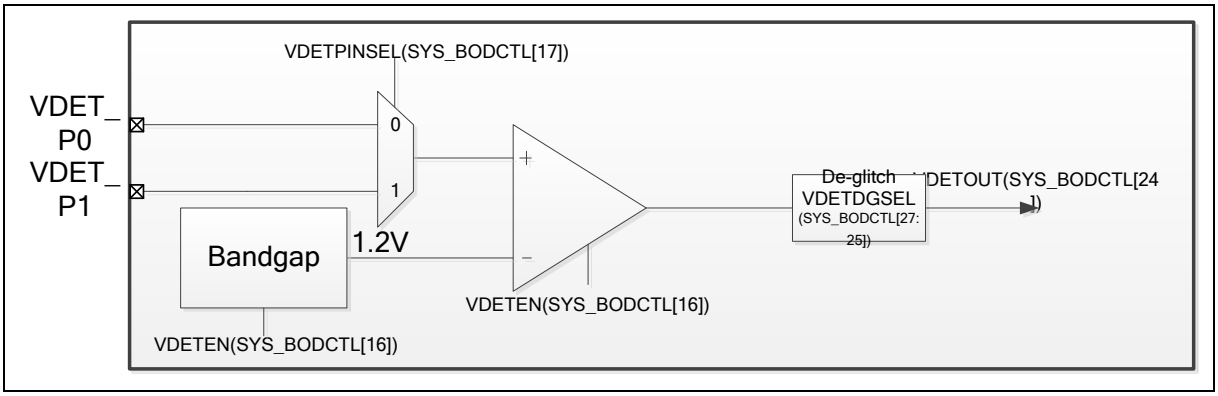


Figure 6.2-11 VDET Block Diagram

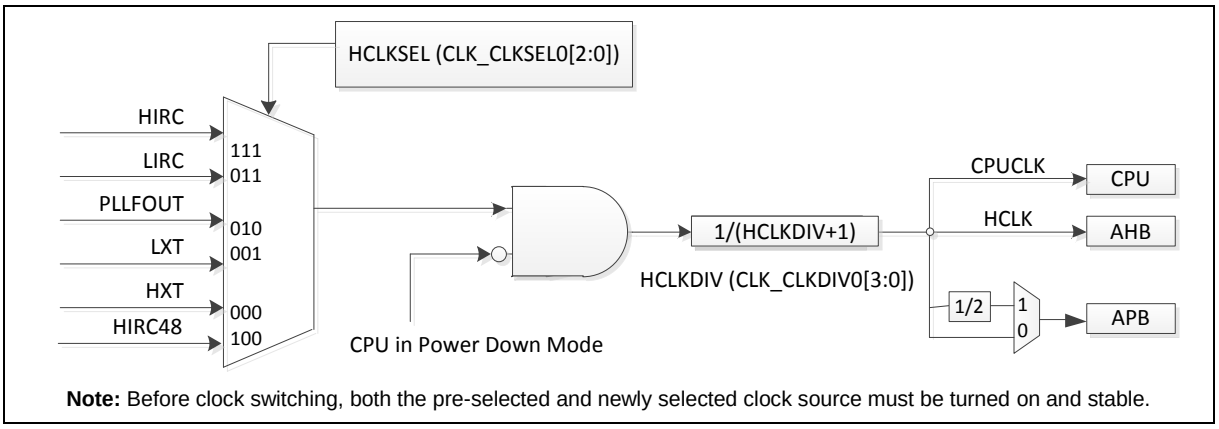
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ)	16 ~ 47	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-6 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BOD_INT	Brown-out low voltage detected interrupt
17	1	WDT_INT	Window Watchdog Timer interrupt
18	2	EINT024	External interrupt from PA.0/PC.0/PD.2/PE.0/PE.4 pin
19	3	EINT135	External interrupt from PB.0/PC.0/ PD.0/PD.3/PE.5/PF.0 pin
20	4	GPAB_INT	External signal interrupt from PA[15:0]/PB[13:0]
21	5	GPCDEF_INT	External interrupt from PC[15:0]/PD[15:0]/PE[13:0]/PF[7:0]
22	6	PWM0_INT	PWM0 interrupt
23	7	PWM1_INT	PWM1 interrupt
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART02_INT	UART0 and UART2 interrupt
29	13	UART1_INT	UART1 interrupt
30	14	SPI0_INT	SPI0 interrupt
31	15	SPI1_INT	SPI1 interrupt
32	16		Reserved
33	17		Reserved
34	18	I2C0_INT	I^2C0 interrupt
35	19	I2C1_INT	I^2C1 interrupt
36	20		Reserved
37	21		Reserved
38	22	USCI_INT	USCI0, USCI1 and USCI2 interrupt
39	23	USBD_INT	USB Device interrupt
40	24	SC_INT	SC0 and SC1 interrupt
41	25	ACMP01_INT	Analog Comparator interrupt

6.3.2 System Clock and SysTick Clock

The system clock has 6 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0 [2:0]). The block diagram is shown in Figure 6.3-3.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6.3-4.

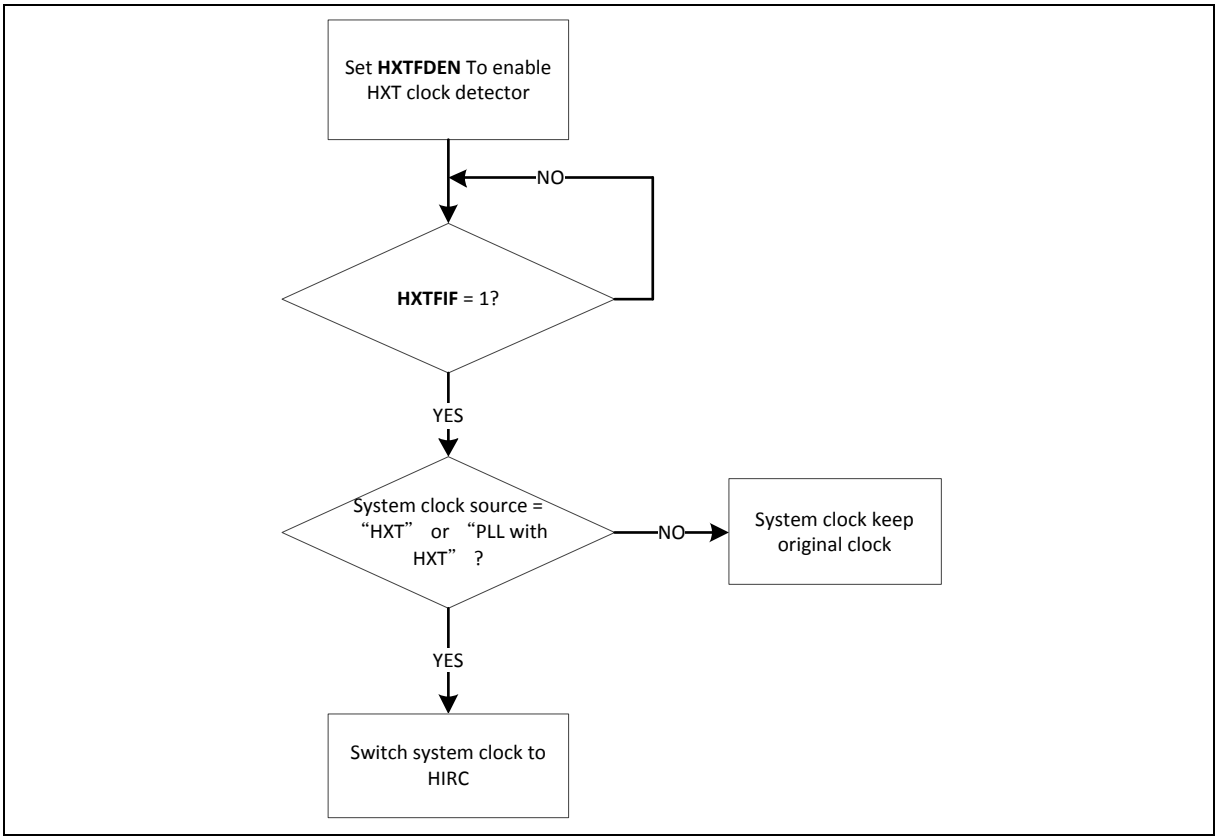
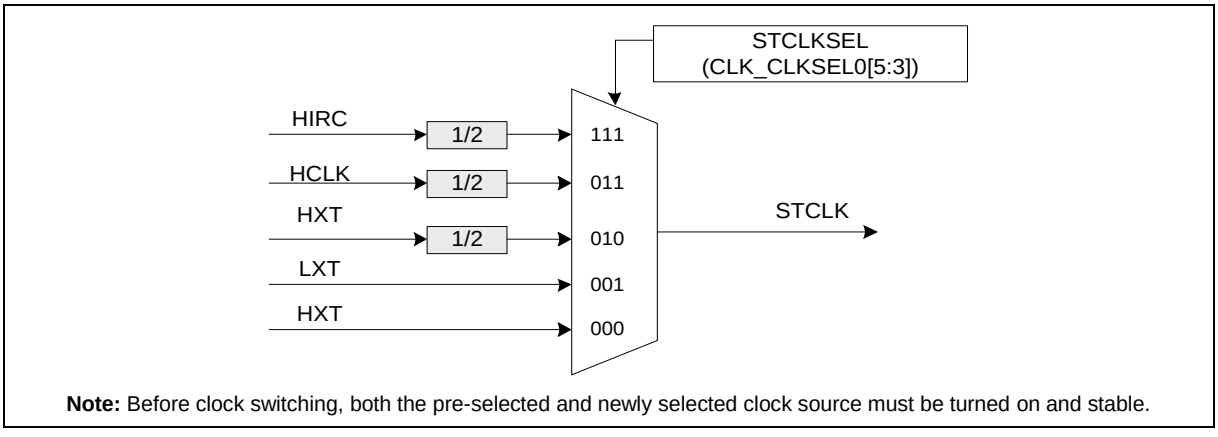


Figure 6.3-4 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.3 Peripherals Clock

The peripherals clock had different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register description in section 6.3.7.

6.6 Analog-to-Digital Converter (ADC)

6.6.1 Overview

The NUC126 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with twenty input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC/PD.2), timer0~3 overflow pulse trigger and PWM trigger.

6.6.2 Features

- Analog input voltage range: 0 ~ AV_{DD}.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 20 single-end analog input channels or 10 differential analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Up to 800k SPS sampling rate
- Configurable ADC internal sampling time
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - PWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and Battery power (V_{BAT})
- Support PDMA transfer mode.

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel (V_{TEMP}) is selected to convert, the sampling rate needs to be less than 300k SPS for accurate result.

Note3: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300k SPS.

6.12 PDMA Controller (PDMA)

6.12.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 5 channels and each channel can perform transfer between memory and peripherals or between memory and memory. The PDMA supports time-out function for channel 0 and channel 1.

6.12.2 Features

- Supports 5 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, I^2S, I^2C, USB, ADC, PWM and TIMER request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function for channel0 and channel 1

6.14 Real Time Clock (RTC)

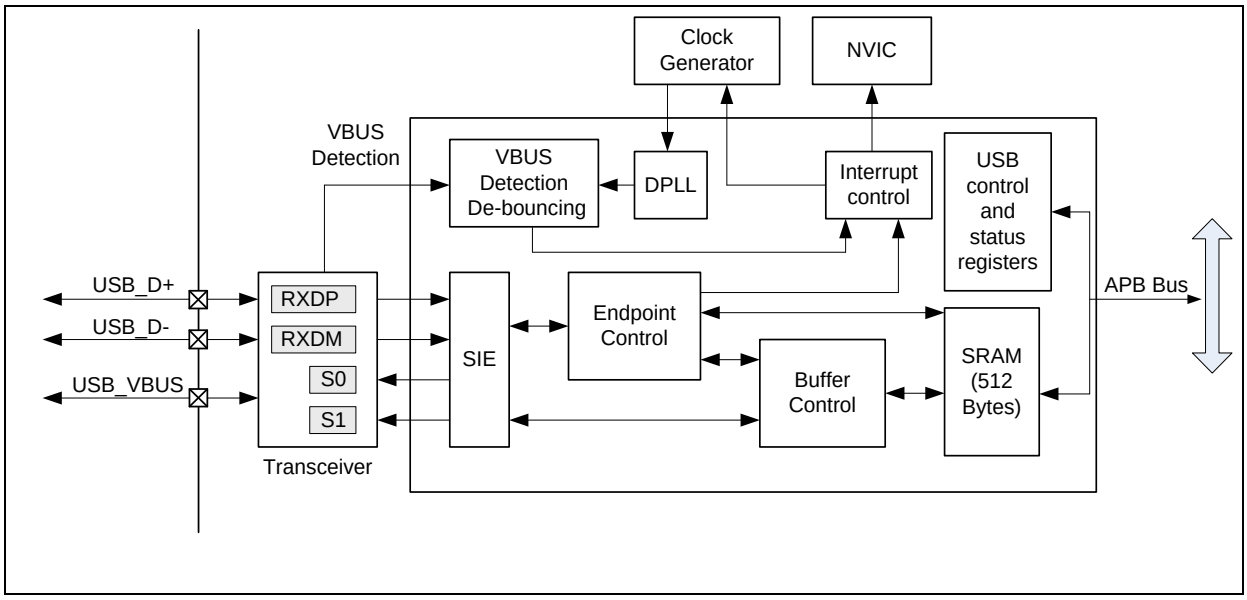
6.14.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.14.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register
-
- Supports Leap Year indication in RTC_LEAPYEAR register
- Supports Day of the Week counter in RTC_WEEKDAY register
- Frequency of RTC clock source compensate by RTC_FREQADJ register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle or Power-down mode while an RTC interrupt signal is generated
- Supports Daylight Saving Time backup control in RTC_DSTCTL

- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events


Clock Generator
NVIC
VBUS Detection
VBUS Detection De-bouncing
DPLL
Interrupt control
USB control and status registers
APB Bus
USB_D+
USB_D-
USB_VBUS
RXDP
RXDM
S0
S1
Transceiver
SIE
Endpoint Control
Buffer Control
SRAM (512 Bytes)

6.19 USCI – Universal Serial Control Interface Controller

6.19.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.19.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.20 USCI – UART Mode

6.20.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake up the system.

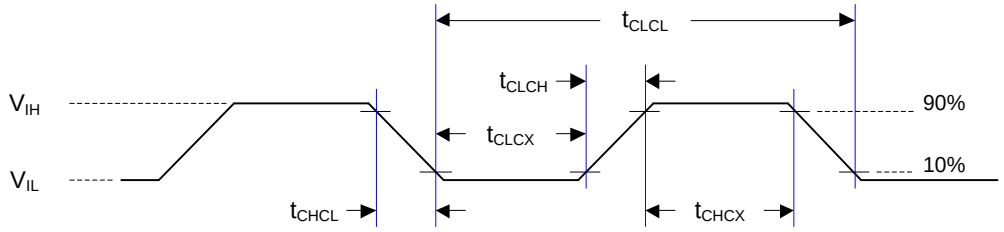
6.20.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-Bit Data Transfer (Support 9-Bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports Wake-up function (Data and nCTS Wakeup Only)

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Crystal (HXT) Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	10	-	-	nS	
Clock Low Time	t_{CLCX}	10	-	-	nS	
Clock Rise Time	t_{CLCH}	2	-	15	nS	
Clock Fall Time	t_{CHCL}	2	-	15	nS	
Input High Voltage	V_{IH}	$0.7V_{DD}$	-	V_{DD}	V	
Input Low Voltage	V_{IL}	0	-	$0.3V_{DD}$	V	



Note: Duty cycle is 50%.

8.3.2 External 4~24 MHz High Speed Crystal (HXT) Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{HXT}	4	-	24	MHz	V_{DD} = 2.5 ~ 5.5V
Temperature	T_{HXT}	-40	-	+105	°C	
Operating current	I_{HXT}	-	TBD	-	mA	V_{DD} = 5.5V @ 12MHz
		-	0.4	-	mA	V_{DD} = 3.3V @ 12MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
4MHz ~ 24 MHz	20pF	20pF	without

t_{DH}	Data hold time	2*PCLK+6	-	-	ns
t_V	Data output valid time	-	2*PCLK+19	2*PCLK+25	ns

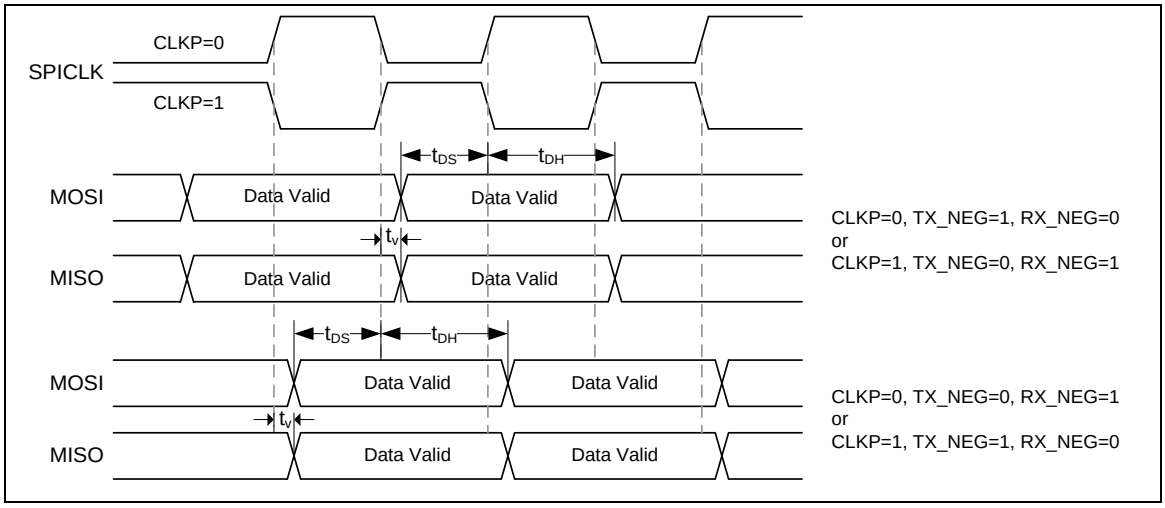


Figure 8.7-2 SPI Slave Mode Timing Diagram