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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVR, PWM, RTC, UCID
Number of I/O	49
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 15x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc126se4ae

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1.1 Key Feature and Application

Product Line	USB	USCI	UART	I^2C	SPI/I^2S	ISO 7816	PWM	EBI	PDMA	ADC	ACMP	RTC V_{BAT}	1.8V IO
NUC126	2.0 FS Device	3	3	2	2	2	12	Y	5	20	2	Y	Y

Table 1.1-1 Key Features Support Table

The NuMicro® NUC126 series is suitable for a wide range of applications such as:

- Industrial Automation
- PLCs
- Inverters
- Home Automation
- Security Alarm System
- Power Metering
- Portable Data Collector
- Portable RFID Reader
- System Supervisors
- Smart Card Reader
- Printer
- Bar Code Scanner
- Motor Control
- Digital Power

- Built-in 22.1184 MHz high speed RC oscillator for system operation (Frequency variation < 2% at -40°C ~ +105°C)
- Built-in 48 MHz internal high speed RC oscillator for USB device operation(Frequency variation < 2% at -40°C ~ +105°C)

Built-in 10 kHz low speed RC oscillator for Watchdog Timer and Wake-up operation
Built-in 4~24 MHz high speed crystal oscillator for precise timing operation
Built-in 32.768 kHz low speed crystal oscillator for Real Time Clock
Supports PLL up to 144 MHz for high resolution PWM operation
Supports dynamically calibrating the HIRC48 to 48 MHz ±0.25% by external 32.768K crystal oscillator (LXT)
Supports dynamically calibrating the HIRC to 22.1184Mhz by external 32.768K crystal oscillator (LXT)
Supports clock on-the-fly switch

- Supports clock failure detection for system clock
- Supports auto clock switch once clock failure detected
- Supports exception (NMI) generated once a clock failure detected
- Supports divided clock output

● GPIO

Four I/O modes
TTL/Schmitt trigger input selectable
I/O pin configured as interrupt source with edge/level trigger setting
Supports high driver and high sink current I/O (up to 20 mA at 5V)
Supports software selectable slew rate control
Supports up to 81/49/35 GPIOs for LQFP100/64/48 respectively

● Timer/PWM

Supports 4 sets of Timers/PWM

Timer Mode	PWM Mode
TM_CNT_OUT	PWM_CH0
TM_EXT	PWM_CH1 (Complementary)

Timer Mode

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function to count the event from external pin
- Supports input capture function to capture or reset counter value
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC and PDMA function
- Supports Inter-Timer trigger mode

PWM Mode

- Supports maximum clock frequency up to 50MHz
- Supports independent mode for 4 sets of independent PWM output channel
- Supports complementary mode for 4 sets of complementary paired PWM output channel with 12-bit Dead-time generator
- Supports 12-bit pre-scalar from 1 to 4096

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface

4.1.2 NuMicro® NUC126 USB Series (M452 Compatible) Selection Guide

Part Number	Flash (KB)	SRAM (KB)	Data Flash(KB)	SPROM(KB)	ISP ROM (KB)	I/O	Timer/PWM	PWM		Connectivity					ADC(12-Bit)	ACMP	PDMA	VBAT(RTC)	LVIO	EBI	ICP/IAP/ISP	Package
									USBD	USCI*	UART	SC/UART	SPI/I²S	I²C								
NUC126LE4AE	128	20	Conf*	2	4	35	4	10	1	3	3	2	2	2	9-ch	2	5	--	√	√	√	LQFP 48
NUC126LG4AE	256	20	Conf*	2	4	35	4	10	1	3	3	2	2	2	9-ch	2	5	--	√	√	√	LQFP 48
NUC126SE4AE	128	20	Conf*	2	4	49	4	12	1	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP 64*
NUC126SG4AE	256	20	Conf*	2	4	49	4	12	1	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP 64*
NUC126VG4AE	256	20	Conf*	2	4	81	4	12	1	3	3	2	2	2	20-ch	2	5	√	√	√	√	LQFP 100

Conf*: Configurable
USCI*: support UART, SPI or I²C
LQFP64*: 7x7 mm

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
			PWM0_BRAKE1	I	MFP5	PWM0 Brake 1 input pin.
			TM1	I/O	MFP6	Timer1 event counter input/toggle output pin.
		20	PE.3	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			UART2_RXD	I	MFP4	UART2 data receiver input pin.
			PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		21	PD.6	I/O	MFP0	General purpose digital I/O pin.
			CLKO	O	MFP1	Clock Out
			SPI1_SS	I/O	MFP2	SPI1 slave select pin.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			UART2_TXD	O	MFP4	UART2 data transmitter output pin.
			ACMP0_O	O	MFP5	Analog comparator 0 output pin.
			PWM0_CH5	I/O	MFP6	PWM0 channel 5 output/capture input.
			EBI_nWR	O	MFP7	EBI write enable output pin.
10	13	22	V_{BAT}	P	MFP0	Power supply by batteries for RTC.
11	14	23	PF.0	I/O	MFP0	General purpose digital I/O pin.
			X32_OUT	O	MFP1	External 32.768 kHz crystal output pin.
			USCI2_CTL1	I/O	MFP5	USCI2 control 1 pin.
			INT5	I	MFP8	External interrupt 5 input pin.
12	15	24	PF.1	I/O	MFP0	General purpose digital I/O pin.
			X32_IN	I	MFP1	External 32.768 kHz crystal input pin.
			USCI2_CTL0	I/O	MFP5	USCI2 control 0 pin.
			PWM1_BRAKE0	I	MFP6	PWM1 Brake 0 input pin.
13	16	25	PF.2	I/O	MFP0	General purpose digital I/O pin.
			USCI2_CLK	I/O	MFP5	USCI2 clock pin.
			PWM1_BRAKE1	I	MFP6	PWM1 Brake 1 input pin.
		26	PD.10	I/O	MFP0	General purpose digital I/O pin.
			TM2	I/O	MFP4	Timer2 event counter input/toggle output pin.
			USCI2_DAT0	I/O	MFP5	USCI2 data 0 pin.
		27	PD.11	I/O	MFP0	General purpose digital I/O pin.
			TM3	I/O	MFP4	Timer3 event counter input/toggle output pin.
			USCI2_DAT1	I/O	MFP5	USCI2 data 1 pin.
	17	28	PD.12	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CTL0	I/O	MFP1	USCI1 control 0 pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
			SPI1_SS	I/O	MFP2	SPI1 slave select pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
			PWM1_CH0	I/O	MFP6	PWM1 channel 0 output/capture input.
			EBI_ADR16	O	MFP7	EBI address bus bit 16.
	18	29	PD.13	I/O	MFP0	General purpose digital I/O pin.
			USCI1_DAT1	I/O	MFP1	USCI1 data 1 pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			PWM1_CH1	I/O	MFP6	PWM1 channel 1 output/capture input.
			EBI_ADR17	O	MFP7	EBI address bus bit 17.
	19	30	PD.14	I/O	MFP0	General purpose digital I/O pin.
			USCI1_DAT0	I/O	MFP1	USCI1 data 0 pin.
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
			UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
			PWM1_CH2	I/O	MFP6	PWM1 channel 2 output/capture input.
			EBI_ADR18	O	MFP7	EBI address bus bit 18.
	20	31	PD.15	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CLK	I/O	MFP1	USCI1 clock pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			UART0_nRTS	O	MFP3	UART0 request to Send output pin.
			PWM1_CH3	I/O	MFP6	PWM1 channel 3 output/capture input.
			EBI_ADR19	O	MFP7	EBI address bus bit 19.
14	21	32	PD.7	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CTL1	I/O	MFP1	USCI1 control 1 pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			PWM0_SYNC_IN	I	MFP3	PWM0 counter synchronous trigger input pin.
			TM1	I/O	MFP4	Timer1 event counter input/toggle output pin.
			ACMP0_O	O	MFP5	Analog comparator 0 output pin.
			PWM0_CH5	I/O	MFP6	PWM0 channel 5 output/capture input.
			EBI_nRD	O	MFP7	EBI read enable output pin.
15	22	33	PF.3	I/O	MFP0	General purpose digital I/O pin.
			XT1_OUT	O	MFP1	External 4~24 MHz (high speed) crystal output pin.
			I2C1_SCL	I/O	MFP3	I2C1 clock pin.
16	23	34	PF.4	I/O	MFP0	General purpose digital I/O pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
			XT1_IN	I	MFP1	External 4~24 MHz (high speed) crystal input pin.
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
17	24	35	V_{SS}	P	MFP0	Ground pin for digital circuit.
	25	36	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
18	26	37	LDO_CAP	A	MFP0	LDO output pin.
		38	PC.9	I/O	MFP0	General purpose digital I/O pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			I2C1_SCL	I/O	MFP3	I2C1 clock pin.
			USCI2_CTL1	I/O	MFP4	USCI2 control 1 pin.
			PWM1_CH0	I/O	MFP6	PWM1 channel 0 output/capture input.
		39	PC.10	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI	I/O	MFP2	SPI0 MOSI (Master Out, Slave In) pin.
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
			USCI2_DAT1	I/O	MFP4	USCI2 data 1 pin.
			PWM1_CH1	I/O	MFP6	PWM1 channel 1 output/capture input.
		40	PC.11	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			USCI2_CLK	I/O	MFP4	USCI2 clock pin.
			PWM1_CH2	I/O	MFP6	PWM1 channel 2 output/capture input.
		41	PC.12	I/O	MFP0	General purpose digital I/O pin.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			USCI2_CTL0	I/O	MFP4	USCI2 control 0 pin.
			PWM1_CH3	I/O	MFP6	PWM1 channel 3 output/capture input.
		42	PC.13	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS	I/O	MFP2	SPI0 slave select pin.
			USCI2_DAT0	I/O	MFP4	USCI2 data 0 pin.
			PWM1_CH4	I/O	MFP6	PWM1 channel 4 output/capture input.
		43	PC.14	I/O	MFP0	General purpose digital I/O pin.
			PWM1_CH5	I/O	MFP6	PWM1 channel 5 output/capture input.
19	27	44	PC.0	I/O	MFP0	General purpose digital I/O pin.
			SC0_DAT	I/O	MFP1	Smart Card 0 data pin.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			UART2_nCTS	I	MFP3	UART2 clear to Send input pin.

Group	Pin Name	GPIO	MFP*	Type	Description
	PWM0_CH4	PC.4	MFP6	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	PD.6	MFP6	I/O	PWM0 channel 5 output/capture input.
		PD.7	MFP6	I/O	
		PC.5	MFP6	I/O	
	PWM0_SYNC_IN	PD.1	MFP2	I	PWM0 counter synchronous trigger input pin.
		PD.7	MFP3	I	
	PWM0_SYNC_OUT	PB.1	MFP6	O	PWM0 counter synchronous trigger output pin.
PWM1	PWM1_BRAKE0	PF.1	MFP6	I	PWM1 Brake 0 input pin.
		PE.4	MFP6	I	
	PWM1_BRAKE1	PF.2	MFP6	I	PWM1 Brake 1 input pin.
		PE.5	MFP6	I	
		PA.9	MFP7	I	
	PWM1_CH0	PD.12	MFP6	I/O	PWM1 channel 0 output/capture input.
		PC.9	MFP6	I/O	
		PC.6	MFP6	I/O	
	PWM1_CH1	PD.13	MFP6	I/O	PWM1 channel 1 output/capture input.
		PC.10	MFP6	I/O	
		PC.7	MFP6	I/O	
		PB.12	MFP6	I/O	
	PWM1_CH2	PD.14	MFP6	I/O	PWM1 channel 2 output/capture input.
		PC.11	MFP6	I/O	
		PA.3	MFP6	I/O	
	PWM1_CH3	PD.15	MFP6	I/O	PWM1 channel 3 output/capture input.
		PC.12	MFP6	I/O	
		PA.2	MFP6	I/O	
	PWM1_CH4	PC.13	MFP6	I/O	PWM1 channel 4 output/capture input.
		PA.1	MFP6	I/O	
	PWM1_CH5	PC.14	MFP6	I/O	PWM1 channel 5 output/capture input.
		PA.0	MFP6	I/O	
SC0	SC0_CLK	PC.1	MFP2	O	Smart Card 0 clock pin.
		PE.11	MFP5	O	
		PA.0	MFP5	O	
	SC0_DAT	PC.0	MFP1	I/O	Smart Card 0 data pin.
		PE.10	MFP5	I/O	

Group	Pin Name	GPIO	MFP*	Type	Description
		PD.9	MFP4	I/O	
		PF.1	MFP5	I/O	
		PC.12	MFP4	I/O	
	USCI2_CTL1	PB.7	MFP4	I/O	USCI2 control 1 pin.
		PD.8	MFP4	I/O	
		PF.0	MFP5	I/O	
		PC.9	MFP4	I/O	
	USCI2_DAT0	PD.2	MFP4	I/O	USCI2 data 0 pin.
		PD.10	MFP5	I/O	
		PC.13	MFP4	I/O	
	USCI2_DAT1	PD.3	MFP4	I/O	USCI2 data 1 pin.
		PD.11	MFP5	I/O	
		PC.10	MFP4	I/O	
VDET	VDET_P0	PB.0	MFP2	A	Voltage detector positive input 0 pin.
	VDET_P1	PB.1	MFP2	A	Voltage detector positive input 1 pin.
X32	X32_IN	PF.1	MFP1	I	External 32.768 kHz crystal input pin.
	X32_OUT	PF.0	MFP1	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PF.4	MFP1	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	PF.3	MFP1	O	External 4~24 MHz (high speed) crystal output pin.

Table 4.3-1 NUC126 GPIO Multi-function Table

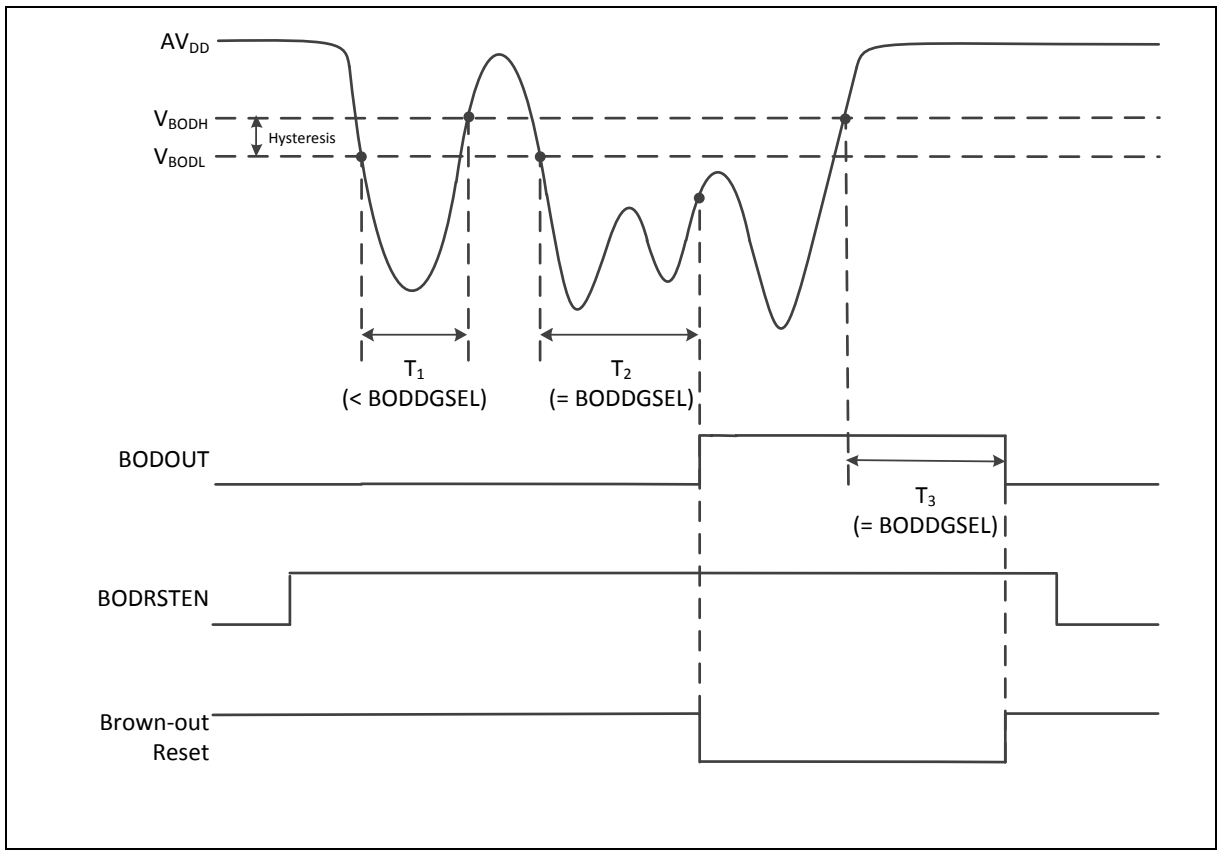


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

6.2.5 System Memory Map

The NUC126 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-5. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NUC126 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 KB)
0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256 KB)
0x0004_0000 – 0x0005_FFFF	Reserved	Reserved
0x0006_0000 – 0x0007_FFFF	Reserved	Reserved
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20 KB)
0x2000_4000 – 0x2000_BFFF	Reserved	Reserved
0x2000_C000 – 0x2000_FFFF	Reserved	Reserved
0x6000_0000 – 0x601F_FFFF	EXTMEM_BA	External Memory Space for EBI Interface (2 MB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	EBI Control Registers
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware Divider Registers
0x5001_8000 – 0x5001_FFFF	CRC_BA	CRC Generator Registers
Peripheral Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	Reserved	Reserved
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x4007_0000 – 0x4007_3FFF	USCI0_BA	USCI0 Control Registers

according to the accurate external 32.768 kHz crystal oscillator or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 22.1184 MHz clock. In such case, if users do not want to use PLL as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL0[1:0] trim frequency selection) to “01”, set REFCKSEL (SYS_IRCTCTL0[9] reference clock selection) to “0”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) “1” indicates the HIRC0 output frequency is accurate within 0.25% deviation. To get better results, it is recommended to set both LOOPSEL (SYS_IRCTCTL[5:4] trim calculation loop) and RETRYCNT (SYS_IRCTCTL[7:6] trim value update limitation count) to “11”.

Another example is that the system needs an accurate 48 MHz clock for USB application. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL1[10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL1[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK1 (SYS_IRCTISTS[8] HIRC frequency lock status) “1” indicates the HIRC1 output frequency is accurate within 0.25% deviation.

6.2.9 UART1_TXD modulation with PWM

This chip supports UART1_TXD to modulate with PWM channel. User can set MODPWMSEL(SYS_MODCTL[6:4]) to choice which PWM0 channel to modulate with UART1_TXD and set MODEN(SYS_MODCTL[0]) to enable modulation function. User can set TXDINV(UART_LINE[8]) to inverse UART1_TXD before moulating with PWM.

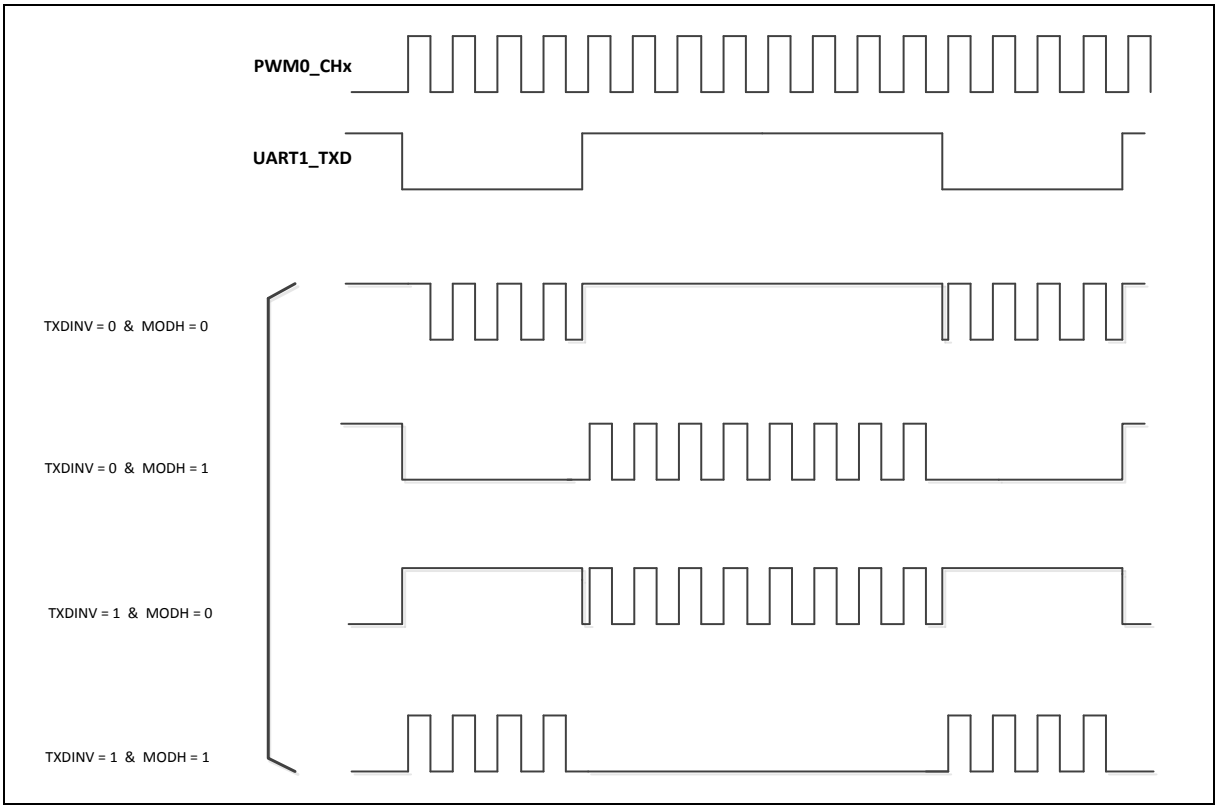


Figure 6.2-10 UART1_TXD Modulated with PWM Channel

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M0 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT), internal 22.1184 MHz internal high speed RC oscillator (HIRC) and 48 MHz internal high speed RC oscillator (HIRC48) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

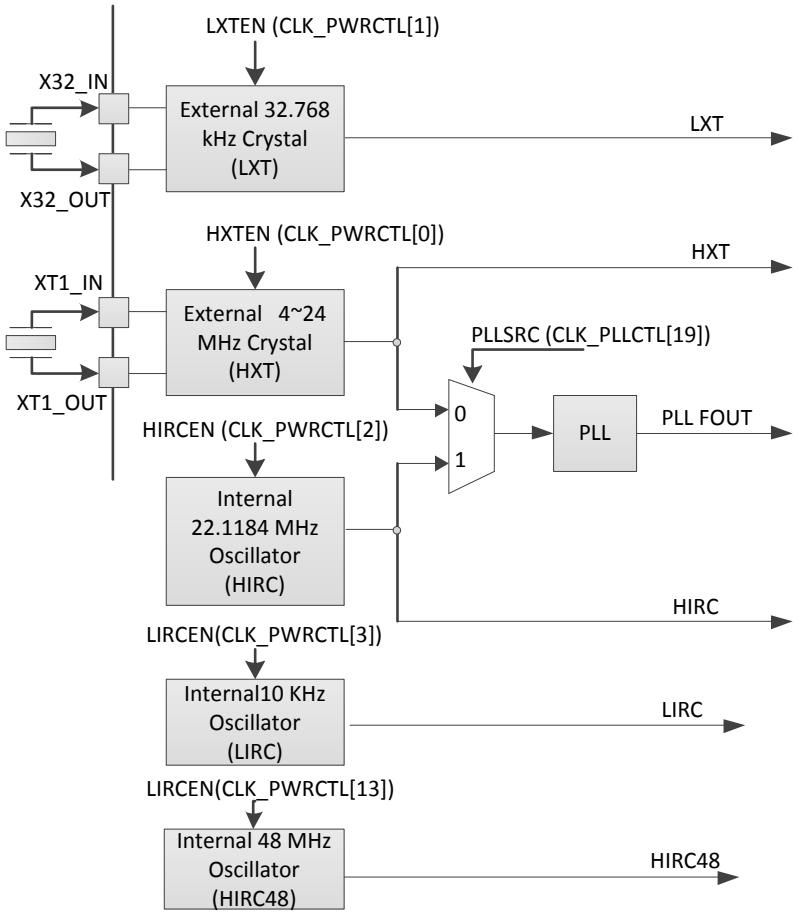
The clock generator consists of 6 clock sources, which are listed below:

- 32.768 kHz external low-speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 48 MHz internal high speed RC oscillator (HIRC48)
- 10 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index (HIRCSTB(CLK_STATUS[4]), LIRCSTB(CLK_STATUS[3]), PLLSTB(CLK_STATUS[2]), HXTSTB(CLK_STATUS[0]), LXTSTB(CLK_STATUS[1]) and HIRC48STB(CLK_STATUS[5])) are set to 1 after stable counter value reach a define value as shown in Table 6.3-8. System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will auto clear when user disables the clock source (LIRCEN(CLK_PWRCTL[3]), HIRCEN(CLK_PWRCTL[2]), HXTEN(CLK_PWRCTL[0]), PD(CLK_PLLCTL[16]), LXTEN(CLK_PWRCTL[1]) and HIRC48EN(CLK_PWRCTL[13])). Besides, the clock stable index of HXT, HIRC and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value	Clock Stable Time
HXT	4096 HXT clock	341.33 uS for 12 Mhz
PLL	It's based on the value of STBSEL (CLK_PLLCTL[23]) STBSEL = 0, stable count is 6144 clocks of PLL clock source. STBSEL = 1, stable count is 12288 clocks of PLL clock source. (Default)	STBSEL = 0, 512 uS for 512 Mhz STBSEL = 1, 1024 uS for 12 Mhz
HIRC48	512 HIRC48 clock	10.67 uS for 48 Mhz
HIRC	256 HIRC clock	11.574 uS for 22.1184 Mhz
LIRC	1 LIRC clock	100 uS for 10 kHz
LXT	1 LXT clock	30.51 uS for 32.768 khz

Table 6.3-8 Clock Stable Count Value Table



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-1 Clock Generator Block Diagram

6.10 Hardware Divider (HDIV)

6.10.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.10.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Write divisor to trigger calculation
- Waiting for calculation ready automatically when reading quotient and remainder

6.10.3 Blcok Diagram

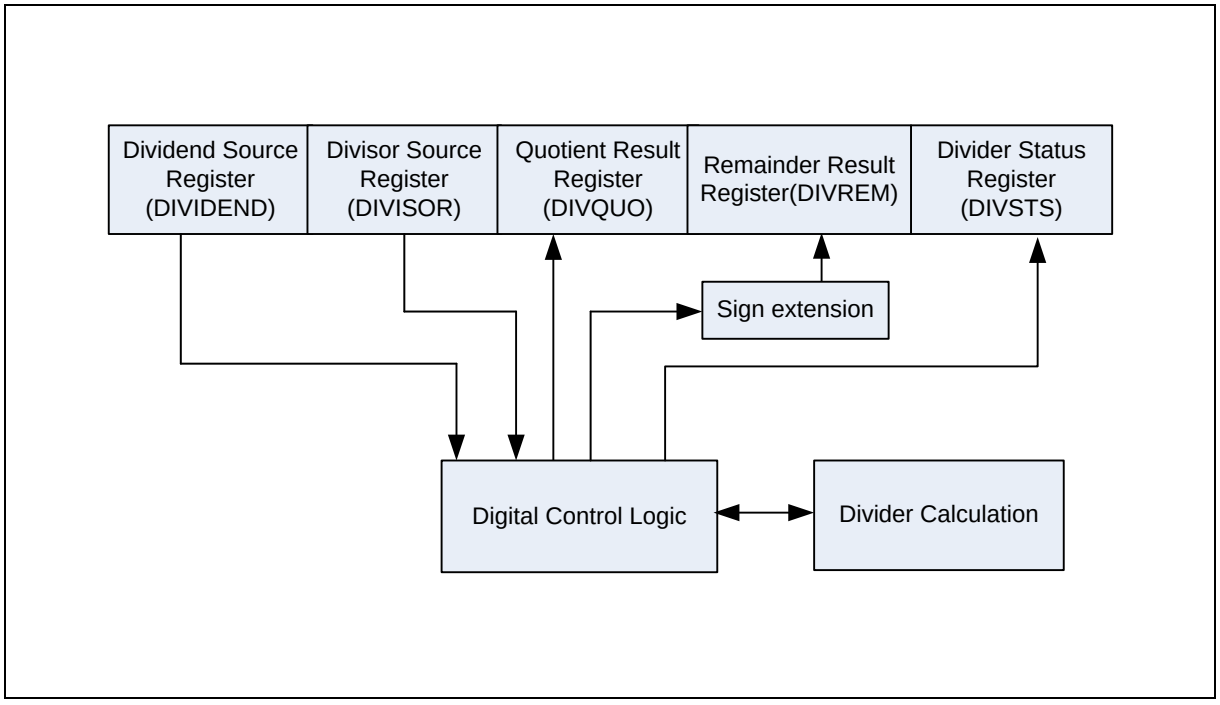


Figure 6.10-1 Hardware Divider Block Diagram

6.13 PWM Generator and Capture Timer (PWM)

6.13.1 Overview

The NUC126 provides two PWM generator: PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various PWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for ADC. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.13.2 Features

6.13.2.1 PWM function features

- Supports maximum clock frequency up to144MHz
- Supports up to two PWM modules, each module provides 6 output channels.
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channels:
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up-down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator, ADC result monitor and system safety events (clock failed, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared

6.19 USCI – Universal Serial Control Interface Controller

6.19.1 Overview

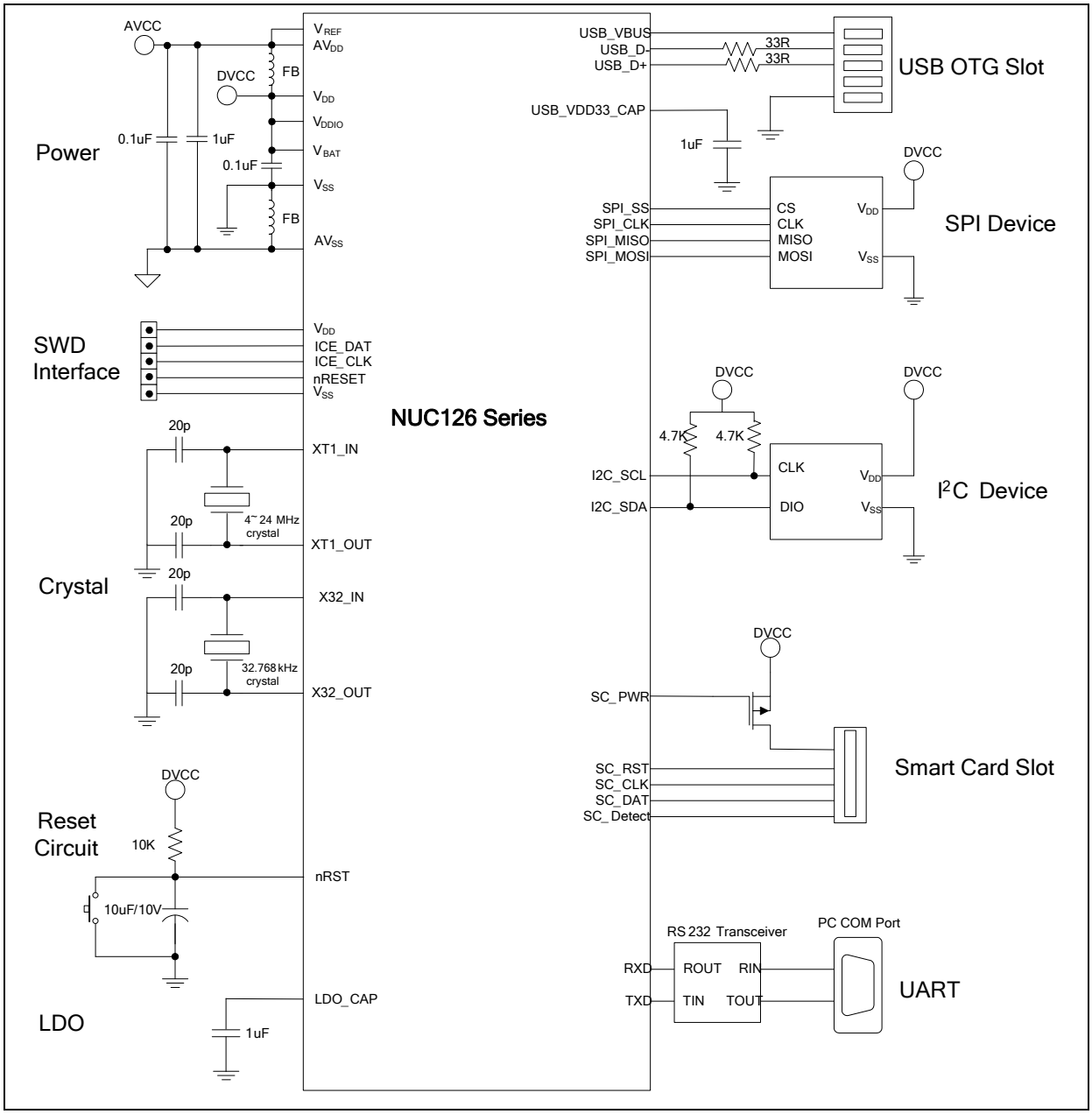
The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.19.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

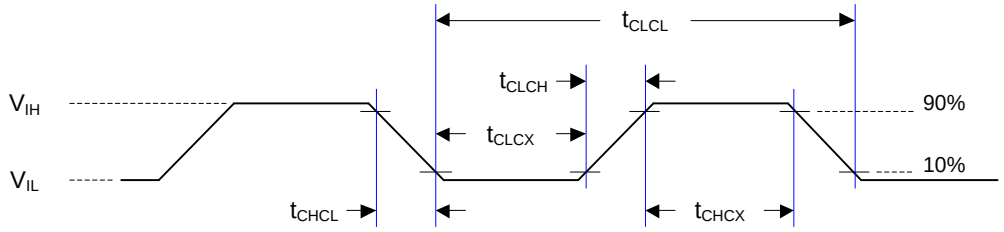
7 APPLICATION CIRCUIT



8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Crystal (HXT) Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	10	-	-	nS	
Clock Low Time	t_{CLCX}	10	-	-	nS	
Clock Rise Time	t_{CLCH}	2	-	15	nS	
Clock Fall Time	t_{CHCL}	2	-	15	nS	
Input High Voltage	V_{IH}	$0.7V_{DD}$	-	V_{DD}	V	
Input Low Voltage	V_{IL}	0	-	$0.3V_{DD}$	V	



Note: Duty cycle is 50%.

8.3.2 External 4~24 MHz High Speed Crystal (HXT) Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{HXT}	4	-	24	MHz	V_{DD} = 2.5 ~ 5.5V
Temperature	T_{HXT}	-40	-	+105	°C	
Operating current	I_{HXT}	-	TBD	-	mA	V_{DD} = 5.5V @ 12MHz
		-	0.4	-	mA	V_{DD} = 3.3V @ 12MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
4MHz ~ 24 MHz	20pF	20pF	without