Nuvoton Technology Corporation - NUC126SG4AE Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVR, PWM, RTC, UCID
Number of I/O	49
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 15x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc126sg4ae

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2 FEATURES

2.1 NuMicro® NUC126 Features

- Core
  - ARM® Cortex®-M0 core running up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports programmable mask-able interrupts
  - Serial Wire Debug supports with 2 watch-points/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Flash Memory
  - Supports 256/128 KB application ROM (APROM)
  - Supports 4 KB Flash for loader (LDROM)
  - Supports 2 KB Security Protection Rom (SPROM)
  - Supports 12 bytes User Configuration block to control system initiation
  - Supports Data Flash with configurable memory size
  - Supports 2 KB page erase for all embedded flash
  - Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded flash memory
  - Supports CRC-32 checksum calculation function
  - Supports flash all one verification function
  - Hardware external read protection of whole flash memory by Security Lock Bit
  - Supports 2-wired ICP update through SWD/ICE interface
- SRAM Memory
  - 20 KB embedded SRAM
  - Supports byte-, half-word- and word-access
  - Supports PDMA mode
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Write divisor to trigger calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- PDMA (Peripheral DMA)
  - Supports 5 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports single and burst transfer type
  - Supports Normal and Scatter-Gather Transfer modes
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Supports incrementing mode for the source and destination address for each channel
  - Supports time-out function for channel 0 and channel 1
  - Supports software and SPI/I2S, UART, USCI, USB, ADC, PWM and TIMER request
- Clock Control

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4.1.2 NuMicro® NUC126 USB Series (M452 Compatible) Selection Guide

Part Number	Flash (KB)	SRAM (KB)	Data Flash(KB)	SPROM(KB)	ISP ROM (KB)	I/O	Timer/PWM	PWM		Connectivity					ADC(12-Bit)	ACMP	PDMA	VBAT(RTC)	LVIO	EBI	ICP/IAP/ISP	Package
									USBD	USCI*	UART	SC/UART	SPI/I²S	I²C								
NUC126LE4AE	128	20	Conf*	2	4	35	4	10	1	3	3	2	2	2	9-ch	2	5	--	√	√	√	LQFP 48
NUC126LG4AE	256	20	Conf*	2	4	35	4	10	1	3	3	2	2	2	9-ch	2	5	--	√	√	√	LQFP 48
NUC126SE4AE	128	20	Conf*	2	4	49	4	12	1	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP 64*
NUC126SG4AE	256	20	Conf*	2	4	49	4	12	1	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP 64*
NUC126VG4AE	256	20	Conf*	2	4	81	4	12	1	3	3	2	2	2	20-ch	2	5	√	√	√	√	LQFP 100

Conf*: Configurable
USCI*: support UART, SPI or I²C
LQFP64*: 7x7 mm

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
			ACMP0_P0	A	MFP5	Analog comparator 0 positive input 0 pin.
			SC1_DAT	I/O	MFP6	Smart Card 1 data pin.
			EBI_AD4	I/O	MFP7	EBI address/data bus bit 4.
4	5	7	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
5	6	8	PD.0	I/O	MFP0	General purpose digital I/O pin.
			SPI0_I2SMCLK	I/O	MFP1	SPI0 I2S master clock output pin
			SPI1_I2SMCLK	I/O	MFP2	SPI1 I2S master clock output pin
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			USCI2_CTL0	I/O	MFP4	USCI2 control 0 pin.
			ACMP1_N	A	MFP5	Analog comparator 1 negative input pin.
			SC1_CLK	O	MFP6	Smart Card 1 clock pin.
			INT3	I	MFP8	External interrupt 3 input pin.
6	7	9	AV_{SS}	P	MFP0	Ground pin for analog circuit.
		10	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
		11	V_{SS}	P	MFP0	Ground pin for digital circuit.
		12	PC.8	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH16	A	MFP1	ADC0 channel 16 analog input.
			UART0_nRTS	O	MFP3	UART0 request to Send output pin.
	8	13	PD.8	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH17	A	MFP1	ADC0 channel 17 analog input.
			UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
			USCI2_CTL1	I/O	MFP4	USCI2 control 1 pin.
			TM2	I/O	MFP6	Timer2 event counter input/toggle output pin.
			EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
	9	14	PD.9	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH18	A	MFP1	ADC0 channel 18 analog input.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			USCI2_CTL0	I/O	MFP4	USCI2 control 0 pin.
			ACMP1_P3	A	MFP5	Analog comparator 1 positive input 3 pin.
			TM3	I/O	MFP6	Timer3 event counter input/toggle output pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
7	10	15	PD.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH19	A	MFP1	ADC0 channel 19 analog input.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
			PWM0_SYNC_IN	I	MFP2	PWM0 counter synchronous trigger input pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
			USCI2_CLK	I/O	MFP4	USCI2 clock pin.
			ACMP1_P2	A	MFP5	Analog comparator 1 positive input 2 pin.
			TM0	I/O	MFP6	Timer0 event counter input/toggle output pin.
			EBI_nRD	O	MFP7	EBI read enable output pin.
8	11	16	PD.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_ST	I	MFP1	ADC0 external trigger input pin.
			TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin.
			USCI2_DAT0	I/O	MFP4	USCI2 data 0 pin.
			ACMP1_P1	A	MFP5	Analog comparator 1 positive input 1 pin.
			PWM0_BRAKE0	I	MFP6	PWM0 Brake 0 input pin.
			EBI_nWR	O	MFP7	EBI write enable output pin.
			INT0	I	MFP8	External interrupt 0 input pin.
9	12	17	PD.3	I/O	MFP0	General purpose digital I/O pin.
			TM2	I/O	MFP1	Timer2 event counter input/toggle output pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
			USCI2_DAT1	I/O	MFP4	USCI2 data 1 pin.
			ACMP1_P0	A	MFP5	Analog comparator 1 positive input 0 pin.
			PWM0_BRAKE1	I	MFP6	PWM0 Brake 1 input pin.
			EBI_MCLK	O	MFP7	EBI external clock output pin.
			INT1	I	MFP8	External interrupt 1 input pin.
		18	PD.4	I/O	MFP0	General purpose digital I/O pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
			UART2_nRTS	O	MFP4	UART2 request to Send output pin.
			PWM0_BRAKE0	I	MFP5	PWM0 Brake 0 input pin.
			TM0	I/O	MFP6	Timer0 event counter input/toggle output pin.
		19	PD.5	I/O	MFP0	General purpose digital I/O pin.
			CLKO	O	MFP1	Clock Out
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
			I2C0_SCL	I/O	MFP3	I2C0 clock pin.
			UART2_nCTS	I	MFP4	UART2 clear to Send input pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
			USCI0_CLK	I/O	MFP4	USCI0 clock pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
			PWM1_BRAKE1	I	MFP6	PWM1 Brake 1 input pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
			INT1	I	MFP8	External interrupt 1 input pin.
25	35	55	PE.6	I/O	MFP0	General purpose digital I/O pin.
			ICE_CLK	I	MFP1	Serial wired debugger clock pin.
			I2C0_SCL	I/O	MFP2	I2C0 clock pin.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
26	36	56	PE.7	I/O	MFP0	General purpose digital I/O pin.
			ICE_DAT	O	MFP1	Serial wired debugger data pin.
			I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
		57	PA.8	I/O	MFP0	General purpose digital I/O pin.
			CLKO	O	MFP1	Clock Out
			I2C1_SCL	I/O	MFP2	I2C1 clock pin.
			UART1_TXD	O	MFP3	UART1 data transmitter output pin.
			SC0_PWR	O	MFP4	Smart Card 0 power pin.
			SC1_RST	O	MFP5	Smart Card 1 reset pin.
			TM_BRAKE0	I	MFP6	Timer Brake 0 input pin.
			PWM0_BRAKE0	I	MFP7	PWM0 Brake 0 input pin.
			TM1	I/O	MFP8	Timer1 event counter input/toggle output pin.
		58	PA.9	I/O	MFP0	General purpose digital I/O pin.
			SPI1_I2SMCLK	I/O	MFP1	SPI1 I2S master clock output pin
			I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
			UART1_RXD	I	MFP3	UART1 data receiver input pin.
			SC0_RST	O	MFP4	Smart Card 0 reset pin.
			SC1_PWR	O	MFP5	Smart Card 1 power pin.
			TM_BRAKE1	I	MFP6	Timer Brake 1 input pin.
			PWM1_BRAKE1	I	MFP7	PWM1 Brake 1 input pin.
			TM2	I/O	MFP8	Timer2 event counter input/toggle output pin.
		59	PA.7	I/O	MFP0	General purpose digital I/O pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP*	Description
45	58	92	PB.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
			VDET_P1	A	MFP2	Voltage detector positive input 1 pin.
			UART2_TXD	O	MFP3	UART2 data transmitter output pin.
			TM3	I/O	MFP4	Timer3 event counter input/toggle output pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
			PWM0_SYNC_OUT	O	MFP6	PWM0 counter synchronous trigger output pin.
			EBI_nWRH	O	MFP7	EBI high byte write enable output pin
			USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
46	59	93	PB.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
			UART1_RXD	I	MFP4	UART1 data receiver input pin.
			SC0_nCD	I	MFP5	Smart Card 0 card detect pin.
			TM_BRAKE0	I	MFP6	Timer Brake 0 input pin.
			EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
			USCI0_DAT0	I/O	MFP8	USCI0 data 0 pin.
			TM2_EXT	I/O	MFP10	Timer2 external capture input/toggle output pin.
47	60	94	PB.3	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
			UART1_TXD	O	MFP4	UART1 data transmitter output pin.
			TM_BRAKE1	I	MFP6	Timer Brake 1 input pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
			USCI0_DAT1	I/O	MFP8	USCI0 data 1 pin.
			TM0_EXT	I/O	MFP10	Timer0 external capture input/toggle output pin.
48	61	95	PB.4	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
			SPI0_SS	I/O	MFP2	SPI0 slave select pin.
			SPI1_SS	I/O	MFP3	SPI1 slave select pin.
			UART1_nCTS	I	MFP4	UART1 clear to Send input pin.
			ACMP0_N	A	MFP5	Analog comparator 0 negative input pin.

4.3.2 GPIO Multi-function Pin Summary

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GP0_MFPL[3:0]=0x0.

PA.9 MFP5 means SYS_GP0_MFPH[7:4]=0x5.

Group	Pin Name	GPIO	MFP*	Type	Description
ACMP0	ACMP0_N	PB.4	MFP5	A	Analog comparator 0 negative input pin.
	ACMP0_O	PD.6	MFP5	O	Analog comparator 0 output pin.
		PD.7	MFP5	O	
	ACMP0_P0	PB.7	MFP5	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	PB.6	MFP5	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	PB.5	MFP5	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	PB.15	MFP5	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	PC.0	MFP5	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	PD.0	MFP5	A	Analog comparator 1 negative input pin.
	ACMP1_O	PC.2	MFP5	O	Analog comparator 1 output pin.
		PC.6	MFP5	O	
	ACMP1_P0	PD.3	MFP5	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	PD.2	MFP5	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	PD.1	MFP5	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	PD.9	MFP5	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	PC.1	MFP5	I	Analog comparator 1 window latch input pin
ADC0	ADC0_CH0	PB.0	MFP1	A	ADC0 channel 0 analog input.
	ADC0_CH1	PB.1	MFP1	A	ADC0 channel 1 analog input.
	ADC0_CH2	PB.2	MFP1	A	ADC0 channel 2 analog input.
	ADC0_CH3	PB.3	MFP1	A	ADC0 channel 3 analog input.
	ADC0_CH4	PB.4	MFP1	A	ADC0 channel 4 analog input.
	ADC0_CH5	PB.8	MFP1	A	ADC0 channel 5 analog input.
	ADC0_CH6	PB.9	MFP1	A	ADC0 channel 6 analog input.
	ADC0_CH7	PB.10	MFP1	A	ADC0 channel 7 analog input.
	ADC0_CH8	PB.11	MFP1	A	ADC0 channel 8 analog input.
	ADC0_CH9	PE.2	MFP1	A	ADC0 channel 9 analog input.
	ADC0_CH10	PB.13	MFP1	A	ADC0 channel 10 analog input.
	ADC0_CH11	PB.14	MFP1	A	ADC0 channel 11 analog input.
	ADC0_CH12	PB.15	MFP1	A	ADC0 channel 12 analog input.
	ADC0_CH13	PB.5	MFP1	A	ADC0 channel 13 analog input.
	ADC0_CH14	PB.6	MFP1	A	ADC0 channel 14 analog input.

Group	Pin Name	GPIO	MFP*	Type	Description
	PWM0_CH4	PC.4	MFP6	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	PD.6	MFP6	I/O	PWM0 channel 5 output/capture input.
		PD.7	MFP6	I/O	
		PC.5	MFP6	I/O	
	PWM0_SYNC_IN	PD.1	MFP2	I	PWM0 counter synchronous trigger input pin.
		PD.7	MFP3	I	
	PWM0_SYNC_OUT	PB.1	MFP6	O	PWM0 counter synchronous trigger output pin.
PWM1	PWM1_BRAKE0	PF.1	MFP6	I	PWM1 Brake 0 input pin.
		PE.4	MFP6	I	
	PWM1_BRAKE1	PF.2	MFP6	I	PWM1 Brake 1 input pin.
		PE.5	MFP6	I	
		PA.9	MFP7	I	
	PWM1_CH0	PD.12	MFP6	I/O	PWM1 channel 0 output/capture input.
		PC.9	MFP6	I/O	
		PC.6	MFP6	I/O	
	PWM1_CH1	PD.13	MFP6	I/O	PWM1 channel 1 output/capture input.
		PC.10	MFP6	I/O	
		PC.7	MFP6	I/O	
		PB.12	MFP6	I/O	
	PWM1_CH2	PD.14	MFP6	I/O	PWM1 channel 2 output/capture input.
		PC.11	MFP6	I/O	
		PA.3	MFP6	I/O	
	PWM1_CH3	PD.15	MFP6	I/O	PWM1 channel 3 output/capture input.
		PC.12	MFP6	I/O	
		PA.2	MFP6	I/O	
	PWM1_CH4	PC.13	MFP6	I/O	PWM1 channel 4 output/capture input.
		PA.1	MFP6	I/O	
	PWM1_CH5	PC.14	MFP6	I/O	PWM1 channel 5 output/capture input.
		PA.0	MFP6	I/O	
SC0	SC0_CLK	PC.1	MFP2	O	Smart Card 0 clock pin.
		PE.11	MFP5	O	
		PA.0	MFP5	O	
	SC0_DAT	PC.0	MFP1	I/O	Smart Card 0 data pin.
		PE.10	MFP5	I/O	

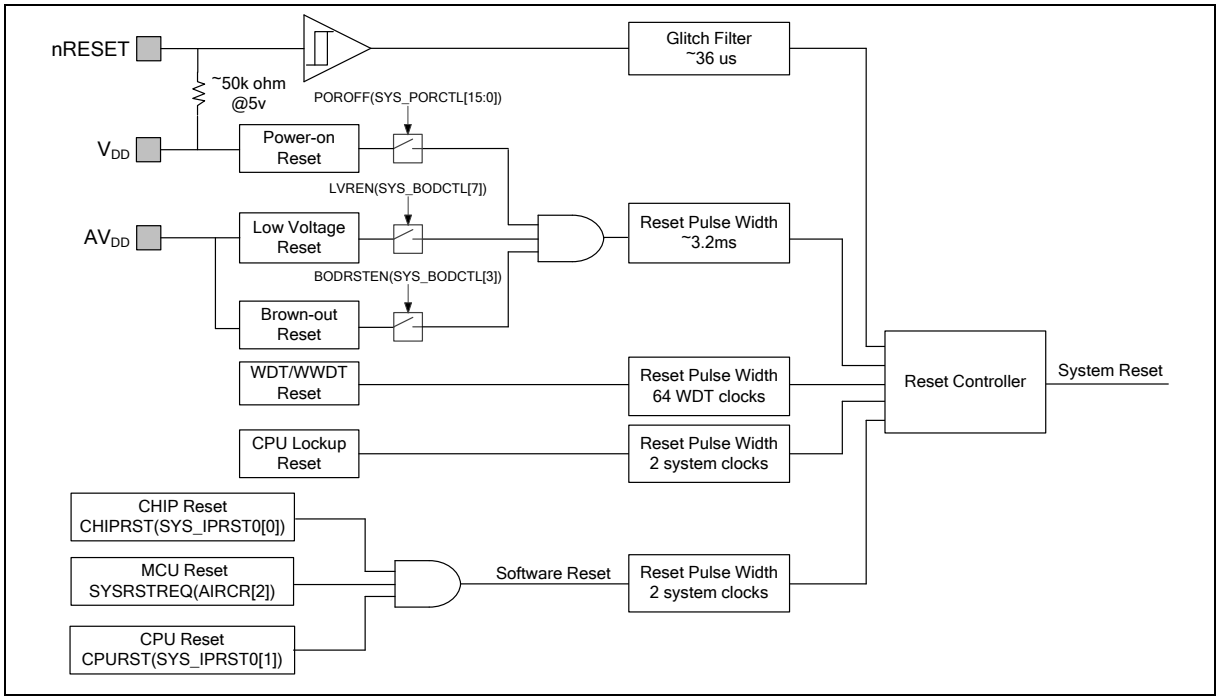

Figure 6.2-1 System Reset Sources

6.2.5 System Memory Map

The NUC126 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-5. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NUC126 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 KB)
0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256 KB)
0x0004_0000 – 0x0005_FFFF	Reserved	Reserved
0x0006_0000 – 0x0007_FFFF	Reserved	Reserved
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20 KB)
0x2000_4000 – 0x2000_BFFF	Reserved	Reserved
0x2000_C000 – 0x2000_FFFF	Reserved	Reserved
0x6000_0000 – 0x601F_FFFF	EXTMEM_BA	External Memory Space for EBI Interface (2 MB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	EBI Control Registers
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware Divider Registers
0x5001_8000 – 0x5001_FFFF	CRC_BA	CRC Generator Registers
Peripheral Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	Reserved	Reserved
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x4007_0000 – 0x4007_3FFF	USCI0_BA	USCI0 Control Registers

6.2.6 SRAM Memory Orginization

The NUC126 supports embedded SRAM with total 20 Kbytes size in one bank.

- Supports total 20 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

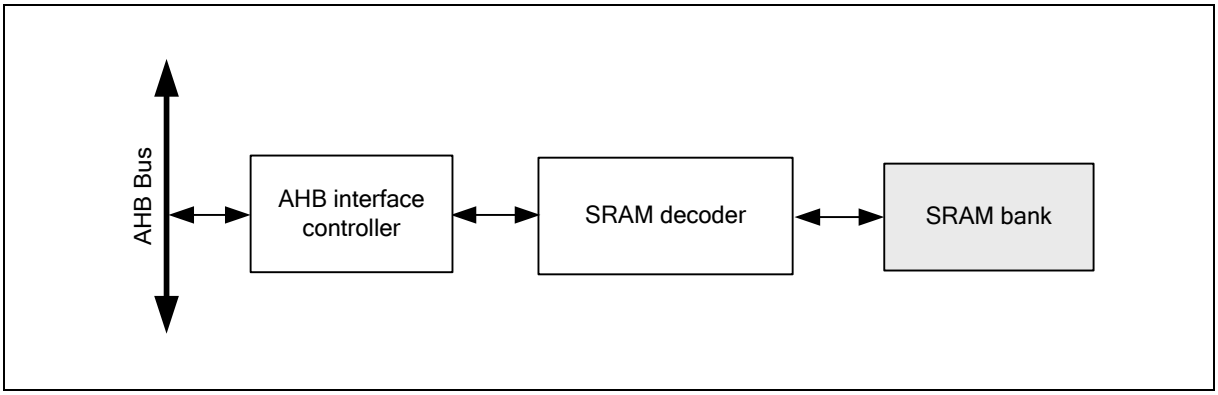

Figure 6.2-8 SRAM Block Diagram

Figure 6.2-9 shows the SRAM organization of NUC126. There is one SRAM bank in the NUC126 and addressed to 20 Kbytes. The address space is from 0x2000_0000 to 0x2000_4FFF. The address between 0x2000_5000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

42	26	PDMA_INT	PDMA interrupt
43	27		Reserved
44	28	PWRWU_INT	Clock controller interrupt for chip wake-up from Power-down state
45	29	ADC_INT	ADC interrupt
46	30	CLKDIRC_INT	Clock fail detect and IRC TRIM interrupt
47	31	RTC_INT	Real Time Clock interrupt

Table 6.2-7 Interrupt Number Table

6.2.12.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.4 Flash Memeory Controller (FMC)

6.4.1 Overview

The NUC126 series is equipped with 128/256 Kbytes on-chip embedded flash for application and configurable Data Flash to store some application dependent data. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 2 Kbytes security protection ROM (SPROM) can conceal user program. A 4KB cache with zero wait cycle is used to improve flash access performance. This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

6.4.2 Features

- Supports 128/256 Kbytes application ROM (APROM).
- Supports 4 Kbytes loader ROM (LDROM).
- Supports 2 Kbytes security protection ROM (SPROM) to conceal user program.
- Supports Data Flash with configurable memory size.
- Supports 12 bytes User Configuration block to control system initiation.
- Supports 2 Kbytes page erase for all embedded flash.
- Supports 32-bit/64-bit and multi-word flash programming function.
- Supports CRC-32 checksum calculation function.
- Supports flash all one verification function.
- Supports embedded SRAM remap to system vector memory.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory.
- Supports cache memory to improve flash access performance and reduce power consumption.

6.10 Hardware Divider (HDIV)

6.10.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.10.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Write divisor to trigger calculation
- Waiting for calculation ready automatically when reading quotient and remainder

6.10.3 Blcok Diagram

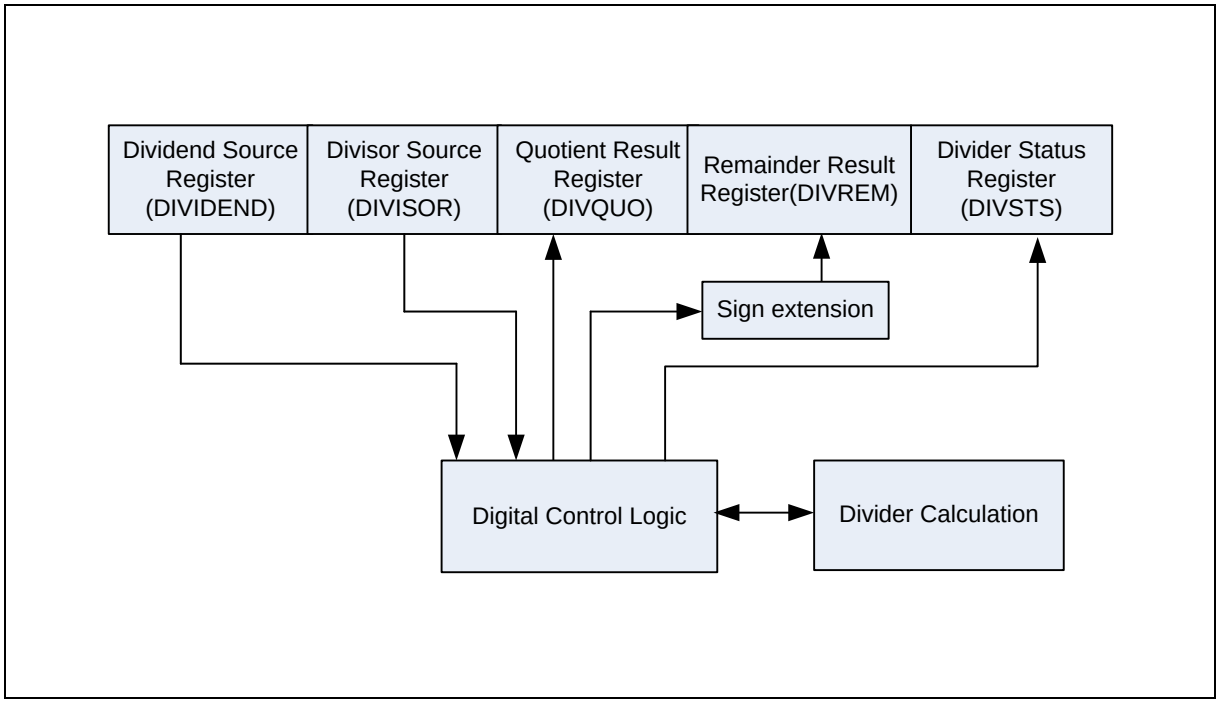

Figure 6.10-1 Hardware Divider Block Diagram

6.15 Smart Card Host Interface (SC)

6.15.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.15.2 Features

- ISO-7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Two ISO-7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the interval between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving/transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SC_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

8.3.4 External 32.768 kHz Low Speed Crystal (LXT) Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}	-	32.768	-	kHz	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V
Temperature	T_{LXT}	-40	-	+105	°C	
Operating current	I_{LXT}		0.7		µA	$V_{DD} = V_{BAT}$ = 2.5 ~ 5.5V

8.3.4.1 Typical Crystal Application Circuits

CRYSTAL	C3	C4	R2
32.768 kHz	20pF	20pF	without

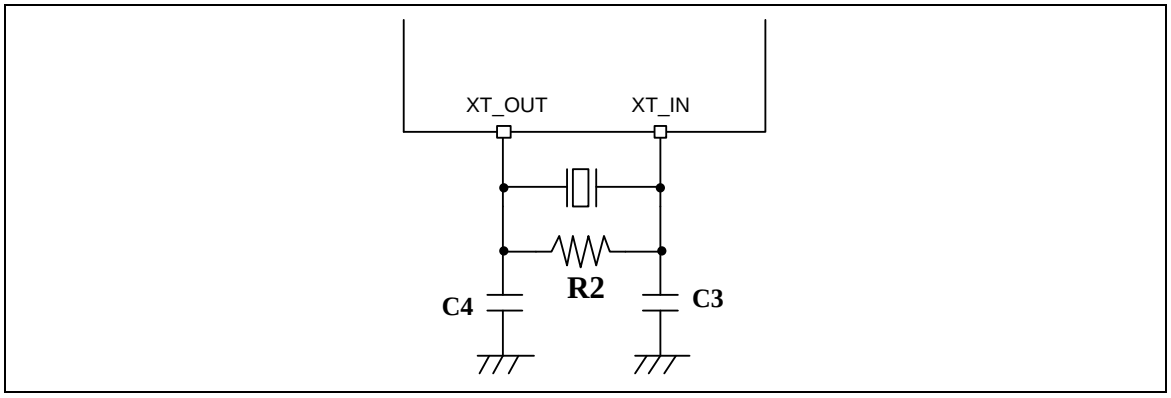

Figure 8.3-2 Typical Crystal Application Circuit

8.4 Analog Characteristics

8.4.1 LDO

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Temperature	T_A	-40	-	+105	°C	
DC Power Supply	V_{DD}	2.5	-	5.5	V	
Output Voltage	V_{LDO}	1.62	1.8	1.98	V	

Note 1: It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

Note 2: For ensuring power stability, a 1μF Capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

8.4.2 Temperature Sensor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Detection Temperature	T_{DET}	-40	-	+105	°C	
Gain	V_{TG}	-1.76	-1.70	-1.64	mV/°C	
Offset	V_{TO}	-	745	-	mV	Temperature at 0 °C
Operating current	I_{TEMP}	6.4	-	10.5	μA	

Note 1: The temperature sensor formula for the output voltage (Vtemp) is as below equation.

Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)

8.4.3 Internal Voltage Reference (Int_V_{REF})

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
V_{REF} (2.048V)	V_{REF1}	1.986	-	2.151	V	VREFCTL = 3, AV_{DD}≥2.5V
V_{REF} (2.56V)	V_{REF2}	2.483	-	2.637	V	VREFCTL = 3, AV_{DD}≥2.9V
V_{REF} (3.072V)	V_{REF3}	2.98	-	3.164	V	VREFCTL = 3, AV_{DD}≥3.4V
V_{REF} (4.096V)	V_{REF4}	3.973	-	4.219	V	VREFCTL = 3, AV_{DD}≥4.5V
Start-up Time	T_{VREF_Start}	-	700	2000	uS	C_{VREF} = 4.7uF
Operating current	I_{VREF}		100		μA	