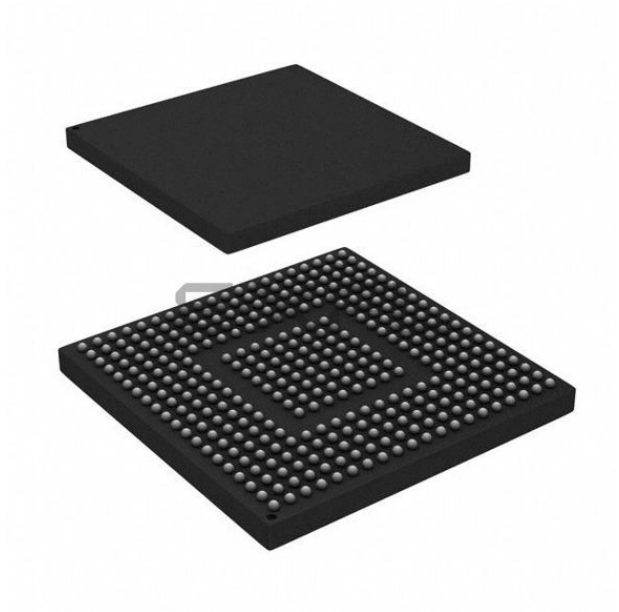

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5 + Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	400MHz, 133MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf532r2k1cmk4r

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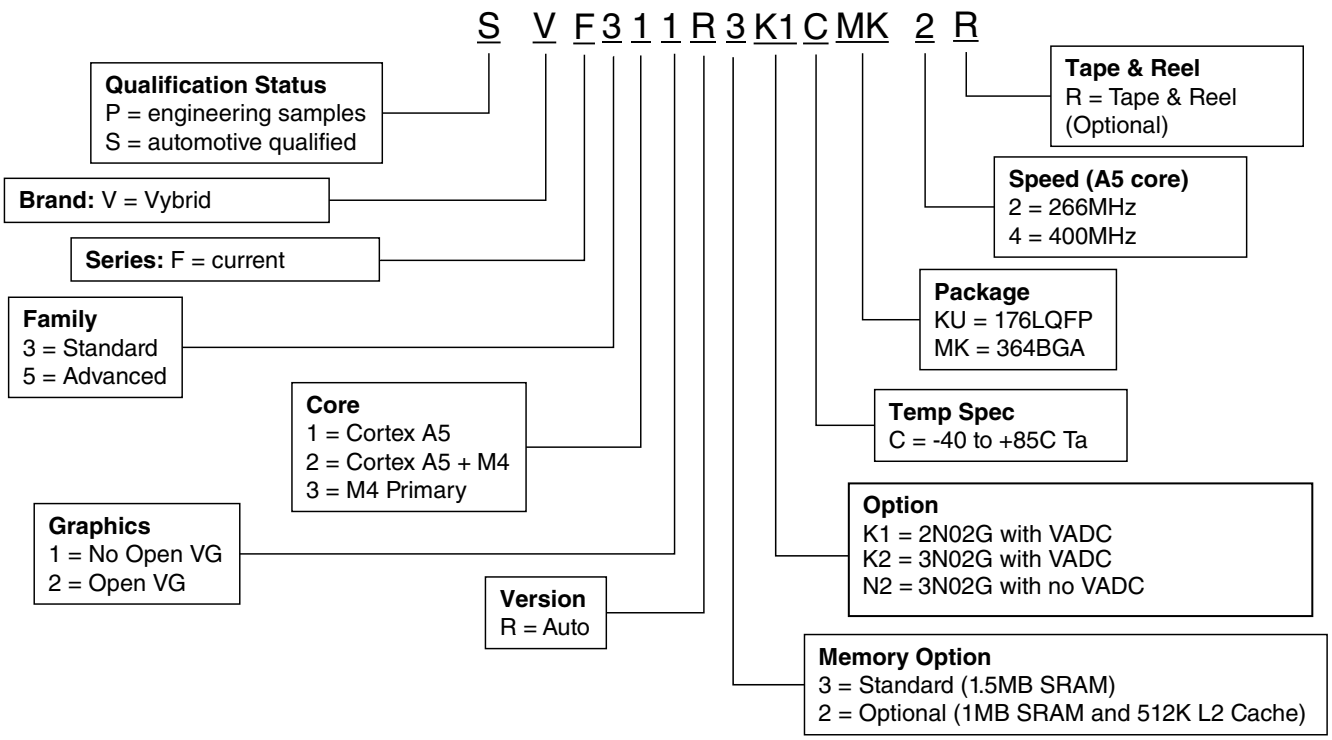


Figure 1. Part Number Format

2.3 Part Numbers

This table lists the part numbers on the device.

Part Number	Mask	VADC	Package	Description
SVF311R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, 176LQFP-EP
SVF312R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, OpenVG GPU, 176LQFP-EP
SVF321R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, M4, 176LQFP-EP
SVF322R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, M4, OpenVG GPU, 176LQFP
SVF331R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, 176LQFP-EP
SVF332R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, OpenVG GPU, 176LQFP-EP
SVF511R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, 364BGA
SVF512R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, OpenVG GPU, 364BGA
SVF521R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4, 364BGA
SVF522R2K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4, L2 Cache, OpenVG GPU, 364BGA
SVF522R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4, OpenVG GPU, 364BG

Table continues on the next page...

Part Number	Mask	VADC	Package	Description
SVF531R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, 364BG
SVF532R2K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, L2 Cache OpenVG GPU, 364BGA
SVF532R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, OpenVG GPU, 364BGA
SVF311R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, 176LQFP-EP
SVF312R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, OpenVG GPU, 176LQFP-EP
SVF321R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, M4, 176LQFP-EP
SVF322R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, M4, OpenVG GPU, 176LQFP
SVF331R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, 176LQFP-EP
SVF332R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, OpenVG GPU, 176LQFP-EP
SVF511R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, 364BGA
SVF512R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, OpenVG GPU, 364BGA
SVF521R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4, 364BGA
SVF522R2N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4, L2 Cache, OpenVG GPU, 364BGA
SVF522R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4, OpenVG GPU, 364BG
SVF531R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, 364BG
SVF532R2N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, L2 Cache OpenVG GPU, 364BGA
SVF532R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, OpenVG GPU, 364BGA

3 Terminology and guidelines

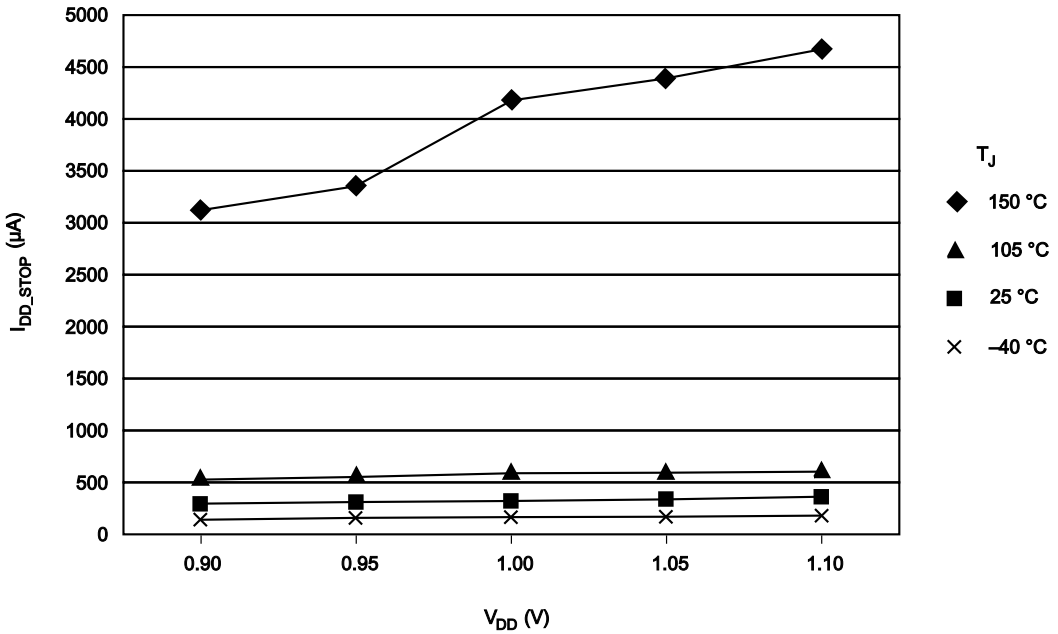
3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Handling ratings

4.1 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
I_{LAT}	Latch-up Current at ambient temperature of 85 °C	-100	100	mA	

1. Determined according to the AEC spec AEC-Q100-002 for HBM
2. Determined according to AEC spec AEC-Q100-011

Table 24. LPDDR2 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.9*ovdd			V	Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.
Vol	Low-level output voltage				0.1*ovdd	V	
Vref	Input reference voltage		0.49*ovdd	0.5*ovdd	0.51*ovdd	V	
Vih(dc)	DC input high voltage		Vref+0.13		ovdd	V	
Vil(dc)	DC input low voltage		ovss		Vref-0.13	V	
Vih(diff)	DC differential input logic high		0.26		Note[1]	V	
Vil(diff)	DC differential input logic low		Note[1]		-0.26	V	
Iin[2]	Input current (no pull-up/ down)	Vin = ovdd or 0			2.5	uA	
Tri-state I/O supply current[2]	Icc-ovdd	Vin = ovdd or 0			4		
Tri-state vdd2p5 supply current[2]	Icc-vdd2p5	Vi = vddi or 0			1.5		
Tri-state core supply current[2]	Icc-vddi				1		
Driver unit (240 Ohm) calibration resolution	Rres				10	Ohm	

1. The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.
2. Typ condition: typ model, 1.2 V, and 25 °C junction. Max condition: bcs model, 1.26V, and -40 °C. Min condition: wcs model, 1.14V, and Tj 125 °C.

Table 25. DDR3 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.8*ovdd			V	Note that the JEDEC JESD79_3E specification supersedes any
Vol	Low-level output voltage	Iol= 1mA			0.2*ovdd	V	

Table continues on the next page...

Table 30. Recommended operating conditions (continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VSSA33_AFE	Ground supply of AFE (Video ADC)			0		V
VSS12_AFE	Ground supply for AFE (Video ADC)			0		V
SDRAMC_VDD1P5	LPDDR2	External CAP 10uF	1.142	1.2	1.26	V
SDRAMC_VDD1P5	DDR3	External CAP 10uF	1.425	1.5	1.575	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	External CAP 10uF	2.25	2.5	2.75	V
-	Maximum power supply ramp rate (Slew limit for power-up)		-		0.1	V/us

1. For customer applications, this is governed by ballast output which is controlled by the device and appropriate voltage ranges are maintained.

8.5 Recommended Connections for Unused Analog Interfaces

NOTE

There are two options to handle unused power pins:

1. Connect all unused supplies to their respective voltage. To save the power, do not enable the module and/or do not enable clock gate to the module.
2. Keep all unused supplies floating.

If pin is shared by several peripheral, then all peripherals connected to multiplexer have to be powered. For example: if pin is shared by GPIO and ADC input and GPIO functionality is used, then ADC has to be powered due to internal structure of the multiplexer. Keep unused input signals grounded if power pins are powered. Keep unused input signals floating if power pins are floating. Keep unused output signals floating.

Module	Name	Recommendation if Unused
ADC	VDDA33_ADC	3.3V or float (Note: Powers both ADC and DAC)
	VREFH_ADC, VREFL_ADC	VREFH_ADC same as VDDA33_ADC VREFL_ADC ground or float
	ADC0SE8, ADC0SE9, ADC1SE8, ADC1SE9	Ground or float
CCM	LVDS0P, LVDS0N	Float
DAC	DACO0, DACO1	Float

Table continues on the next page...

3. 1 LSB = (V_{REFH} - V_{REFL})/2N

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

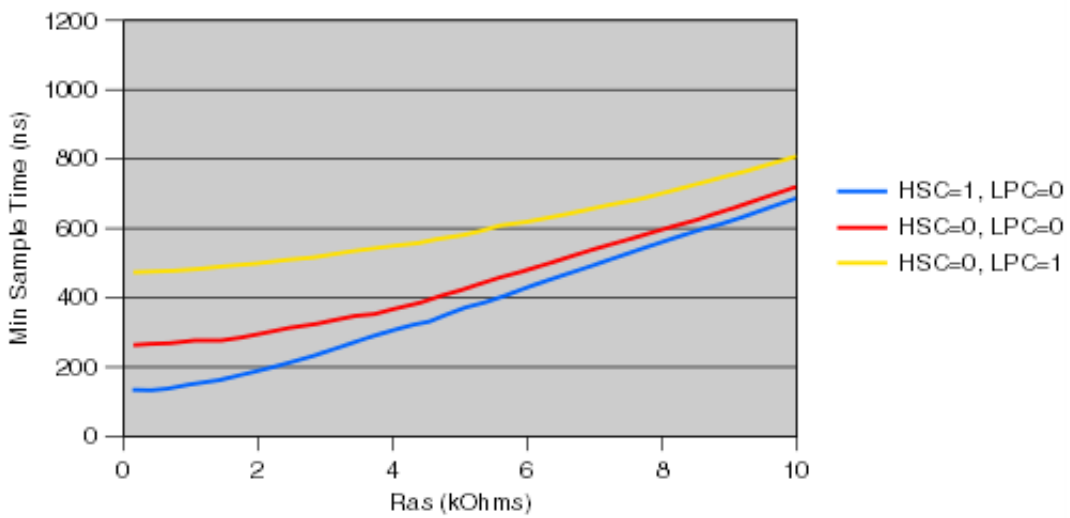


Figure 6. Minimum Sample Time Vs Ras (Cas = 2pF)

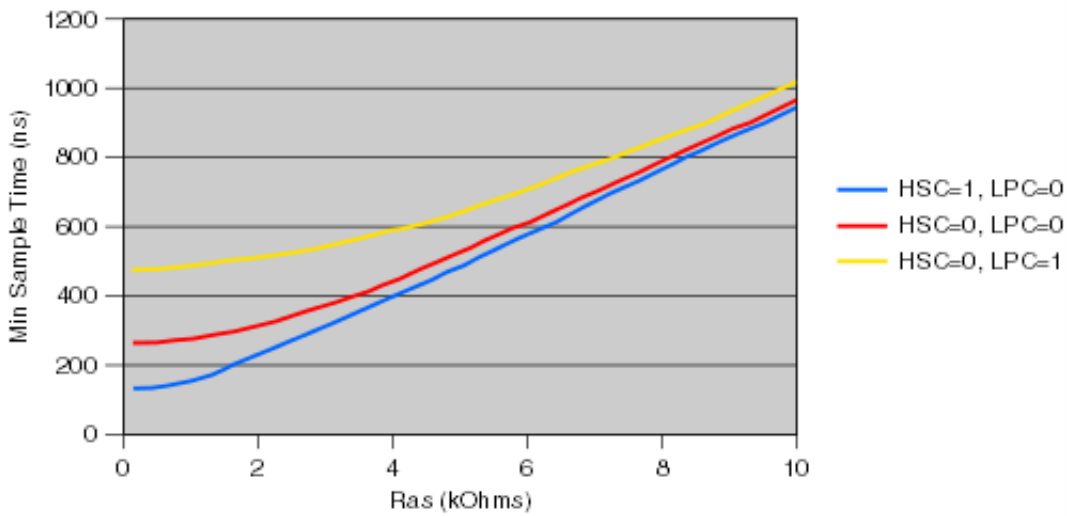


Figure 7. Minimum Sample Time Vs Ras (Cas = 5pF)

2. Intra bit skew is less than 2 ns
3. Load CL = 50 pf

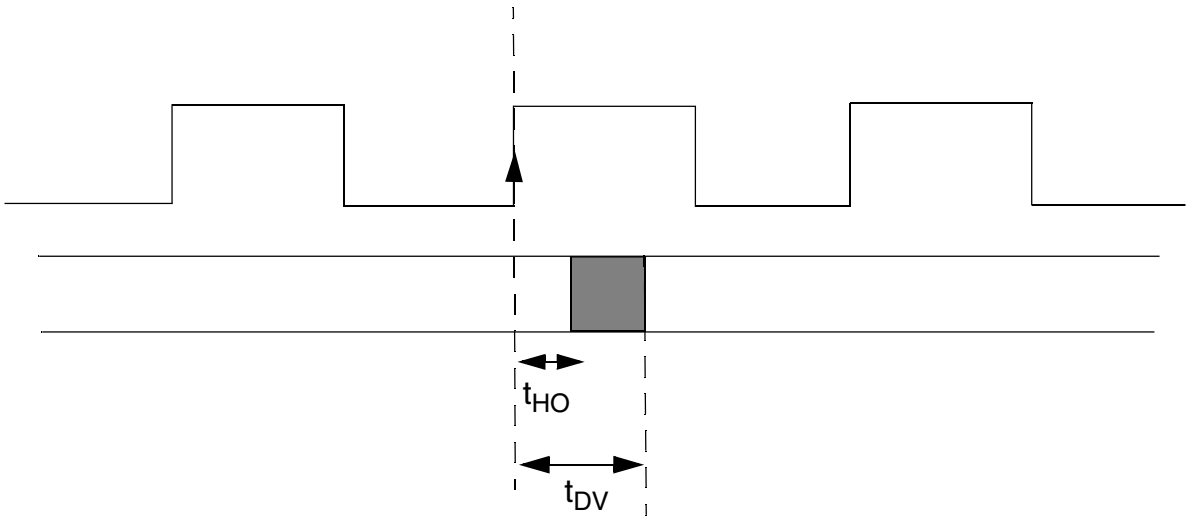


Figure 17. LCD Interface Timing Parameters—Access Level

9.2.2 Video Input Unit timing

This section provides the timing parameters of the Video Input Unit (VIU) interface.

These are the clocking requirements of the VIU interface:

- The platform bus clock must be 2.5x pixel clock
- If the VIU3 does 2x horizontal upscaling, the ratio must be 3x

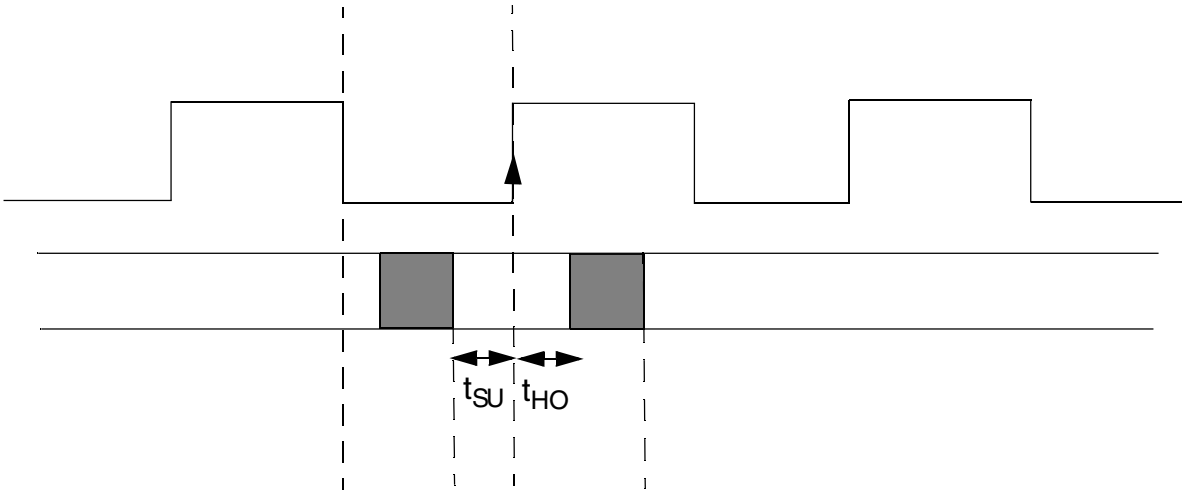


Figure 18. VIU Timing Parameters

Table 38. VIU Timing Parameters

Symbol	Characteristic	Min Value	Max Value	Unit
f_{PIX_CK}	VIU pixel clock frequency	_	64	MHz
t_{DSU}	VIU data setup time	4	_	ns
t_{DHD}	VIU data hold time	1	_	ns

9.2.3 LCD driver electrical characteristics

This section provides LCD driver electrical specification at V_{DD33} = 3.3 V ± 10%.

Table 39. LCD driver specifications

Symbol	Parameter	Min	Typical	Max	Unit
VLCD	Voltage on VLCD (LCD supply) pin with respect to VSS	0		VDD33 + 0.3	V
$Z_{BP/FP}$	LCD output impedance (BP[n-1:0],FP[m-1:0]) for output levels VDDE, VSS	_	_	5.0	KΩ
$I_{BP/FP}$	LCD output current (BP[n-1:0],FP[m-1:0]) for outputs charge/discharge voltage levels VDDE2/3, VDDE1/2, VDDE/3)[1]	_	25	_	µA

1. With PWR=10, BSTEN=0, and BSTAO=0

9.3 Ethernet specifications

9.3.1 Ethernet Switching Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. All Ethernet signals use pad type pad_fsr. The timing specifications described i the section assume a pad slew rate setting of 11 and a load of 50 pF[2].

9.3.2 Receive and Transmit signal timing specifications

This section provides timing specs that meet the requirements for RMII interfaces for a range of transceiver devices.

Table 40. Receive signal timing for RMII interfaces

	Characteristic	RMII Mode		Unit
		Min	Max	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
E3, E7	RMII_CLK pulse width high	35%	65%	RMII_CLK period
E4, E8	RMII_CLK pulse width low	35%	65%	RMII_CLK period
E1	RXD[1:0], CVS_DV, RXER to RMII_CLK setup	4	—	ns
E2	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
E6	RMII_CLK to TXD[1:0], TXEN valid	—	14	ns
E5	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

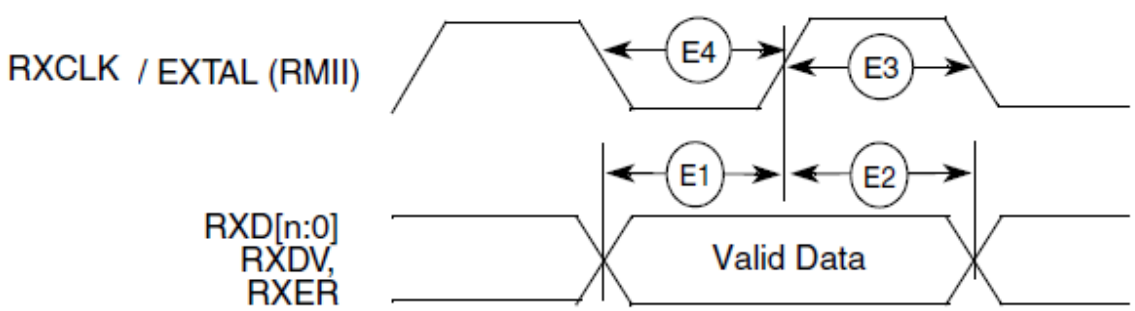


Figure 19. RMII receive signal timing diagram

2. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

NOTE

RESET pin has a external weak pull UP requirement if DDR3 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

Table 54. DDR3 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tCK
DDR2	CK clock low-level width	tCL	0.47	0.53	tCK
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	440	-	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	315	-	ps
DDR6	Address output setup time	tIS	440	-	ps
DDR7	Address output hold time	tIH	315	-	ps

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.5 LPDDR2 Read Cycle

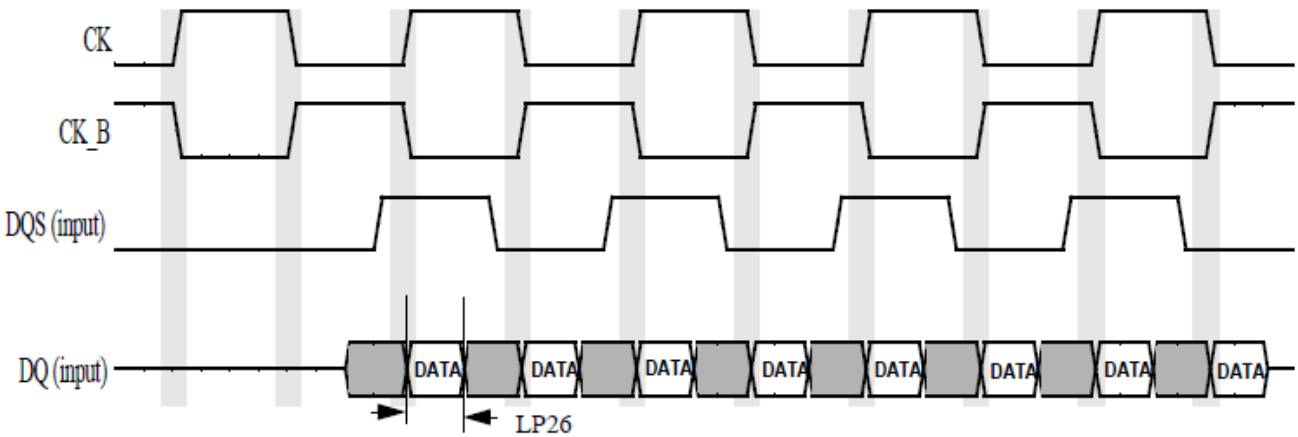


Figure 45. LPDDR2 Read cycle

Table 58. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	-	270	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

Table 63. DSPI timing (continued)

No.	Symbol	Characteristic	Condition	Min	Max	Unit
			Slave	4	—	
10	t_{HI}	Data Hold Time for Inputs	Master	0	—	ns
			Slave	2	—	
11	t_{DV}	Data Valid (after SCK edge) for Outputs	Master	—	5	ns
			Slave	—	10	
12	t_{HO}	Data Hold Time for Outputs	Master	0	—	ns
			Slave	0	—	

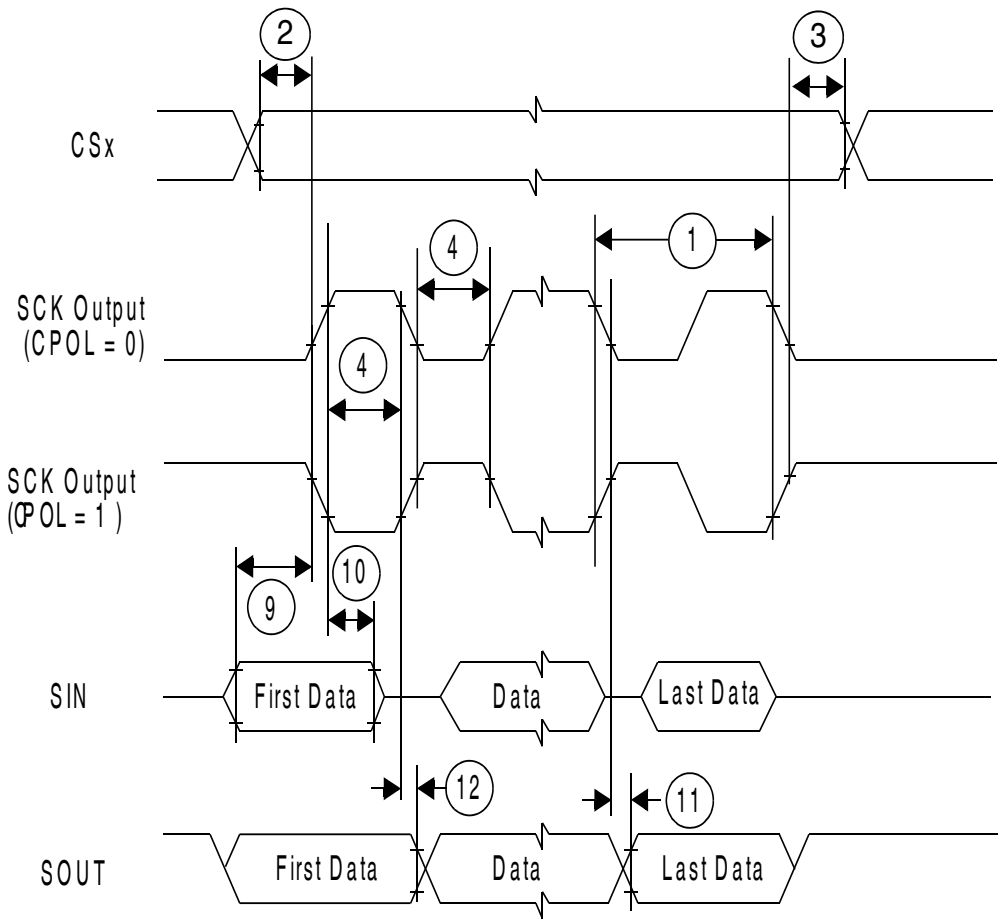


Figure 48. DSPI classic SPI timing master, CPHA=0

Table 67. 24MHz external oscillator electrical characteristics (continued)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
C_{IN}	Input Capacitance	EXTAL and XTAL pins	—	9	—	pF
VIH	XTAL pin input high voltage	—	0.8 x Vdd[1]	—	Vdd +0.3	V
VIL	XTAL pin input low voltage	—	Vss -0.3	—	0.2 x Vdd	V

1. V_{DD} =1.1 V ± 10%, TA = -40 to +85 °C, unless otherwise specified.

9.7.2 32 KHz Oscillator Specifications

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery or VDDIO such as the oscillator consumes power from VDDIO when that supply is available and transitions to the back up battery when VDDIO is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to the 128kHz internal RC clock divided by 4.

The OSC32k runs from vdd_rtc supply, generated inside OSC32k itself from VDDIO/ VBAT. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDIO range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell.

For example:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

Table 68. OSC32K Main Characteristics

	Notes	Min	Typ	Max
F_{OSC}	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.		32.768 KHz	
Current consumption	The 4 µA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 µA when ring oscillator is inactive, 20 µA when the ring		4 µA	

Table continues on the next page...

9.7.7 PLL5 (Ethernet PLL) Electrical Parameters

Table 73. PLL5 Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Cycle to cycle jitter (p2p)[1]	<400ps @ 50 MHz
Duty Cycle	45%~55%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out IO pad.

9.7.8 PLL4 (Audio PLL) Electrical Parameters

Table 74. PLL4 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)	<42ps @1128MHz
Period jitter(p2p)[1]	<115ps@1128MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad.

9.7.9 PLL6 (Video PLL) Electrical Parameters

Table 75. PLL6 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)[1]	<42ps @ 1128 MHz
Period jitter(p2p)	<130ps @960MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad & at use case frequency.

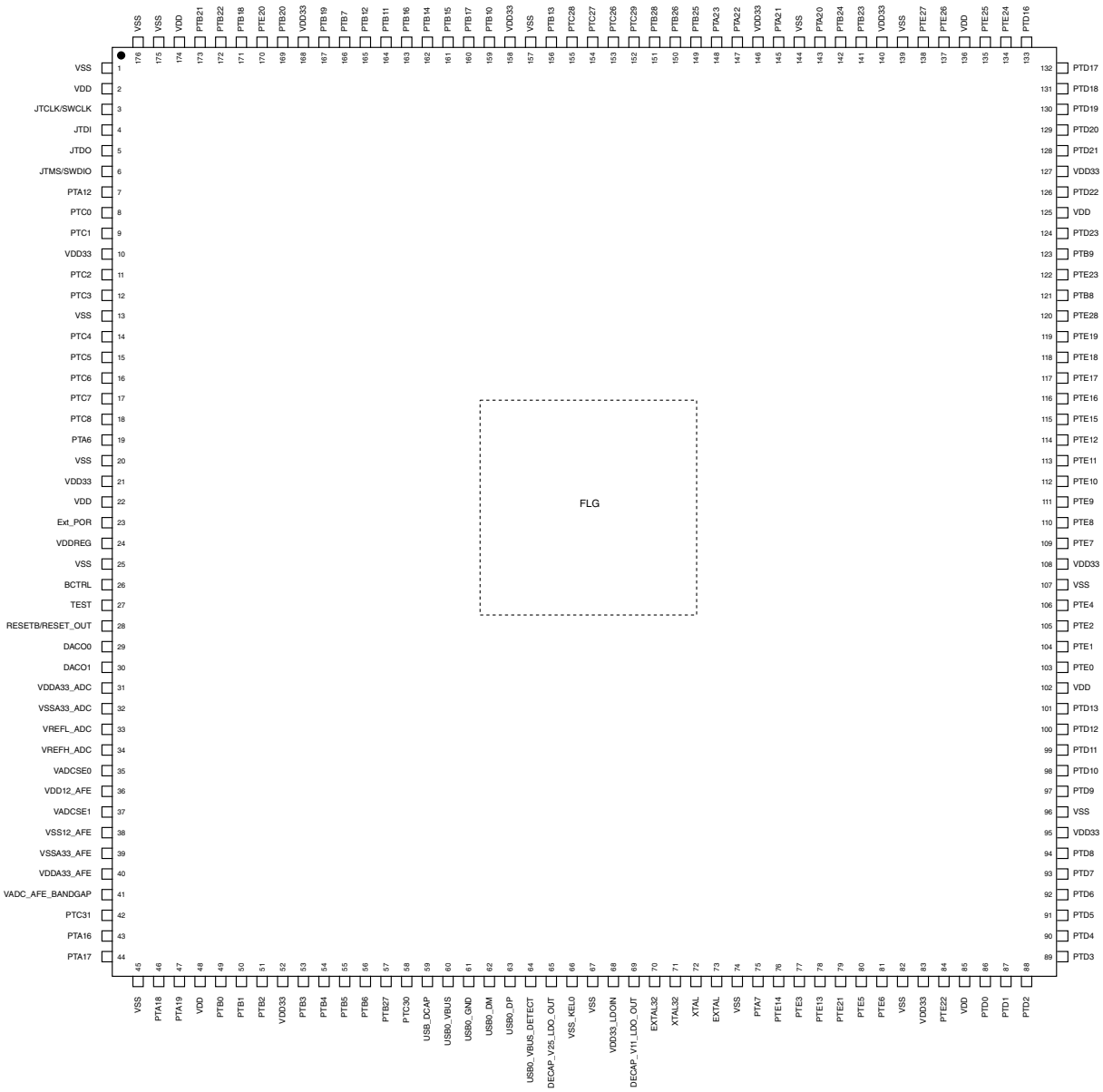


Figure 59. 176 LQFP Pinout Diagram

Table 79. Special Signal Considerations (continued)

Special Signal	Comments
JTCLK, JTDI, JTDO, JTMS	For JTAG the use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is matched. For example, do not use an external pull down on an input that has on-chip pull-up. JTDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTDO is detrimental and should be avoided.
LVDS0N, LVDS0P	Not recommended for application use, intended for clock observation purposes during debug only.
RESETB/RESET_OUT	Active low input used to generate a system wide reset (except the SRTC). A glitch filter is include to help prevent unexpected resets, a minimum pulse width of 125 nsecs is required to guarantee a reset is detected.
XTAL, EXTAL	A 24.0 MHz fundamental mode crystal should be connected between XTAL and EXTAL. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTAL must be directly driven by the external oscillator and EXTAL floated. The XTAL signal level must swing from ~0.8 x DECAP_V11_ LDO_OUT to ~0.2 V.
XTAL32, EXTAL32	If the user wishes to configure XTAL32 and EXTAL32 as an RTC oscillator, a 32.768 kHz crystal, (≤50 kΩ ESR, 10 pF load) should be connected between XTAL32 and EXTAL32. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from XTAL32 and EXTAL32 to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically XTAL32 and EXTAL32 should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into XTAL32 the EXTAL32 pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed DECAP_V11_ LDO_OUT level and the frequency should be <100 kHz under typical conditions. In the case where the SIRC is used, it is recommended to connect XTAL32 to ground and leave EXTAL32 floating.

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTC11	P4	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC12	P3	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC13	P1	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC14	R1	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC15	P2	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC16	R3	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC17	R4	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC26	D16	153	VDD33	GPIO	ALT3	RCON24	Input	Disabled
PTC27	E16	154	VDD33	GPIO	ALT3	RCON25	Input	Disabled
PTC28	E15	155	VDD33	GPIO	ALT3	RCON26	Input	Disabled
PTC29	C16	152	VDD33	GPIO	ALT3	RCON27	Input	Disabled
PTC30	T8	58	VDD33	GPIO	ALT3	RCON28	Input	Disabled
PTC31	W5	42	VDD33	GPIO	ALT3	RCON29	Input	Disabled
PTD0	Y17	86	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD1	Y18	87	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD2	V18	88	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD3	Y19	89	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD4	W19	90	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD5	W20	91	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD6	V20	92	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD7	V19	93	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD8	U17	94	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD9	U18	97	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD10	U20	98	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD11	T20	99	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD12	T19	100	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD13	T18	101	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD16	D20	133	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD17	E20	132	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD18	E18	131	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD19	F16	130	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD20	F17	129	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD21	F19	128	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD22	F20	126	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD23	G20	124	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD24	G19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD25	G18	—	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTD26	G16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD27	H16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD28	H17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD29	H18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD30	H20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD31	J20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE0	N16	103	VDD33	GPIO	ALT2	BMODE1	Input	Disabled
PTE1	N18	104	VDD33	GPIO	ALT2	BMODE0	Input	Disabled
PTE2	N19	105	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE3	Y15	77	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE4	N20	106	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE5	T16	80	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE6	W16	81	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE7	M20	109	VDD33	GPIO	ALT3	RCON0	Input	Disabled
PTE8	M19	110	VDD33	GPIO	ALT3	RCON1	Input	Disabled
PTE9	M17	111	VDD33	GPIO	ALT3	RCON2	Input	Disabled
PTE10	M16	112	VDD33	GPIO	ALT3	RCON3	Input	Disabled
PTE11	L16	113	VDD33	GPIO	ALT3	RCON4	Input	Disabled
PTE12	L17	114	VDD33	GPIO	ALT3	RCON5	Input	Disabled
PTE13	Y16	78	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE14	W15	76	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE15	L18	115	VDD33	GPIO	ALT3	RCON6	Input	Disabled
PTE16	L20	116	VDD33	GPIO	ALT3	RCON7	Input	Disabled
PTE17	K20	117	VDD33	GPIO	ALT3	RCON8	Input	Disabled
PTE18	K19	118	VDD33	GPIO	ALT3	RCON9	Input	Disabled
PTE19	K18	119	VDD33	GPIO	ALT3	RCON10	Input	Disabled
PTE20	A12	170	VDD33	GPIO	ALT3	RCON11	Input	Disabled
PTE21	V16	79	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE22	W17	84	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE23	J17	122	VDD33	GPIO	ALT3	RCON12	Input	Disabled
PTE24	D19	134	VDD33	GPIO	ALT3	RCON13	Input	Disabled
PTE25	C19	135	VDD33	GPIO	ALT3	RCON14	Input	Disabled
PTE26	C20	137	VDD33	GPIO	ALT3	RCON15	Input	Disabled
PTE27	B20	138	VDD33	GPIO	ALT3	RCON16	Input	Disabled
PTE28	K16	120	VDD33	GPIO	ALT3	RCON17	Input	Disabled
RESETB/ RESET_OUT	T4	28	VDD33	GPIO	—	RESETB/ RESET_OUT	—	—

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15 Revision History

The following table provides a revision history for this document.

Table 82. Revision History

Rev. No.	Date	Substantial Changes
Rev 1	12/2011	Initial release
Rev 2	2/2012	Updated feature list Updated VREG electrical specifications Updated LDO_1P1, LDO2P5 tables Updated DDR IO parameters Added DDR memory controller parameters Updated Power sequencing table Added Power supply diagram Updated Recommended operating conditions Replaced DryIce Tamper Electrical Specifications with Voltage and temperature monitor electrical specifications Updated VideoADC electricals. Updated VideoADC supply scheme diagram. Added VideoADC supply_decoupling diagram Added QuadSPI DDR mode electrical specifications Updated Fast internal RC oscillator table Updated Slow internal RC oscillator table Updated Pinouts section
Rev 3	4/2012	Updated device name throughout the document Minor editorial updates in the feature list Updated VREG electrical specifications Updated LDO electrical specifications Updated Power consumption operating behaviors table Added USB PHY Current Consumption table Updated GPIO parameters Updated DDR parameters Updated Power sequencing Updated Power supply figure Updated Recommended operating conditions table Removed Reset specifications Updated 12-bit DAC operating requirements Added a note in 12-bit ADC operating conditions section

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