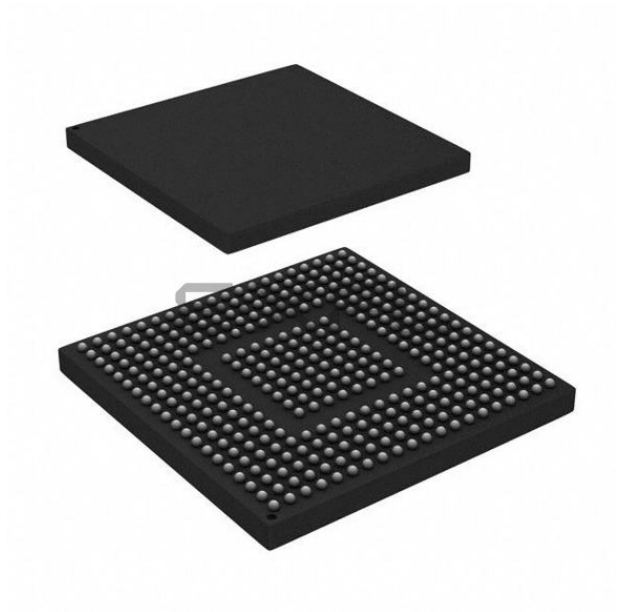

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5 + Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	400MHz, 133MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf532r2k2cmk4r

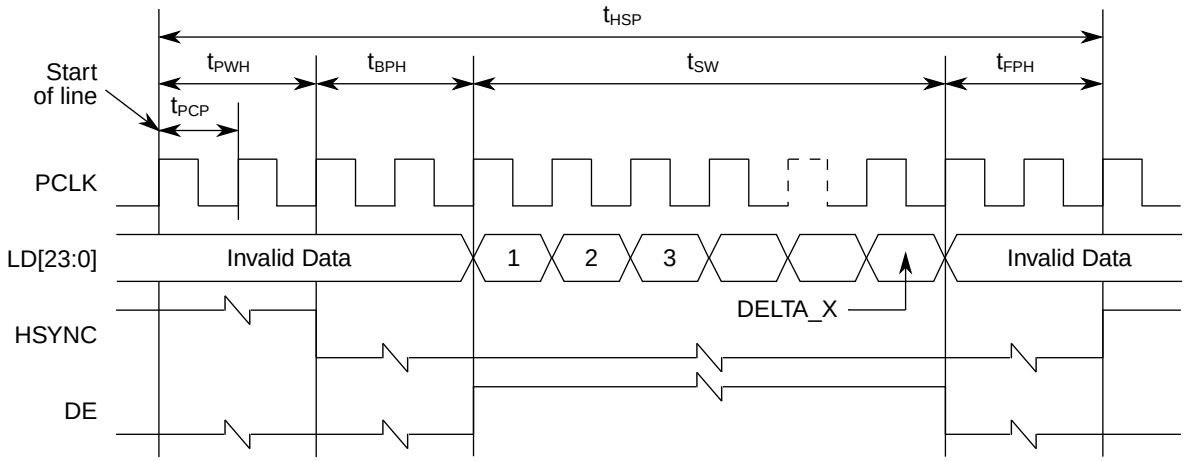

Figure 15. Horizontal sync timing

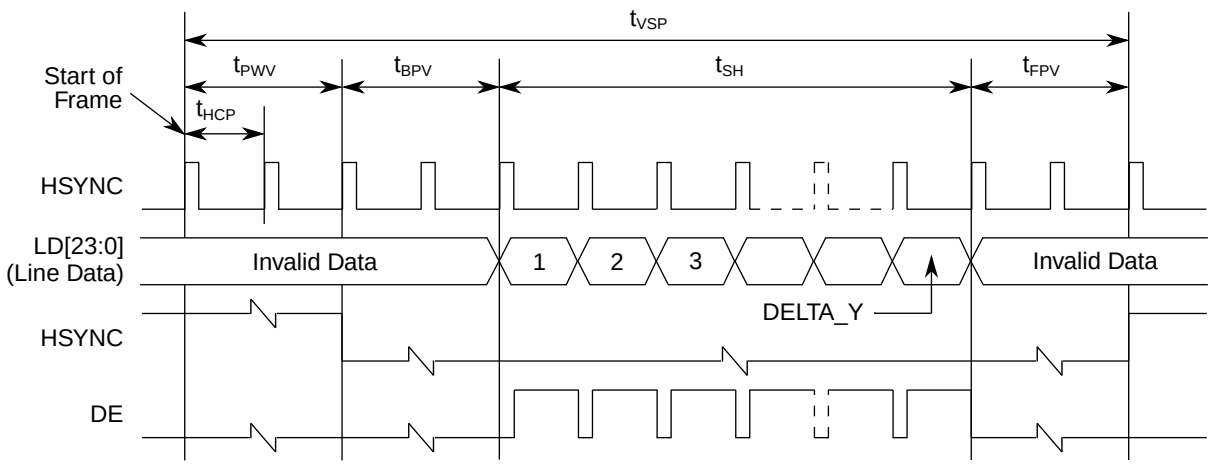

Figure 16. Vertical sync pulse

9.2.1.3 Interface to TFT LCD panels*f* access level

This section provides the access level timing parameters of the LCD interface.

Table 37. LCD Interface Timing Parameters 1, 2, 3*f* Access Level

Symbol	Description	Min	Max	Unit
t_{CKP}	Pixel Clock Period	11.2	_	ns
t^{DV}	TFT interface data valid after pixel clock	_	4.4	ns
t^{DV}	TFT interface HSYNC valid after pixel clock	_	4.4	ns
t^{DV}	TFT interface VSYNC valid after pixel clock	_	4.4	ns
t^{DV}	TFT interface DE valid after pixel clock	_	4.4	ns
t^{HO}	TFT interface output hold time for data and control bits	0	_	ns
	Relative skew between the data bits	_	4.4	ns

1. The characteristics in this table are based on the assumption that data is output at +ve edge and displays latch data on -ve edg6

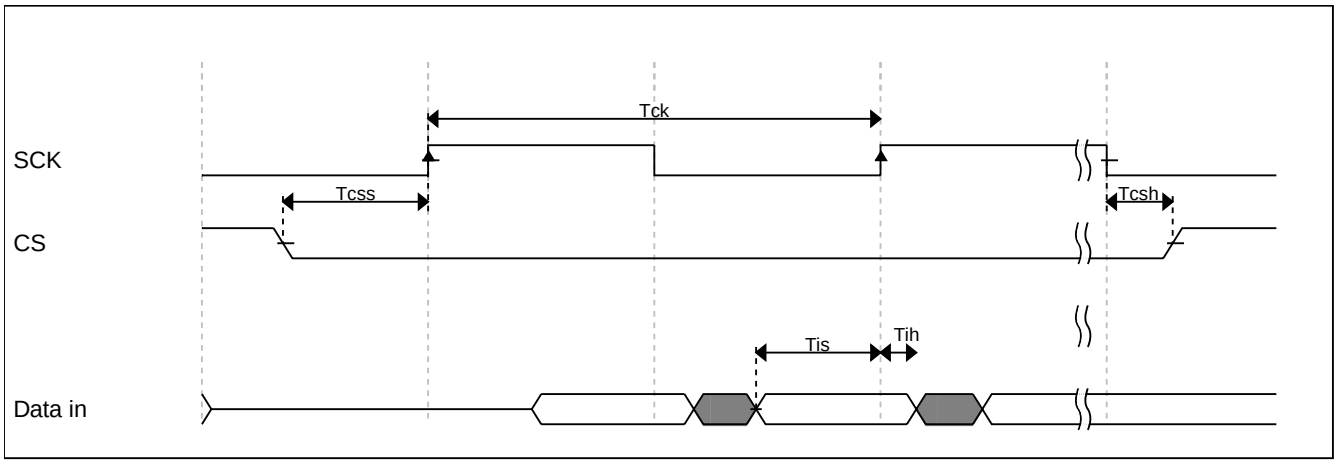

Figure 32. QuadSPI Input/Read timing (DDR mode)

NOTE

- The numbers are for a setting of 0x1 in register QuadSPI_SMPR[DDRSMP]
- Read frequency calculations should be: Tck/2 > (flash access time) + Setup (Tis) - (QuadSPI_SMPR[DDRSMP])x Tck/4
- Frequency calculator guideline (Max read frequency): Tck/2 > (Flash access time)max + (Tis)max - (QuadSPI_SMPR[DDRSMP]) x Tck/4
- Hold timing: flash_access (min) + flash_data_valid (min) > Tck/2 + HOLD(Tih) + (QuadSPI_SMPR[DDRSMP])Tck/4

Table 50. QuadSPI Input/Read timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	6.5	•	ns
T_{ih}	Hold time requirement for incoming data	0	•	ns

NOTE

9.5.4.3 DDR3 Write cycle

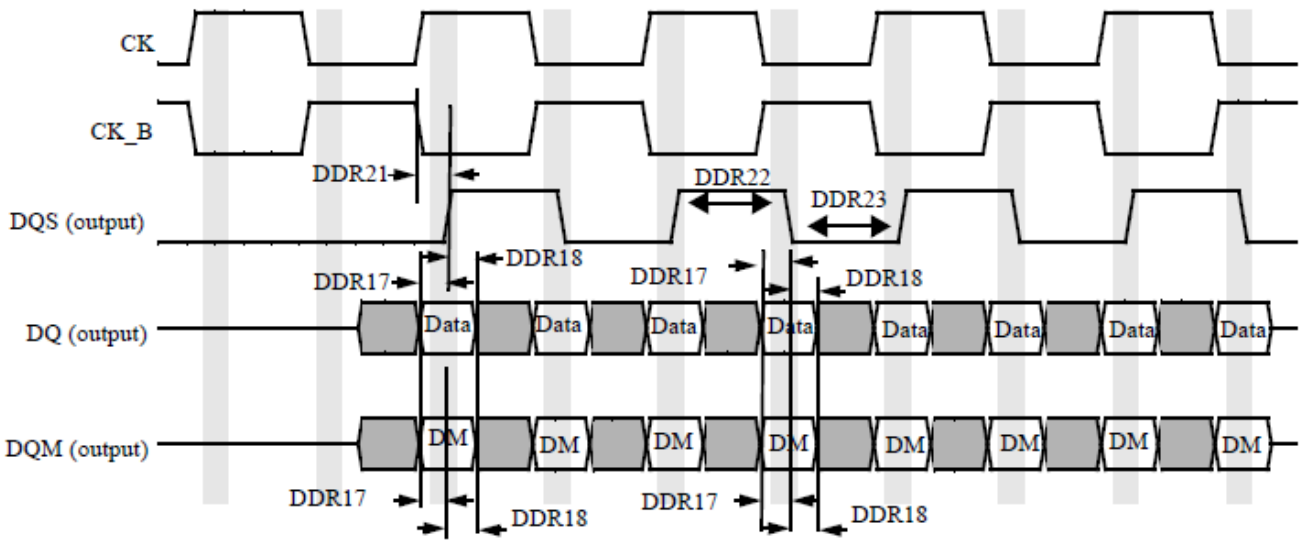

Figure 43. DDR3 Write cycle

Table 56. DDR3 Write cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	240	•	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	215	•	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR22	DQS low level width	tDQSL	0.45	0.55	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.5 LPDDR2 Read Cycle

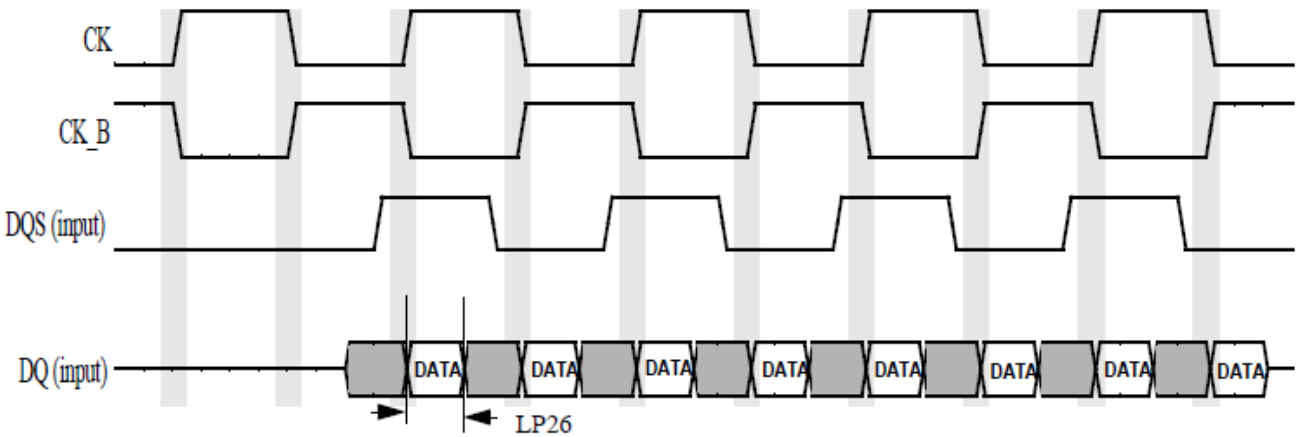

Figure 45. LPDDR2 Read cycle

Table 58. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	-	270	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

9.5.4.6 LPDDR2 Write Cycle

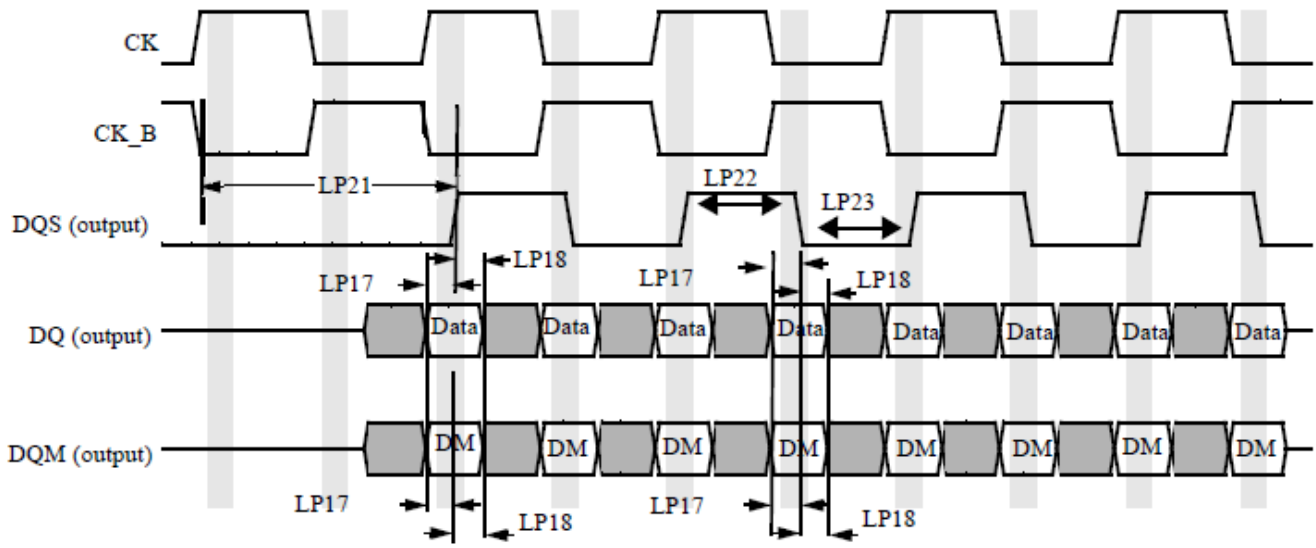

Figure 46. LPDDR3 Write Cycle

Table 59. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	tDS	220	0.55	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	tDH	220	0.55	ps
LP21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
LP22	DQS high level width	tDQSH	0.4	-	tCK
LP23	DQS low level width	tDQSL	0.4	-	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

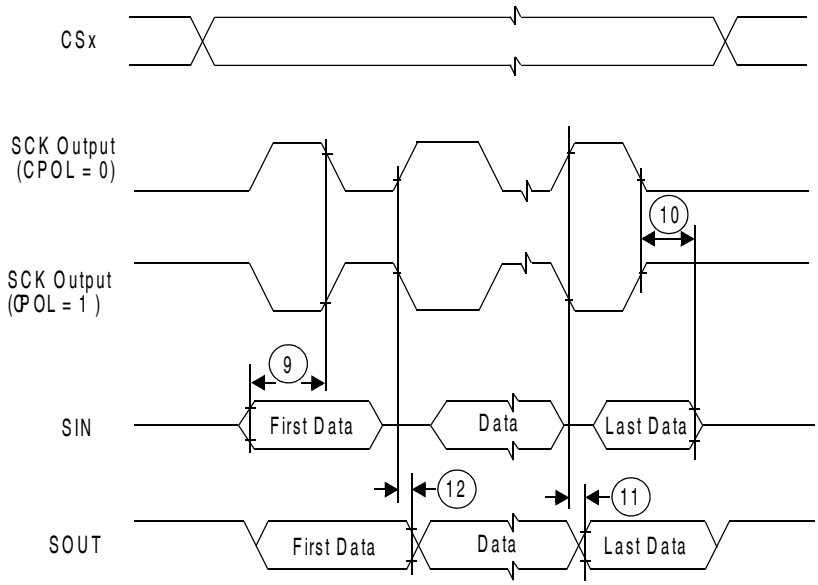

Figure 49. DSPI classic SPI timing master, CPHA=1

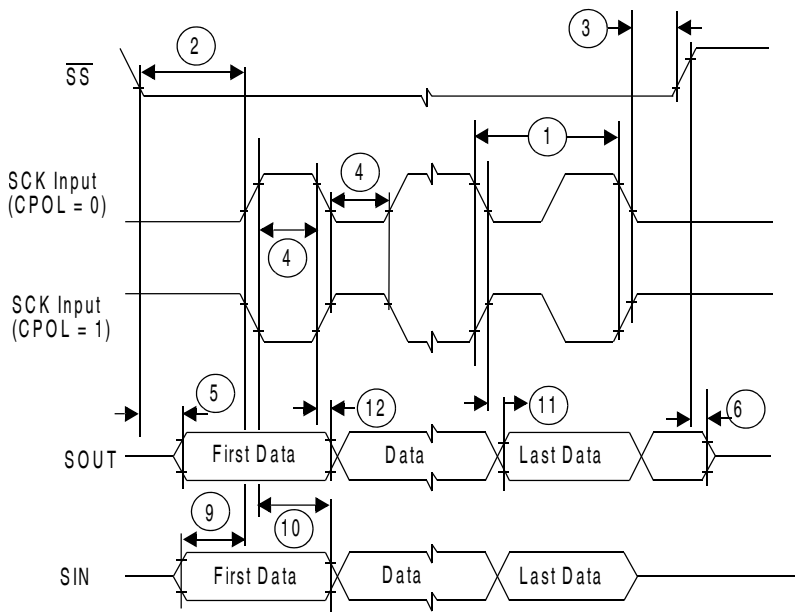

Figure 50. DSPI classic SPI timing slave, CPHA=0

Board type	Symbol	Description	364 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	ƒC/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	28	ƒC/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	37	ƒC/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	24	ƒC/W	1,3
•	$R_{\theta JB}$	Thermal resistance, junction to board	17	ƒC/W	4
•	$R_{\theta JC}$	Thermal resistance, junction to case	10	ƒC/W	5
•	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	ƒC/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

11 Dimensions

11.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing†s document number:

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
Y16	78	PTE13		PTE13	DCU0_G0			LCD13				
W15	76	PTE14		PTE14	DCU0_G1			LCD14				
L18	115	PTE15	RCON6	PTE15	DCU0_G2		RCON6	LCD15				
L20	116	PTE16	RCON7	PTE16	DCU0_G3		RCON7	LCD16				
K20	117	PTE17	RCON8	PTE17	DCU0_G4		RCON8	LCD17				
K19	118	PTE18	RCON9	PTE18	DCU0_G5		RCON9	LCD18				
K18	119	PTE19	RCON10	PTE19	DCU0_G6		RCON10	LCD19	I2C0_SCL			
A12	170	PTE20	RCON11	PTE20	DCU0_G7		RCON11	LCD20	I2C0_SDA		EWM_in	
V16	79	PTE21		PTE21	DCU0_B0			LCD21				
W17	84	PTE22		PTE22	DCU0_B1			LCD22				
J17	122	PTE23	RCON12	PTE23	DCU0_B2		RCON12	LCD23				
D19	134	PTE24	RCON13	PTE24	DCU0_B3		RCON13	LCD24				
C19	135	PTE25	RCON14	PTE25	DCU0_B4		RCON14	LCD25				
C20	137	PTE26	RCON15	PTE26	DCU0_B5		RCON15	LCD26				
B20	138	PTE27	RCON16	PTE27	DCU0_B6		RCON16	LCD27	I2C1_SCL			
K16	120	PTE28	RCON17	PTE28	DCU0_B7		RCON17	LCD28	I2C1_SDA		EWM_out	
V15	75	PTA7		PTA7	VIU_PIX_CLK							
T14	•	EXT_TAMPER0			EXT_TAMPER0							
U14	•	EXT_TAMPER1			EXT_TAMPER1							
T13	•	EXT_TAMPER2/EXT_WM0_TAMPER_IN			EXT_TAMPER2/EXT_WM0_TAMPER_IN							
U13	•	EXT_TAMPER3/EXT_WM0_TAMPER_OUT			EXT_TAMPER3/EXT_WM0_TAMPER_OUT							
U12	•	EXT_TAMPER4/EXT_WM1_TAMPER_IN			EXT_TAMPER4/EXT_WM1_TAMPER_IN							
U10	•	EXT_TAMPER5/EXT_WM1_TAMPER_OUT			EXT_TAMPER5/EXT_WM1_TAMPER_OUT							
G7	2	VDD			VDD							
J7	22	VDD			VDD							
L7	48	VDD			VDD							
H8	•	VDD			VDD							
K8	85	VDD			VDD							

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[79]	PORT2[15]	PTD0	IOMUXC_PTD0	4004813C
RGPIO[80]	PORT2[16]	PTD1	IOMUXC_PTD1	40048140
RGPIO[81]	PORT2[17]	PTD2	IOMUXC_PTD2	40048144
RGPIO[82]	PORT2[18]	PTD3	IOMUXC_PTD3	40048148
RGPIO[83]	PORT2[19]	PTD4	IOMUXC_PTD4	4004814C
RGPIO[84]	PORT2[20]	PTD5	IOMUXC_PTD5	40048150
RGPIO[85]	PORT2[21]	PTD6	IOMUXC_PTD6	40048154
RGPIO[86]	PORT2[22]	PTD7	IOMUXC_PTD7	40048158
RGPIO[87]	PORT2[23]	PTD8	IOMUXC_PTD8	4004815C
RGPIO[88]	PORT2[24]	PTD9	IOMUXC_PTD9	40048160
RGPIO[89]	PORT2[25]	PTD10	IOMUXC_PTD10	40048164
RGPIO[90]	PORT2[26]	PTD11	IOMUXC_PTD11	40048168
RGPIO[91]	PORT2[27]	PTD12	IOMUXC_PTD12	4004816C
RGPIO[92]	PORT2[28]	PTD13	IOMUXC_PTD13	40048170
RGPIO[93]	PORT2[29]	PTB23	IOMUXC_PTB23	40048174
RGPIO[94]	PORT2[30]	PTB24	IOMUXC_PTB24	40048178
RGPIO[95]	PORT2[31]	PTB25	IOMUXC_PTB25	4004817C
RGPIO[96]	PORT3[0]	PTB26	IOMUXC_PTB26	40048180
RGPIO[97]	PORT3[1]	PTB27	IOMUXC_PTB27	40048184
RGPIO[98]	PORT3[2]	PTB28	IOMUXC_PTB28	40048188
RGPIO[99]	PORT3[3]	PTC26	IOMUXC_PTC26	4004818C
RGPIO[100]	PORT3[4]	PTC27	IOMUXC_PTC27	40048190
RGPIO[101]	PORT3[5]	PTC28	IOMUXC_PTC28	40048194
RGPIO[102]	PORT3[6]	PTC29	IOMUXC_PTC29	40048198
RGPIO[103]	PORT3[7]	PTC30	IOMUXC_PTC30	4004819C
RGPIO[104]	PORT3[8]	PTC31	IOMUXC_PTC31	400481A0
RGPIO[105]	PORT3[9]	PTE0	IOMUXC_PTE0	400481A4
RGPIO[106]	PORT3[10]	PTE1	IOMUXC_PTE1	400481A8
RGPIO[107]	PORT3[11]	PTE2	IOMUXC_PTE2	400481AC
RGPIO[108]	PORT3[12]	PTE3	IOMUXC_PTE3	400481B0
RGPIO[109]	PORT3[13]	PTE4	IOMUXC_PTE4	400481B4
RGPIO[110]	PORT3[14]	PTE5	IOMUXC_PTE5	400481B8
RGPIO[111]	PORT3[15]	PTE6	IOMUXC_PTE6	400481BC
RGPIO[112]	PORT3[16]	PTE7	IOMUXC_PTE7	400481C0
RGPIO[113]	PORT3[17]	PTE8	IOMUXC_PTE8	400481C4
RGPIO[114]	PORT3[18]	PTE9	IOMUXC_PTE9	400481C8
RGPIO[115]	PORT3[19]	PTE10	IOMUXC_PTE10	400481CC
RGPIO[116]	PORT3[20]	PTE11	IOMUXC_PTE11	400481D0
RGPIO[117]	PORT3[21]	PTE12	IOMUXC_PTE12	400481D4

Table continues on the next page...

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