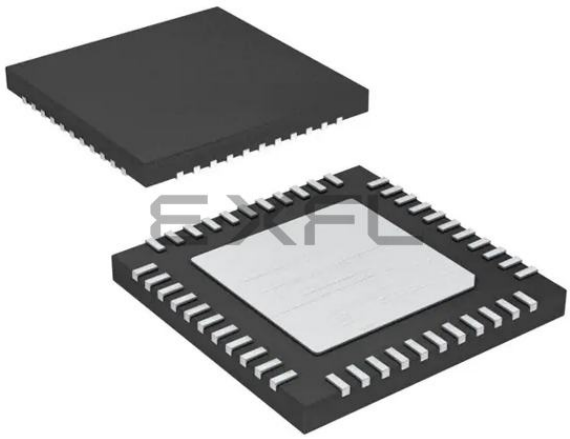
Microchip Technology - PIC18F45J50T-I/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2.15V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f45j50t-i-ml

PIC18F46J50 FAMILY

PIC18F46J50 Family
Silicon Errata and Data Sheet Clarification

The PIC18F46J50 family devices that you have received conform functionally to the current Device Data Sheet (DS39931**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F46J50 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F46J50 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A2	A4
PIC18F24J50	4C0Xh	2h	4h
PIC18F25J50	4C2Xh		
PIC18F26J50	4C4Xh		
PIC18F44J50	4C6Xh		
PIC18F45J50	4C8Xh		
PIC18F46J50	4CAXh		
PIC18LF24J50	4CCXh		
PIC18LF25J50	4CEXh		
PIC18LF26J50	4D0Xh		
PIC18LF44J50	4D2Xh		
PIC18LF45J50	4D4Xh		
PIC18LF46J50	4D6Xh		

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F2XJXX/4XJXX Family Flash Microcontroller Programming Specification"* (DS39687) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A2	A4
Master Synchronous Serial Port (MSSP1)	I^2C™ Modes	1.	Must keep LATB<5:4> bits clear.	X	
Master Synchronous Serial Port (MSSP)	I^2C Slave	2.	Module may not receive the correct data if there is a delay in reading SSPxBUF after SSPxIF interrupt.	X	X
Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	Enable/ Disable	3.	If interrupts are enabled, a 2 TCY delay is needed after re-enabling the module.	X	X
10-Bit Analog-to-Digital Converter (ADC)	FOSC/2 Clock	4.	FOSC/2 A/D Conversion mode may not meet linearity error limits.	X	X
Parallel Master Port (PMP)	PSP/PMP	5.	The data bus may not work correctly.	X	
Low-Power Modes (Deep Sleep)	Deep Sleep	6.	Wake-up events that occur during Deep Sleep entry may not generate an event.	X	X
DC Characteristics (Supply Voltage)	Supply Voltage	7.	Minimum operating voltage (VDD) parameter for “F” devices is 2.25V.	X	
Analog-to-Digital Converter (Band Gap Reference)	Band Gap Reference	8.	At high VDD voltages, performing an A/D conversion on Channel 15 could have issues.	X	X
Charge Time Measurement Unit (CTMU)	Constant Current	9.	Low voltages turn off constant current source.	X	
Timer1/3	Interrupt	10.	When the timer is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Master Synchronous Serial Port (MSSP1)

If the LATB<5> or LATB<4> bit is set, the MSSP1 module will not work correctly in the I^2C™ modes. If both LATB<5> and LATB<4> are clear, the module will work normally.

Work around

Clear the bits, LATB<5:4>, prior to enabling the MSSP1 module in an I^2C mode. Keep these bits clear while using the module.

For operation in I^2C modes, the TRISB<5:4> bits should be set.

Affected Silicon Revisions

A2	A4						
X							

2. Module: Master Synchronous Serial Port (MSSP)

In extremely rare cases, when configured for I^2C™ slave reception, the MSSP module may not receive the correct data. This occurs only if the Serial Receive/Transmit Buffer Register (SSPxBUF) is not read within a window after the SSPxIF interrupt has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I^2C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPxCON2<0>).
- Each time the SSPxIF is set, read the SSPxBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A2	A4						
X	X						

3. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations, when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTAx<7> = 0)
- The EUSART is re-enabled (RCSTAx<7> = 1)
- A 2-cycle instruction is executed immediately after setting SPEN = 1

Work around

Add a 2 TCY delay after any instruction that re-enables the EUSART module (sets SPEN = 1). Refer to Example 1.

EXAMPLE 1: RE-ENABLING A EUSART MODULE

```
;Initial conditions: SPEN = 0 (module disabled)
;To re-enable the module:
;Re-Initialize TXSTAx, BAUDCONx, SPBRGx, SPBRGHx registers (if needed)
;Re-Initialize RCSTAx register (if needed), but do not set SPEN = 1 yet

;Now enable the module, but add a 2-Tcy delay before executing any two-cycle
;instructions
bsf    RCSTA1, SPEN  ;or RCSTA2 if EUSART2
nop    ;1 Tcy delay
nop    ;1 Tcy delay (two total)

;CPU may now execute 2 cycle instructions
```

Affected Silicon Revisions

A2	A4						
X	X						

4. Module: 10-Bit Analog-to-Digital Converter (ADC)

When the A/D conversion clock select bits are set for FOSC/2 (ADCON1<2:0> = 000), the Integral Linearity Error (EIL) parameter (A03) and Differential Linearity Error (EDL) parameter (A04) may exceed data sheet specifications.

Work around

Select one of the alternate AD clock sources shown in Table 3. The EIL and EDL parameters are met for the other clocking options.

TABLE 3: ALTERNATE ADC SETTINGS

ADCON1<2:0> ADCS<2:0>	Clock Setting
110	FOSC/64
101	FOSC/16
100	FOSC/4
011	FRC
010	FOSC/32
001	FOSC/8

Affected Silicon Revisions

A2	A4						
X	X						

5. Module: Parallel Master Port (PMP)

When configured for Parallel Slave Port (PMMODEH<1:0> = 0x and PMPEN = 1), the data bus (PMD<7:0>) may not work correctly and incorrect data could be captured into the PMDIN1L register.

When configured for Parallel Master Port (PMMODEH<1:0> = 1x and PMPEN = 1), clearing a PMEx bit to disable a PMP address line also disables the corresponding PMDx data bus line.

Work around

None.

Affected Silicon Revisions

A2	A4						
X							

6. Module: Low-Power Modes (Deep Sleep)

Entering Deep Sleep mode takes approximately 2 TCY, following the SLEEP instruction. Wake-up events that occur during this Deep Sleep entry period may not generate a wake-up event.

Work around

If using the RTCC alarm for Deep Sleep wake-up, code should only enter Deep Sleep mode when the RTCC Value registers read synchronization bit (RTCCFG<4>) is clear.

This will prevent missing an RTCC alarm that could occur during the period after the SLEEP instruction, but before the Deep Sleep mode has not been fully entered.

The revision A4 silicon allows insertion of a single instruction between setting the Deep Sleep Enable bit (DSEN, DSCONH<7>) and issuing the SLEEP instruction (see Example 2). The insertion of a NOP instruction before the SLEEP instruction eliminates the 2 TCY window where wake-up events could be missed.

Before using this work around, users should check their device's revision ID bits to verify that they have the A4 silicon. This can be done at run time by a table read from address, 3FFFFEh.

On revision A2 silicon devices, the instruction cannot be inserted between setting the DSEN bit and executing the SLEEP instruction or the device will enter conventional Sleep mode, not Deep Sleep.

Even on A4 silicon devices, if the firmware immediately executes SLEEP after setting DSEN, the device will enter Deep Sleep mode without benefitting from this work around.

EXAMPLE 2: DEEP-SLEEP WAKE-UP WORK AROUND

```
EnterDeepSleep:
    bsf     DSCONH, DSEN        ; Enter Deep Sleep mode on SLEEP instruction
    nop                         ; Not compatible with A2 silicon
    sleep                       ; Enter Deep Sleep mode
    (…)                         ; Add code here to handle wake up events that may
                                ; have been asserted prior to Deep Sleep entry
    goto    EnterDeepSleep      ; re-attempt Deep Sleep entry if desired
```

Affected Silicon Revisions

A2	A4						
X							

7. Module: DC Characteristics (Supply Voltage)

The minimum operating voltage (V_{DD}) parameter (D001) for "F" devices is 2.25V. For "LF" devices (such as the PIC18LF46J50), the minimum rated V_{DD} operating voltage is 2.0V.

Work around

None.

Affected Silicon Revisions

A2	A4						
X							

8. Module: Analog-to-Digital Converter (Band Gap Reference)

At high V_{DD} voltages (ex: >2.5V), performing an ADC conversion on Channel 15 (the V_{BG} absolute reference) can temporarily disturb the reference voltage supplied to the HLVD module and comparator module (only when configured to use the V_{IRV}). At lower V_{DD} voltages, the disturbance will be less or non-existent.

Work around

If precise HLVD or comparator V_{IRV} thresholds are required at high V_{DD} voltages, avoid performing ADC conversions on Channel 15 while simultaneously using the HLVD or comparator V_{IRV}. If an ADC conversion is performed on Channel 15, a settling time of approximately 100 µs is needed before the reference voltage fully returns to the original value.

Affected Silicon Revisions

A2	A4						
X	X						

9. Module: Charge Time Measurement Unit (CTMU)

On an "F" device, the CTMU current source will stop sourcing current if the applied V_{DD} voltage falls below the LVDSTAT (WDTCON<6>) threshold (2.45V nominal). When V_{DD} is above the LVDSTAT threshold, the CTMU will function normally. This issue does not apply to "LF" devices. The current source will continue to function normally at all rated voltages for these devices.

Work around

None

Affected Silicon Revisions

A2	A4						
X							

10. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to `0x0000` when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 3.

EXAMPLE 3: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;         //Stop timer from incrementing
PIE1bits.TMR1IE = 0;          //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                 //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;         //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);          //Wait for 2 timer increments more than the Updated Timer
                              //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                        //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;          //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;          //Now re-enable interrupt vectoring for timer 1
```

Affected Silicon Revisions

A2	A4						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (DS39931**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Special Features (CONFIG2L)

The “T1DIG” feature mentioned in the Device Data Sheet (DS39931**D**) is not implemented in this device family. The feature, associated with bit 3 of the CONFIG2L Configuration register, is discussed in **Section 26.1 “Configuration Bits”** and **Section 2.5.1 “Oscillator Control Register”**.

For application firmware to switch to the Timer1 clock source, it must first enable the crystal driver by setting the T1OSCEN bit (T1CON<3>). The microcontroller will ignore attempts to clock switch to the Timer1 clock source when the crystal driver is disabled.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2009)

First release of this document. Silicon issues 1 (T1DIG), 2-3 (MSSP), 4 (EUSART), 5 (ADC), 6 (PMP), 7 (Deep Sleep), 8 (Supply Voltage).

Rev B Document (5/2009)

Added silicon issues 9 (Band Gap Reference) and 10 (Charge Time Measurement Unit – CTMU).

Rev C Document (1/2010)

Converted existing document for the A2 silicon revision to the new, combined format. (There were no other silicon errata or data sheet clarification documents for the device family.)

Removed silicon issue 1 (Special Features, T1DIG) and modified decremented issue 1, formerly 2 (MSSP1) and 6 (Low-Power Modes – Deep Sleep). Added data sheet clarifications 1 (Special Features – CONFIG2L), 2 (DC Characteristics – Power-Down Current) and 3 (DC Characteristics – Input Leakage).

Rev D Document (4/2011)

Updated text description for silicon issue 5 (Parallel Master Port) and removed data sheet clarifications 2 (DC Characteristics – Power-Down Current) and 3 (DC Characteristics – Input Leakage) since both clarifications have been included in the PIC18F46J50 Data Sheet.

Rev E Document (7/2014)

Added MPLAB X IDE; Added Module 10, Timer1/3, to Silicon Errata Issues section.

Note the following details of the code protection feature on Microchip devices:

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