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Details

Product Status	Not For New Designs
Core Processor	CPU32
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	18
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	7.5K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-QFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/sc68376bgcab20

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SECTION 1 INTRODUCTION

The MC68336 and the MC68376 are highly-integrated 32-bit microcontrollers, combining high-performance data manipulation capabilities with powerful peripheral subsystems.

MC68300 microcontrollers are built up from standard modules that interface through a common intermodule bus (IMB). Standardization facilitates rapid development of devices tailored for specific applications.

The MC68336 incorporates a 32-bit CPU (CPU32), a system integration module (SIM), a time processor unit (TPU), a configurable timer module (CTM4), a queued serial module (QSM), a 10-bit queued analog-to-digital converter module (QADC), a 3.5-Kbyte TPU emulation RAM module (TPURAM), and a 4-Kbyte standby RAM module (SRAM).

The MC68376 includes all of the aforementioned modules, plus a CAN 2.0B protocol controller module (TouCAN[™]) and an 8-Kbyte masked ROM (MRM).

The MC68336/376 can either synthesize the system clock signal from a fast reference or use an external clock input directly. Operation with a 4.194 MHz reference frequency is standard. The maximum system clock speed is 20.97 MHz. System hardware and software allow changes in clock rate during operation. Because MCU operation is fully static, register and memory contents are not affected by clock rate changes.

High-density complementary metal-oxide semiconductor (HCMOS) architecture makes the basic power consumption of the MCU low. Power consumption can be minimized by stopping the system clock. The CPU32 instruction set includes a low-power stop (LPSTOP) instruction that efficiently implements this capability.

Documentation for the Modular Microcontroller Family follows the modular construction of the devices in the product line. Each microcontroller has a comprehensive user's manual that provides sufficient information for normal operation of the device. The user's manual is supplemented by module reference manuals that provide detailed information about module operation and applications. Refer to Motorola publication *Advanced Microcontroller Unit (AMCU) Literature* (BR1116/D) for a complete listing of documentation.



2.2 CPU32 Registers

- A6–A0 Address registers (index registers)
- A7 (SSP) Supervisor stack pointer
- A7 (USP) User stack pointer
 - CCR Condition code register (user portion of SR)
 - D7–D0 Data registers (index registers)
 - DFC Alternate function code register
 - PC Program counter
 - SFC Alternate function code register
 - SR Status register
 - VBR Vector base register
 - X Extend indicator
 - N Negative indicator
 - Z Zero indicator
 - V Two's complement overflow indicator
 - C Carry/borrow indicator

2.3 Pin and Signal Mnemonics

ADDR[23:0] — Address Bus

- AN[59:48]/[3:0] QADC Analog Input
 - AN[w, x, y, z] QADC Analog Input
 - AS Address Strobe
 - AVEC Autovector
 - BERR Bus Error
 - BG Bus Grant
 - BGACK Bus Grant Acknowledge
 - BKPT Breakpoint
 - BR Bus Request
 - CANRX0 TouCAN Receive Data
 - CANTX0 TouCAN Transmit Data
 - CLKOUT System Clock
 - CS[10:0] Chip Selects
 - CSBOOT Boot ROM Chip Select
 - CPWM[8:5] CTM Pulse Width Modulation Channel
- CTD[10:9]/[4:3] CTM Double Action Channel
 - CTM2C CTM Modulus Clock
 - DATA[15:0] Data Bus
 - DS Data Strobe



5.4 System Protection

The system protection block preserves reset status, monitors internal activity, and provides periodic interrupt generation. **Figure 5-6** is a block diagram of the submodule.



Figure 5-6 System Protection Block

5.4.1 Reset Status

The reset status register (RSR) latches internal MCU status during reset. Refer to **5.7.10 Reset Status Register** for more information.

5.4.2 Bus Monitor

The internal bus monitor checks data and size acknowledge ($\overline{\text{DSACK}}$) or autovector ($\overline{\text{AVEC}}$) signal response times during normal bus cycles. The monitor asserts the internal bus error ($\overline{\text{BERR}}$) signal when the response time is excessively long.

DSACK and AVEC response times are measured in clock cycles. Maximum allowable response time can be selected by setting the bus monitor timing (BMT[1:0]) field in the system protection control register (SYPCR). **Table 5-4** shows the periods allowed.



Figure 5-18 is a timing diagram for power-on reset. It shows the relationships between RESET, V_{DD} , and bus signals.



Figure 5-18 Power-On Reset

5.7.8 Use of the Three-State Control Pin

Asserting the three-state control (TSC) input causes the MCU to put all output drivers in a disabled, high-impedance state. The signal must remain asserted for approximately ten clock cycles in order for drivers to change state.

When the internal clock synthesizer is used (MODCLK held high during reset), synthesizer ramp-up time affects how long the ten cycles take. Worst case is approximately 20 milliseconds from TSC assertion.

When an external clock signal is applied (MODCLK held low during reset), pins go to high-impedance state as soon after TSC assertion as approximately ten clock pulses have been applied to the EXTAL pin.

NOTE

When TSC assertion takes effect, internal signals are forced to values that can cause inadvertent mode selection. Once the output drivers change state, the MCU must be powered down and restarted before normal operation can resume.



8.9 External Multiplexing Operation

External multiplexers concentrate a number of analog signals onto a few inputs to the analog converter. This is helpful in applications that need to convert more analog signals than the A/D converter can normally provide. External multiplexing also puts the multiplexer closer to the signal source. This minimizes the number of analog signals that need to be shielded due to the close proximity of noisy, high speed digital signals near the MCU.

The QADC can use from one to four external multiplexers to expand the number of analog signals that may be converted. Up to 32 analog channels can be converted through external multiplexer selection. The externally multiplexed channels are automatically selected from the channel field of the conversion command word (CCW) table, the same as internally multiplexed channels.

All of the automatic queue features are available for externally and internally multiplexed channels. The software selects externally multiplexed mode by setting the MUX bit in QACR0.

Figure 8-3 shows the maximum configuration of four external multiplexers connected to the QADC. The external multiplexers select one of eight analog inputs and connect it to one analog output, which becomes an input to the QADC. The QADC provides three multiplexed address signals (MA[2:0]), to select one of eight inputs. These outputs are connected to all four multiplexers. The analog output of each multiplexer is each connected to one of four separate QADC inputs — ANw, ANx, ANy, and ANz.



To accommodate wide variations of the main MCU clock frequency f_{sys} , QCLK is generated by a programmable prescaler which divides the MCU system clock to a frequency within the specified QCLK tolerance range. The prescaler also allows the duty cycle of the QCLK waveform to be programmable.

The basic high phase of the QCLK waveform is selected with the PSH (prescaler clock high time) field in QACR0, and the basic low phase of QCLK with the PSL (prescaler clock low time) field. The duty cycle of QCLK can be further modified with the PSA (prescaler add a clock tick) bit in QACR0. The combination of the PSH and PSL parameters establishes the frequency of QCLK.

Figure 8-8 shows that the prescaler is essentially a variable pulse width signal generator. A 5-bit down counter, clocked at the system clock rate, is used to create both the high phase and the low phase of the QCLK signal. At the beginning of the high phase, the 5-bit counter is loaded with the 5-bit PSH value. When the zero detector finds that the high phase is finished, QCLK is reset. A 3-bit comparator looks for a one's complement match with the 3-bit PSL value, which is the end of the low phase of QCLK. The PSA bit allows the QCLK high-to-low transition to be delayed by a half cycle of the input clock.

The following sequence summarizes the process of determining what values are to be put into the prescaler fields in QACR0:

- 1. Choose the system clock frequency f_{svs} .
- 2. Choose first-try values for PSH, PSL, and PSA, then skip to step 4.
- 3. Choose different values for PSH, PSL, and PSA.
- If the QCLK high time is less than t_{PSH} (QADC clock duty cycle Minimum high phase time), return to step 3. Refer to **Table A-13** for more information on t_{PSH}. QCLK high time is determined by the following equation:

QCLK high time (in ns) =
$$\frac{1000 (1 + PSH + 0.5 PSA)}{f_{sys}(in MHz)}$$

where PSH = 0 to 31 and PSA = 0 or 1.

 If QCLK low time is less than t_{PSL} (QADC clock duty cycle – Minimum low phase time), return to step 3. Refer to **Table A-13** for more information on t_{PSL}. QCLK low time is determined by the following equation:

QCLK low time (in ns) =
$$\frac{1000 (1 + PSL - 0.5 PSA)}{f_{sys}(in MHz)}$$

where PSL = 0 to 7 and PSA = 0 or 1.



SECTION 10 CONFIGURABLE TIMER MODULE 4

This section is an overview of CTM4 function. Refer to the *CTM Reference Manual* (CTMRM/AD) for a comprehensive discussion of CTM capabilities.

10.1 General

The configurable timer module 4 (CTM4) consists of several submodules which are located on either side of the CTM4 internal submodule bus (SMB). All data and control signals within the CTM4 are passed over this bus. The SMB is connected to the outside world via the bus interface unit submodule (BIUSM), which is connected to the intermodule bus (IMB), and subsequently the CPU32. This configuration allows the CPU32 to access the data and control registers in each CTM4 submodule on the SMB. Three time base buses (TBB1, TBB2 and TBB4), each 16-bits wide, are used to transfer timing information from counters to action submodules. **Figure 10-1** shows a block diagram of the CTM4.







In the CTM4, TBB2 is global and accessible to every submodule. TBB1 and TBB4 are split to form two local time base buses. **Table 10-1** shows which time base buses are available to each CTM4 submodule.

	Global/Loca Bus All	I Time Base ocation		Global/Local Time Base Bus Allocation				
Submodule	Global Bus A	Global Bus B	Submodule	Global Bus A	Global Bus B			
DASM9	TBB1	TBB2	MCSM 2	TBB4	TBB2			
DASM10	TBB1	TBB2	DASM 3	TBB4	TBB2			
MCSM 11	TBB1	TBB2	DASM 4	TBB4	TBB2			
FCSM 12	TBB1	TBB2						

Table 10-1 CTM4 Time Base Bus Allocation

Each PWMSM has an independent 16-bit counter and 8-bit prescaler clocked by the PCLK1 signal, which is generated by the CPSM. The PWMSMs are not connected to any of the time base buses. Refer to **10.9 Pulse-Width Modulation Submodule (PWMSM)** for more information.

10.4 Bus Interface Unit Submodule (BIUSM)

The BIUSM connects the SMB to the IMB and allows the CTM4 submodules to communicate with the CPU32. The BIUSM also communicates CTM4 submodule interrupt requests to the IMB, and transfers the interrupt level, arbitration number and vector number to the CPU32 during the interrupt acknowledge cycle.

10.4.1 STOP Effect On the BIUSM

When the CPU32 STOP instruction is executed, only the CPU32 is stopped; the CTM4 continues to operate as normal.

10.4.2 Freeze Effect On the BIUSM

CTM4 response to assertion of the IMB FREEZE signal is controlled by the FRZ bit in the BIUSM configuration register (BIUMCR). Since the BIUSM propagates FREEZE to the CTM4 submodules via the SMB, the setting of FRZ affects all CTM4 submodules.

If the IMB FREEZE signal is asserted and FRZ = 1, all CTM4 submodules freeze. The following conditions apply when the CTM4 is frozen:

- All submodule registers can still be accessed.
- The CPSM, FCSM, MCSM, and PWMSM counters stop counting.
- The IN status bit still reflects the state of the FCSM external clock input pin.
- The IN2 status bit still reflects the state of the MCSM external clock input pin, and the IN1 status bit still reflects the state of the MCSM modulus load input pin.
- DASM capture and compare functions are disabled.
- The DASM IN status bit still reflects the state of its associated pin in the DIS, IPWM, IPM, and IC modes. In the OCB, OCAB, and OPWM modes, IN reflects the state of the DASM output flip flop.
- When configured for OCB, OCAB, or OPWM modes, the state of the DASM



RTR	Initial TX Code	Description	Code After Successful Transmission
Х	1000	Message buffer not ready for transmit.	—
0	1100	Data frame to be transmitted once, unconditionally.	1000
1	1100	Remote frame to be transmitted once, and message buffer be- comes an RX message buffer for data frames.	0100
0	1010 ¹	Data frame to be transmitted only as a response to a remote frame, always.	1010
0	1110	Data frame to be transmitted only once, unconditionally, and then only as a response to remote frame, always.	1010

Table 13-3 Message Buffer Codes for Transmit Buffers

NOTES:

1. When a matching remote request frame is detected, the code for such a message buffer is changed to be 1110.

13.4.1.2 Fields for Extended Format Frames

Table 13-4 describes the message buffer fields used only for extended identifier format frames.

Table 13-4 Extended Format Frames

Field	Description
ID[28:18]/[17:15]	Contains the 14 most significant bits of the extended identifier, located in the ID HIGH word of the message buffer.
Substitute Remote Request (SRR)	Contains a fixed recessive bit, used only in extended format. Should be set to one by the user for TX buffers. It will be stored as received on the CAN bus for RX buffers.
ID Extended (IDE)	If extended format frame is used, this field should be set to one. If zero, standard format frame should be used.
ID[14:0]	Bits [14:0] of the extended identifier, located in the ID LOW word of the message buffer.
Remote Transmission Request (RTR)	This bit is located in the least significant bit of the ID LOW word of the message buffer; 0 = Data Frame, 1 = Remote Frame.

13.4.1.3 Fields for Standard Format Frames

Table 13-5 describes the message buffer fields used only for standard identifier format frames.



NOTES:

1. Applies to :

Port E[7:4] — SIZ[1:0], ĀS, DS Port F[7:0] — IRQ[7:1], MODCLK Port QS[7:0] — TXD, PCS[3:1], PCS0/SS, SCK, MOSI, MISO TPUCH[15:0], T2CLK, CPWM[8:5], CTD[4:3], CTD[10:9], CTM2C BKPT/DSCLK, IFETCH, RESET, RXD, TSTME/TSC EXTAL (when PLL enabled) 2. Input-Only Pins: EXTAL. TSTME/TSC, BKPT, PAI, T2CLK, RXD, CTM2C

Output-Only Pins: EXTAL, ISTME/ISC, BKPT, PAI, IZCLK, RXD, CTM2C Output-Only Pins: CSBOOT, BG/CS, CLKOUT, FREEZE/QUOT, IPIPE Input/Output Pins:

Group 1: DATA[15:0], IFETCH, TPUCH[15:0], CPWM[8:5], CTD[4:3], CTD[10:9] Group 2: Port C[6:0] — ADDR[22:19]/CS[9:6], FC[2:0]/CS[5:3] Port E[7:0] — SIZ[1:0], ĀS, DS, ĀVEC, RMC, DSACK[1:0] Port F[7:0] — IRQ[7:1], MODCLK Port QS[7:3] — TXD, PCS[3:1], PCS0/SS ADDR23/CS10/ECLK, ADDR[18:0], R/W, BERR, BR/CS0, BGACK/CS2 Group 3: HALT, RESET Group 4: MISO, MOSI, SCK

Pin groups do not include QADC pins. See Tables A-11 through A-14 for information concerning the QADC.

- 3. Does not apply to HALT and RESET because they are open drain pins. Does not apply to port QS[7:0] (TXD, PCS[3:1], PCS0/SS, SCK, MOSI, MISO) in wired-OR mode.
- 4. Use of an active pulldown device is recommended.
- 5. Total operating current is the sum of the appropriate I_{DD} , I_{DDSYN} , and I_{SB} values. I_{DD} values include supply currents for device modules powered by V_{DDE} and V_{DDI} pins.
- 6. Current measured at maximum system clock frequency, all modules active.
- 7. The SRAM module will not switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 volts. The SRAM array cannot be accessed while the module is in standby mode.
- 8. When V_{DD} is transitioning during power-up or power down sequence, and V_{SB} is applied, current flows between the V_{STBY} and V_{DD} pins, which causes standby current to increase toward the maximum transient condition specification. System noise on the V_{DD} and V_{STBY} pins can contribute to this condition.
- 9. Power dissipation measured at system clock frequency, all modules active. Power dissipation can be calculated using the following expression:

 $P_{D} = Maximum V_{DD} (Run I_{DD} + I_{DDSYN} + I_{SB}) + Maximum V_{DDA} (I_{DDA})$

10. This parameter is periodically sampled rather than 100% tested.



Table A-6 AC Timing

(V_{DD} and V_{DDSYN} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H)^1

Num	Characteristic	Symbol	Min	Max	Unit
F1	Frequency of Operation ²	f _{sys}	—	20.97	MHz
1	Clock Period	t _{cyc}	47.7	—	ns
1A	ECLK Period	t _{Ecyc}	381	—	ns
1B	External Clock Input Period ³	t _{Xcyc}	47.7	—	ns
2, 3	Clock Pulse Width	t _{CW}	18.8	—	ns
2A, 3A	ECLK Pulse Width	t _{ECW}	183	—	ns
2B, 3B	External Clock Input High/Low Time ³	t _{XCHL}	23.8	—	ns
3, 4	Clock Rise and Fall Time	t _{Crf}	_	5	ns
4A, 5A	Rise and Fall Time — All Outputs except CLKOUT	t _{rf}	_	8	ns
4B, 5B	External Clock Rise and Fall Time ⁴	t _{XCrf}	_	5	ns
4	Clock High to Address, FC, SIZE, RMC Valid	t _{CHAV}	0	23	ns
5	Clock High to Address, Data, FC, SIZE, RMC High Impedance	t _{CHAZx}	0	47	ns
6	Clock High to Address, FC, SIZE, RMC Invalid ⁵	t _{CHAZn}	0	—	ns
7	Clock Low to AS, DS, CS Asserted	t _{CLSA}	0	23	ns
8A	$\overline{\text{AS}}$ to $\overline{\text{DS}}$ or $\overline{\text{CS}}$ Asserted (Read) ⁶	t _{STSA}	-10	10	ns
8C	Clock Low to IFETCH, IPIPE Asserted	t _{CLIA}	2	22	ns
11	Address, FC, SIZE, RMC Valid to AS, CS Asserted	t _{AVSA}	10	—	ns
12	Clock Low to \overline{AS} , \overline{DS} , \overline{CS} Negated	t _{CLSN}	2	23	ns
12A	Clock Low to IFETCH, IPIPE Negated	t _{CLIN}	2	22	ns
13	AS, DS, CS Negated to Address, FC, SIZE Invalid (Address Hold)	t _{SNAI}	10	—	ns
14	AS, CS Width Asserted	t _{SWA}	80	_	ns
14A	DS, CS Width Asserted (Write)	t _{SWAW}	36	—	ns
14B	AS, CS Width Asserted (Fast Write Cycle)	t _{SWDW}	32	_	ns
15	\overline{AS} , \overline{DS} , \overline{CS} Width Negated ⁷	t _{SN}	32	—	ns
16	Clock High to \overline{AS} , \overline{DS} , R/W High Impedance	t _{CHSZ}	—	47	ns
17	\overline{AS} , \overline{DS} , \overline{CS} Negated to R/W Negated	t _{SNRN}	10	—	ns
18	Clock High to R/W High	t _{CHRH}	0	23	ns
20	Clock High to R/W Low	t _{CHRL}	0	23	ns
21	R/\overline{W} Asserted to \overline{AS} , \overline{CS} Asserted	t _{RAAA}	10	_	ns
22	R/\overline{W} Low to \overline{DS} , \overline{CS} Asserted (Write)	t _{RASA}	54	_	ns
23	Clock High to Data Out Valid	t _{CHDO}	—	23	ns
24	Data Out Valid to Negating Edge of \overline{AS} , \overline{CS}	t _{DVASN}	10	—	ns
25	DS, CS Negated to Data Out Invalid (Data Out Hold)	t _{SNDOI}	10	—	ns





68300 FAST RD CYC TIM

Figure A-6 Fast Termination Read Cycle Timing Diagram



Table A-18 DASM Timing Characteristics

 $(V_{DD} = 5.0 \text{ Vdc} \pm 5\%, V_{SS} = 0 \text{ Vdc}, T_A = T_L \text{ to } T_H)$

Num	Parameter	Symbol	Min	Max	Unit
1	Input pin low time	t _{PINL}	2.0/f _{sys}	_	μs
2	Input pin high time	t _{PINH}	2.0/f _{sys}	—	μs
3	Input capture resolution ¹	t _{RESCA}	—	2.0/f _{sys}	μs
4	Pin to input capture delay	t _{PCAPT}	2.5/f _{sys}	4.5/f _{sys}	μs
5	Pin to FLAG set	t _{PFLAG}	2.5/f _{sys}	4.5/f _{sys}	μs
6	Pin to IN bit delay	t _{PINB}	1.5/f _{sys}	2.5/f _{sys}	μs
7	OCT output pulse	t _{OCT}	2.0/f _{sys}	—	μs
8	Compare resolution	t _{RESCM}	—	2.0/f	μs
9	TBB change to FLAG set	t _{CFLAG}	1.5/f _{sys}	1.5/f _{sys}	μs
10	TBB change to pin change ²	t _{CPIN}	1.5/f _{sys}	1.5/f _{sys}	μs
11	FLAG to IMB interrupt request	t _{FIRQ}	1.0/f _{sys}	1.0/f _{sys}	μs

NOTES:

1. Minimum resolution depends on counter and prescaler divide ratio selection.

2. Time given from when new value is stable on time base bus.



Table A-19 PWMSM Timing Characteristics

 $(V_{DD} = 5.0 \text{Vdc} \pm 5\%, V_{SS} = 0 \text{Vdc}, T_A = T_L \text{ to } T_H)$

Num	Parameter	Symbol	Min	Max	Unit
1	PWMSM output resolution ¹	t _{PWMR}	-	_	μs
2	PWMSM output pulse ²	t _{PWMO}	2.0/f _{sys}	—	μs
3	PWMSM output pulse ³	t _{PWMO}	2.0/f _{sys}	2.0/f _{sys}	μs
4	CPSM enable to output set PWMSM enabled before CPSM , DIV23 = 0 PWMSM enabled before CPSM , DIV23 = 1	t _{PWMP}	3.5/f 6.5/f _{sys}	_	μs
5	PWM enable to output set PWMSM enabled before CPSM , DIV23 = 0 PWMSM enabled before CPSM , DIV23 = 1	t _{PWME}	3.5/f 5.5/f _{sys}	4.5/f 6.5/f _{sys}	μs
6	FLAG to IMB interrupt request	t _{FIRQ}	1.5/f _{sys}	2.5/f _{sys}	μs

NOTES:

1. Minimum output resolution depends on counter and prescaler divide ratio selection.

2. Excluding the case where the output is always zero.

3. Excluding the case where the output is always zero.



To reset the software watchdog:

- 1. Write \$55 to SWSR.
- 2. Write \$AA to SWSR.

Both writes must occur in the order specified before the software watchdog times out, but any number of instructions can occur between the two writes.

D.2.16 Port C Data Register

PORTC — Port C Data Register

\$YFFA41

15	8	7	6	5	4	3	2	1	0
NOT USED		0	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:									
		0	1	1	1	1	1	1	1

PORTC latches data for chip-select pins configured as discrete outputs.

D.2.17 Chip-Select Pin Assignment Registers

CSPAR0 — Chip-Select Pin Assignment Register 0

\$YFFA44

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	CS5P/	A[1:0]	CS4PA	[1:0]	CS3PA	CS3PA[1:0]		CS2PA[1:0]		CS1PA[1:0]		CS0PA[1:0]		CSBTPA[1:0]	
RES	SET:															
0	0	DATA2	1	DATA2	1	DATA2	1	DATA1	1	DATA1	1	DATA1	1	1	DATA0	

The chip-select pin assignment registers configure the chip-select pins for use as discrete I/O, an alternate function, or as an 8-bit or 16-bit chip-select. Each 2-bit field in CSPAR[0:1] (except for CSBTPA[1:0]) has the possible encoding shown in **Table D-9**.

CSxPA[1:0]	Description
00	Discrete output ¹
01	Alternate function ¹
10	Chip-select (8-bit port)
11	Chip-select (16-bit port)

Table D-9 Pin Assignment Field Encoding

NOTES:

1. Does not apply to the \overline{CSBOOT} field.

CSPAR0 contains seven 2-bit fields that determine the function of corresponding chipselect pins. Bits [15:14] are not used. These bits always read zero; writes have no effect. CSPAR0 bit 1 always reads one; writes to CSPAR0 bit 1 have no effect. The alternate functions can be enabled by data bus mode selection during reset.

 Table D-10 shows CSPAR0 pin assignments.



SCBR[12:0] - SCI Baud Rate

SCI baud rate is programmed by writing a 13-bit value to this field. Writing a value of zero to SCBR disables the baud rate generator. Baud clock rate is calculated as follows:

SCI Baud Rate =
$$\frac{f_{sys}}{32 \times SCBR[12:0]}$$

$$SCBR[12:0] = \frac{f_{sys}}{32 \times SCI Baud Rate Desired}$$

where SCBR[12:0] is in the range of 1 to 8191.

D.6.6 SCI Control Register 1

SCCR1	— SCI	Control	Register '	1
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\$YFFC0A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LOOPS	WOMS	ILT	PT	PE	М	WAKE	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCCR1 contains SCI configuration parameters, including transmitter and receiver enable bits, interrupt enable bits, and operating mode enable bits. SCCR0 can be read or written at any time. The SCI can modify the RWU bit under certain circumstances. Changing the value of SCCR1 bits during a transfer operation can disrupt the transfer.

Bit 15 — Not Implemented

- LOOPS Loop Mode
 - 0 = Normal SCI operation, no looping, feedback path disabled.
 - 1 = Test SCI operation, looping, feedback path enabled.

WOMS — Wired-OR Mode for SCI Pins

- 0 = If configured as an output, TXD is a normal CMOS output.
- 1 = If configured as an output, TXD is an open-drain output.

ILT — Idle-Line Detect Type

0 = Short idle-line detect (start count on first one).

- 1 = Long idle-line detect (start count on first one after stop bit(s)).
- PT Parity Type
 - 0 = Even parity
 - 1 = Odd parity
- PE Parity Enable
 - 0 = SCI parity disabled.
 - 1 = SCI parity enabled.

MC68336/376 USER'S MANUAL **REGISTER SUMMARY**



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