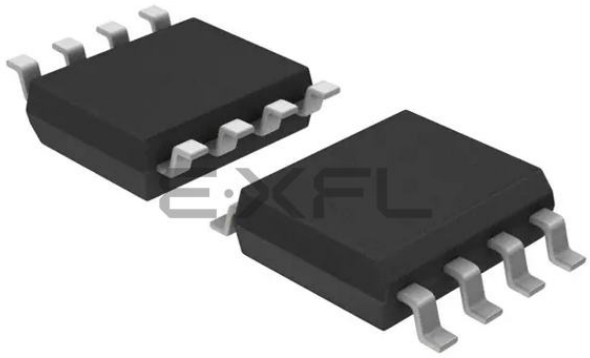

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, IR, POR, PWM, WDT
Number of I/O	6
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l001j3m3

List of figures

3.5 Memory

The STM8L001J3 devices have the following main features:

- 1.5 Kbytes of RAM
- The EEPROM is divided into two memory arrays (see the *STM8L001xx, STM8L101xx microcontroller family* reference manual (RM0013) for details on the memory mapping):
  - 8 Kbytes of low-density embedded Flash program including up to 2 Kbytes of data EEPROM. Data EEPROM and Flash program areas can be write protected independently by using the memory access security mechanism (MASS).
  - 64 option bytes (one block) of which 5 bytes are already used for the device.

Error correction code is implemented on the EEPROM.

Recommendation for the device's programming:

The device's 8 Kbytes program memory is not empty on virgin devices; there is code loop implemented on the reset vector. It is recommended to keep valid code loop in the device to avoid the program execution from an invalid memory address (which would be any memory address out of 8 Kbytes program memory space).

If the device's program memory is empty (0x00 content), it displays the behavior described below:

- After the power on, the “empty” code is executed (0x0000 opcodes = instructions: NEG (0x00, SP)) until the device reaches the end of the 8 Kbytes program memory (the end address = 0x9FFF).
  It takes around 4 milliseconds to reach the end of the 8 Kbytes memory space @2 MHz HSI clock.
- Once the device reaches the end of the 8 Kbytes program memory, the program continues and code from a non-existing memory is fetched and executed.

The reading of non-existing memory is a random content which can lead to the execution of invalid instructions.

The execution of invalid instructions generates a software reset and the program starts again. A reset can be generated every 4 milliseconds or more.

Only the “connect on-the-fly” method can be used to program the device through the SWIM interface. The “connect under-reset” method cannot be used because the NRST pin is not available on this device.

The “connect on-the-fly” mode can be used while the device is executing code, but if there is a device reset (by software reset) during the SWIM connection, this connection is aborted and it must be performed again from the debug tool. Note that the software reset occurrence can be of every 4 milliseconds, making it difficult to successfully connect to the device's debug tool (there is practically only one successful connection trial for every 10 attempts). Once that a successful connection is reached, the device can be programmed with a valid firmware without problems; therefore it is recommended that device is never erased and that is contains always a valid code loop.

16-bit general purpose timers

The 16-bit timers consist of 16-bit up/down auto-reload counters driven by a programmable prescaler. They perform a wide range of functions, including:

- Time base generation
- Measuring the pulse lengths of input signals (input capture)
- Generating output waveforms (output compare, PWM and One pulse mode)
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.12 Beeper

The STM8L001J3 devices include a beeper function used to generate a beep signal in the range of 1, 2 or 4 kHz when the LSI clock is operating at a frequency of 38 kHz.

3.13 Infrared (IR) interface

The STM8L001J3 devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.14 Comparators

The STM8L001J3 features two zero-crossing comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal (comparison with ground) or external (comparison to a reference pin voltage).

Each comparator is connected to 4 channels, which can be used to generate interrupt, timer input capture or timer break. Their polarity can be inverted.

3.15 USART

The USART interface (USART) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

3.16 SPI

The serial peripheral interface (SPI) provides half/ full duplex synchronous serial communication with external devices. It can be configured as the master and in this case it provides the communication clock (SCK) to the external slave device. The interface can also operate in multi-master configuration.

Table 6. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR	AWU control/status register	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 51FF	Reserved area (268 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205 to 0x00 520F	Reserved area (11 bytes)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215		Reserved area (1 byte)		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02

Table 6. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 521E to 0x00 522F	Reserved area (18 bytes)			
0x00 5230	USART	USART_SR	USART status register	0xC0
0x00 5231		USART_DR	USART data register	0xXX
0x00 5232		USART_BRR1	USART baud rate register 1	0x00
0x00 5233		USART_BRR2	USART baud rate register 2	0x00
0x00 5234		USART_CR1	USART control register 1	0x00
0x00 5235		USART_CR2	USART control register 2	0x00
0x00 5236		USART_CR3	USART control register 3	0x00
0x00 5237		USART_CR4	USART control register 4	0x00
0x00 5238 to 0x00 524F	Reserved area (18 bytes)			

Table 6. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5251		TIM2_CR2	TIM2 control register 2	0x00
0x00 5252		TIM2_SMCR	TIM2 slave mode control register	0x00
0x00 5253		TIM2_ETR	TIM2 external trigger register	0x00
0x00 5254		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5255		TIM2_SR1	TIM2 status register 1	0x00
0x00 5256		TIM2_SR2	TIM2 status register 2	0x00
0x00 5257		TIM2_EGR	TIM2 event generation register	0x00
0x00 5258		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5259		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 525A		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 525B		TIM2_CNTRH	TIM2 counter high	0x00
0x00 525C		TIM2_CNTRL	TIM2 counter low	0x00
0x00 525D		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 525E		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 525F		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5260		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5261		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5262		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5263		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5264		TIM2_BKR	TIM2 break register	0x00
0x00 5265		TIM2_OISR	TIM2 output idle state register	0x00
0x00 5266 to 0x00 527F	Reserved area (26 bytes)			

Table 6. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5285		TIM3_SR1	TIM3 status register 1	0x00
0x00 5286		TIM3_SR2	TIM3 status register 2	0x00
0x00 5287		TIM3_EGR	TIM3 event generation register	0x00
0x00 5288		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5289		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 528A		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 528B		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528C		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528D		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528E		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 528F		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 5290		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 5291		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 5292		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5293		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5294		TIM3_BKR	TIM3 break register	0x00
0x00 5295		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5296 to 0x00 52DF	Reserved area (74 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 52E4		TIM4_SR1	TIM4 Status register 1	0x00
0x00 52E5		TIM4_EGR	TIM4 event generation register	0x00
0x00 52E6		TIM4_CNTR	TIM4 counter	0x00
0x00 52E7		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E8		TIM4_ARR	TIM4 auto-reload register low	0xFF

Table 7. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	Breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	Breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	Breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	Breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	Breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	Breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	Debug module control register 1	0x00
0x00 7F97		DM_CR2	Debug module control register 2	0x00
0x00 7F98		DM_CSR1	Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	Enable function register	0xFF

1. Refer to *Table 6: General hardware register map on page 19* (addresses 0x00 50A0 to 0x00 50A5) for a list of external interrupt registers.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated row of the memory.

All option bytes can be modified only in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 9* for details on option byte addresses.

Refer to the *How to program STM8L and STM8AL Flash program memory and data EEPROM* programming manual (PM0054) and the *STM8 SWIM communication protocol and debug module* user manual (UM0470) for information on SWIM programming procedures.

Table 9. Option bytes

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT1	ROP[7:0]								0x00
0x4807	-	-	Reserved								0x00
0x4802	UBC (User Boot code size)	OPT2	UBC[7:0]								0x00
0x4803	DATASIZE	OPT3	DATASIZE[7:0]								0x00
0x4808	Independent watchdog option	OPT4 [1:0]	Reserved						IWDG _HALT	IWDG _HW	0x00

Table 10. Option byte description

OPT1	**ROP[7:0]** *Memory readout protection (ROP)* 0xAA: Enable readout protection (write access via SWIM protocol) Refer to *Read-out protection* section in the *STM8L001xx, STM8L101xx microcontroller family* reference manual (RM0013) for details.
OPT2	**UBC[7:0]** *Size of the user boot code area* 0x00: no UBC 0x01-0x02: UBC contains only the interrupt vectors. 0x03: Page 0 and 1 reserved for the interrupt vectors. Page 2 is available to store user boot code. Memory is write protected ... 0x7F - Page 0 to 126 reserved for UBC, memory is write protected Refer to *User boot area (UBC)* section in the *STM8L001xx, STM8L101xx microcontroller family* reference manual (RM0013) for more details. UBC[7] is forced to 0 internally by HW.

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	-25	
$I_{INJ(PIN)}$	Injected current on any pin (1)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (2)	±25	

1. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
2. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

8.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

8.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MASTER} (1)	Master clock frequency	1.8 V ≤ V_{DD} < 3.6 V	0	16	MHz
V_{DD}	Standard operating voltage	-	1.8	3.6	V
P_D (2)	Power dissipation at T_A= 125 °C for suffix 3 devices	SO8N	-	49	mW
T_A	Temperature range	1.8 V ≤ V_{DD} < 3.6 V (3 suffix version)	–40	125	°C
T_J	Junction temperature range	-40 °C ≤ T_A ≤ 125 °C (3 suffix version)	- 40	130	°C

1. $f_{MASTER} = f_{CPU}$
2. To calculate $P_{Dmax}(T_A)$ use the formula given in thermal characteristics $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in table “Thermal characteristics”

8.3.2 Power-up / power-down operating conditions

Table 15. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	20	-	1300	µs/V
t_{TEMP}	Reset release delay	V_{DD} rising	-	1	-	ms
V_{POR}(1)(2)	Power on reset threshold	-	1.35	-	1.65(3)	V
V_{PDR}(1)(2)	Power down reset threshold	-	1.40	-	1.60	V

1. Guaranteed by characterization results.
2. Correct device reset during power on sequence is guaranteed when $t_{VDD[max]}$ is respected. External reset circuit is recommended to ensure correct device reset during power down, when $V_{PDR} < V_{DD} < V_{DD[min]}$.
3. Tested in production.

8.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 16. Total current consumption in Run mode (1)

Symbol	Parameter	Conditions(2)		Typ	Max(3)	Unit
$I_{DD\ (Run)}$	Supply current in Run mode(4) (5)	Code executed from RAM	f_{MASTER} = 2 MHz	0.39	0.60	mA
			f_{MASTER} = 4 MHz	0.55	0.70	
			f_{MASTER} = 8 MHz	0.90	1.20	
			f_{MASTER} = 16 MHz	1.60	2.10(6)	
		Code executed from Flash	f_{MASTER} = 2 MHz	0.55	0.70	
			f_{MASTER} = 4 MHz	0.88	1.80	
			f_{MASTER} = 8 MHz	1.50	2.50	
			f_{MASTER} = 16 MHz	2.70	3.50	

1. Based on characterization results, unless otherwise specified.
2. All peripherals off, V_{DD} from 1.8 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{MASTER}$
3. Maximum values are given for T_A = –40 to 125 °C.
4. CPU executing typical data processing.
5. An approximate value of $I_{DD(Run)}$ can be given by the following formula: $I_{DD(Run)} = f_{MASTER}$ x 150 µA/MHz +215 µA.
6. Tested in production.

Figure 6. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 2 MHz

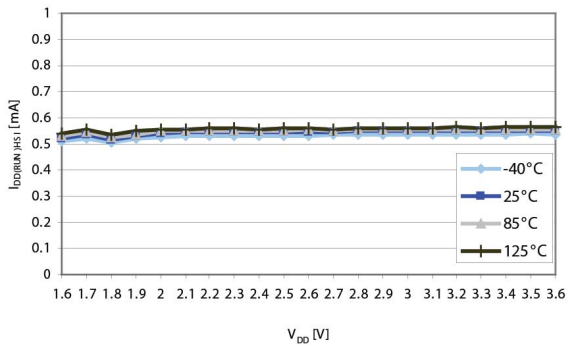
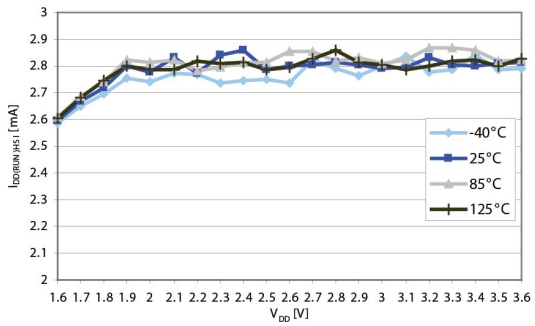


Figure 7. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



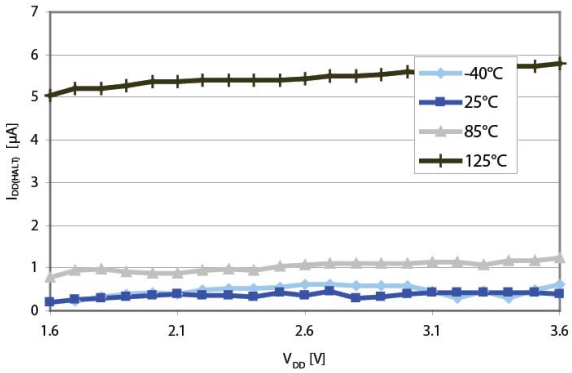
1. Typical current consumption measured with code executed from Flash.

Table 18. Total current consumption and timing in Halt and Active-halt mode at V_{DD} = 1.8 V to 3.6 V (1)(2)

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC osc. (at 37 kHz)	T_A = -40 °C to 25 °C	0.8	2	µA
			T_A = 55 °C	1	2.5	µA
			T_A = 85 °C	1.4	3.2	µA
			T_A = 105 °C	2.9	7.5	µA
			T_A = 125 °C	5.8	13	µA
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode	-	-	2	-	mA
$t_{WU(AH)}$(3)	Wakeup time from Active-halt mode to Run mode	f_{CPU}= 16 MHz		4	6.5	µs
$I_{DD(Halt)}$	Supply current in Halt mode	T_A = -40 °C to 25 °C		0.35	1.2(4)	µA
		T_A = 55 °C		0.6	1.8	µA
		T_A = 85 °C		1	2.5(4)	µA
		T_A = 105 °C		2.5	6.5	µA
		T_A = 125 °C		5.4	12(4)	µA
$I_{DD(WUFH)}$	Supply current during wakeup time from Halt mode			2	-	mA
$t_{WU(Halt)}$(3)	Wakeup time from Halt mode to Run mode	f_{CPU} = 16 MHz		4	6.5	µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Guaranteed by characterization results.
3. Measured from interrupt event to interrupt vector fetch.
   To get t_{WU} for another CPU frequency use $t_{WU}(FREQ) = t_{WU}(16\ MHz) + 1.5\ (T_{FREQ}-T_{16\ MHz})$.
   The first word of interrupt routine is fetched 5 CPU cycles after t_{WU}.
4. Tested in production.

Figure 10. Typ. $I_{DD(Halt)}$ vs. V_{DD}, f_{CPU} = 2 MHz and 16 MHz



1. Typical current consumption measured with code executed from Flash.

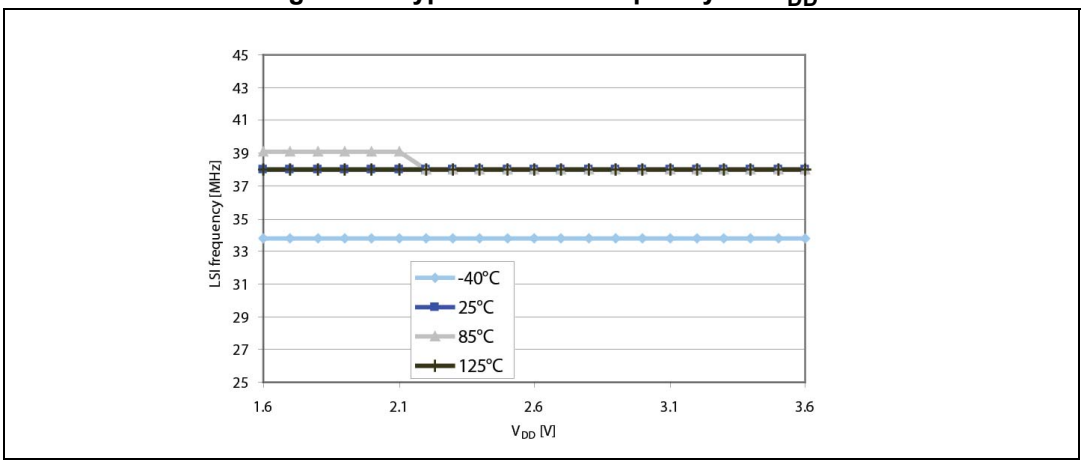
Low speed internal RC oscillator (LSI)

Table 21. LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$f_{drift(LSI)}$	LSI oscillator frequency drift(2)	0 °C ≤ T_A ≤ 85 °C	-12	-	11	%

1. V_{DD} = 1.8 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. For each individual part, this value is the frequency drift from the initial measured frequency.

Figure 14. Typical LSI RC frequency vs. V_{DD}



8.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 22. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization results.

Flash memory

Table 23. Flash program memory

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{MASTER} = 16 MHz	1.8	-	3.6	V
t_{prog}	Programming time for 1- or 64-byte (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1- to 64-byte (block) write cycles (on erased byte)	-	-	3	-	ms

Inter IC control interface (I2C)

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

The STM8L I^2C interface meets the requirements of the Standard I^2C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 29. I2C characteristics

Symbol	Parameter	Standard mode I2C		Fast mode I2C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0 (3)	-	0 (4)	900 (3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SCK} must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL).

Note: For speeds around 200 kHz, achieved speed can have ±5% tolerance
For other speed ranges, achieved speed can have ±2% tolerance
The above variations depend on the accuracy of the external components used.

11 Revision history

Table 38. Document revision history

Date	Revision	Changes
06-Jun-2017	1	Initial release.
04-Oct-2017	2	Updated: – Document's confidentiality level to *public* – *Section 1: Introduction* – *Section 2: Description* – *Section 9: Package information* – *Figure 26: SPI timing diagram - slave mode and CPHA = 1*(1) – *Figure 27: SPI timing diagram - master mode*(1) – *Figure 28: Typical application with I2C bus and timing diagram (1)*
04-Jul-2018	3	Updated: – *Recommendations for SWIM pin (pin#1)* on *Section 3.3: Single wire data interface (SWIM) and debug module*

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