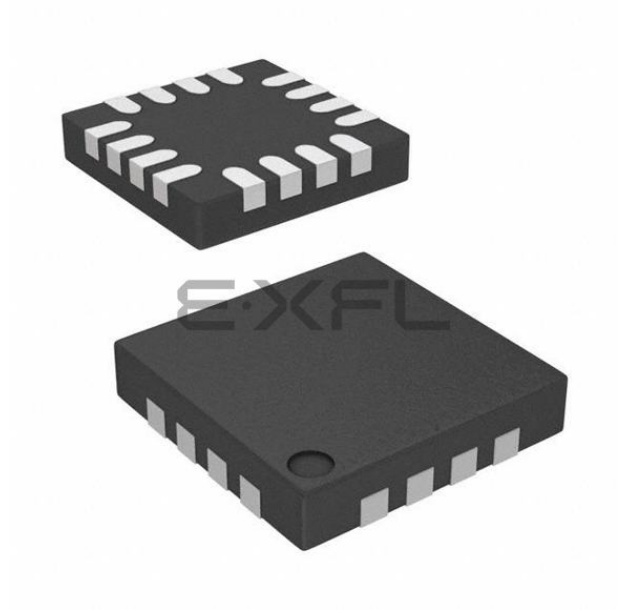

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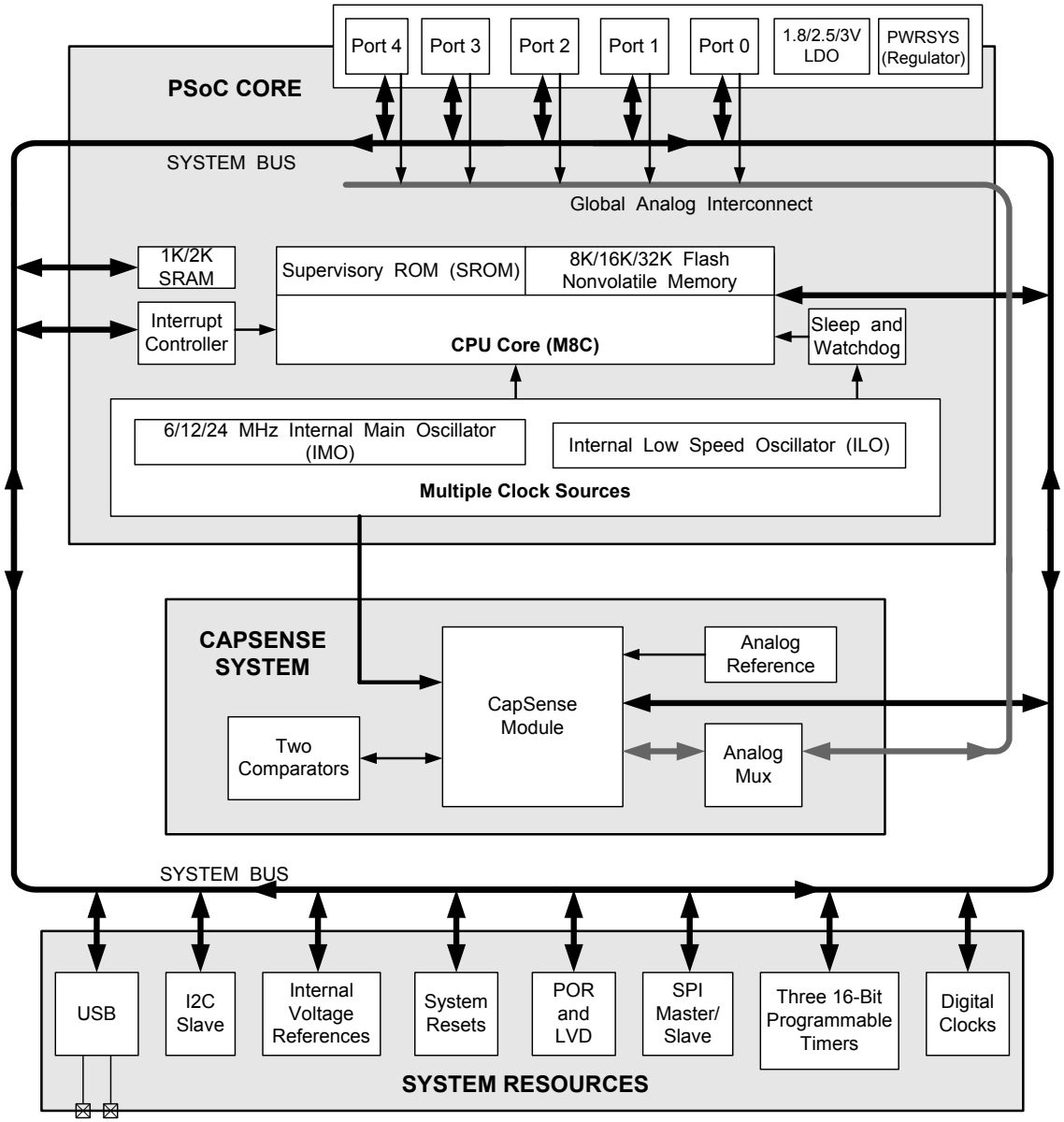
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (8kB)
Controller Series	CY8C20xx6
RAM Size	1K x 8
Interface	I²C, SPI
Number of I/O	13
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20236-24lkxi

Logic Block Diagram



PSoC® Functional Overview

The PSoC family consists of on-chip Controller devices. These devices are designed to replace multiple traditional MCU-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, is comprised of three main areas: the Core, the CapSense Analog System, and the System Resources (including a full speed USB port). A common, versatile bus allows connection between I/O and the analog system. Each CY8C20x36/46/66/96 PSoC Device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 general purpose IO (GPIO) are also included. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard architecture microprocessor.

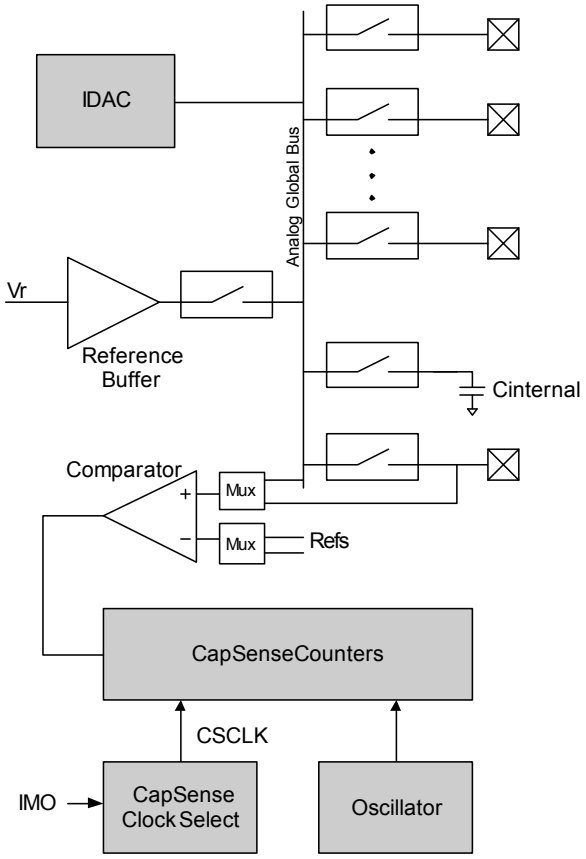
System Resources provide additional capability, such as configurable USB and I2C slave/SPI master-slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

The Analog System is composed of the CapSense PSoC block and an internal 1.2V analog reference, which together support capacitive sensing of up to 36 inputs.

CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

When designing capacitive sensing applications, refer to the latest signal-to-noise signal level requirements Application Notes, which can be found under http://www.cypress.com > Documentation > Application Notes. In general, and unless otherwise noted in the relevant Application Notes, the minimum signal-to-noise ratio (SNR) for CapSense applications is 5:1.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

The system-level view is a drag-and-drop visual embedded system design environment based on PSoC Express. In this view you solve design problems the same way you might think about the system. Select input and output devices based upon system requirements. Add a communication interface and define the interface to the system (registers). Define when and how an output device changes state based upon any/all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC devices that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.x. You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of pre-built, pre-tested hardware peripheral components. In the system-level view these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view the components are called “user modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system-level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog-to-digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, you perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

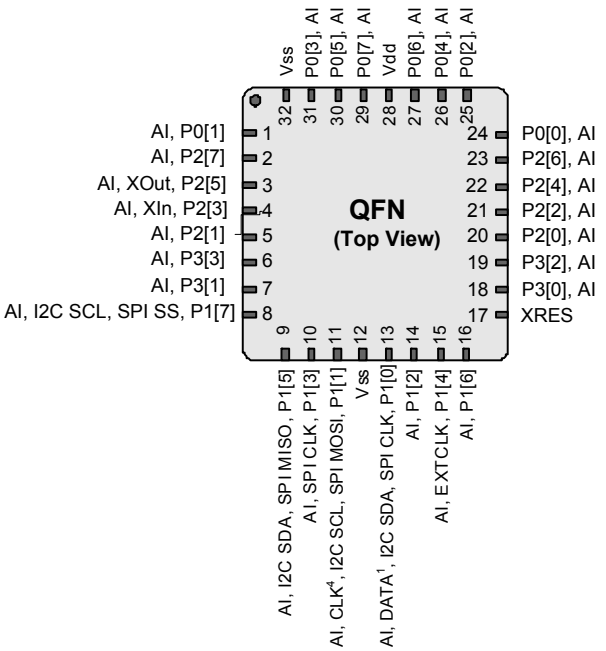
32-Pin QFN

Table 5. Pin Definitions - CY8C20436, CY8C20446, CY8C20466 PSoC Device [2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I2C SCL, SPI SS
9	IOHR	I	P1[5]	I2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI.
12	Power		Vss	Ground connection.
13	IOHR	I	P1[0]	ISSP DATA[1], I2C SDA., SPI CLK
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		Vdd	Supply voltage
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating input
32	Power		Vss	Ground connection
CP	Power		Vss	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 5. CY8C20436, CY8C20446, CY8C20466 PSoC Device



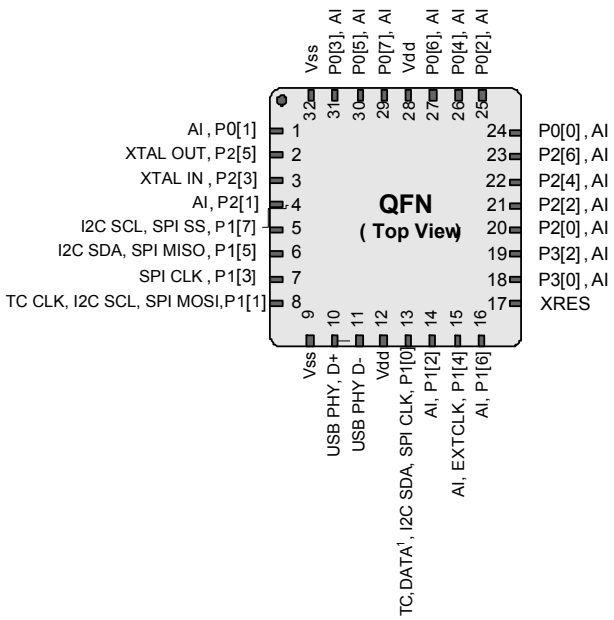
32-Pin QFN (with USB)

Table 6. Pin Definitions - CY8C20496 PSoC Device [2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	
2	I/O	I	P2[5]	XTAL Out
3	I/O	I	P2[3]	XTAL In
4	I/O	I	P2[1]	
5	IOHR	I	P1[7]	I2C SCL, SPI SS
6	IOHR	I	P1[5]	I2C SDA, SPI MISO
7	IOHR	I	P1[3]	SPI CLK
8	IOHR	I	P1[1]	TC CLK, I2C SCL, SPI MOSI
9	Power		V_{SS}	Ground Pin
10	I		D+	USB PHY
11	I		D-	USB PHY
12	Power		Vdd	Power pin
13	IOHR	I	P1[0]	TC DATA*, I2C SDA, SPI CLKI
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	EXTCLK
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		Vdd	Power Pin
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	
32	Power		Vss	Ground Pin

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 5. CY8C20496 PSoC Device

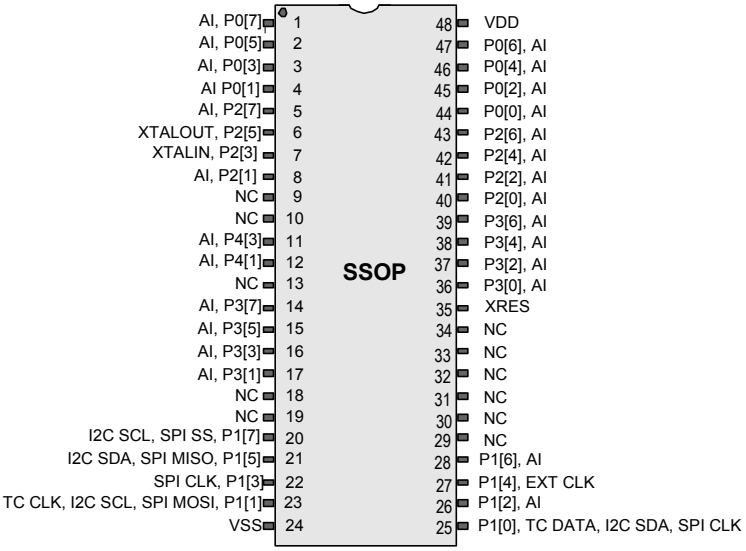


48-Pin SSOP

Table 7. Pin Definitions - CY8C20536, CY8C20546, and CY8C20566 PSoC Device[2]

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[7]	
2	IOH	I	P0[5]	
3	IOH	I	P0[3]	
4	IOH	I	P0[1]	
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	XTAL Out
7	I/O	I	P2[3]	XTAL In
8	I/O	I	P2[1]	
9			NC	No connection
10			NC	No connection
11	I/O	I	P4[3]	
12	I/O	I	P4[1]	
13			NC	No connection
14	I/O	I	P3[7]	
15	I/O	I	P3[5]	
16	I/O	I	P3[3]	
17	I/O	I	P3[1]	
18			NC	No connection
19			NC	No connection
20	IOHR	I	P1[7]	I2C SCL, SPI SS
21	IOHR	I	P1[5]	I2C SDA, SPI MISO
22	IOHR	I	P1[3]	SPI CLK
23	IOHR	I	P1[1]	TC CLK[1], I2C SCL, SPI MOSI
24			VSS	Ground Pin
25	IOHR	I	P1[0]	TC DATA[1], I2C SDA, SPI CLK
26	IOHR	I	P1[2]	
27	IOHR	I	P1[4]	EXT CLK
28	IOHR	I	P1[6]	
29			NC	No connection
30			NC	No connection
31			NC	No connection
32			NC	No connection
33			NC	No connection
34			NC	No connection
35			XRES	Active high external reset with internal pull down
36	I/O	I	P3[0]	
37	I/O	I	P3[2]	
38	I/O	I	P3[4]	
39	I/O	I	P3[6]	
40	I/O	I	P2[0]	
41	I/O	I	P2[2]	
42	I/O	I	P2[4]	
43	I/O	I	P2[6]	
44	IOH	I	P0[0]	
45	IOH	I	P0[2]	
46	IOH	I	P0[4]	
47	IOH	I	P0[6]	
48	Power		Vdd	Power Pin

Figure 6. CY8C20536, CY8C20546, and CY8C20566 PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36/46/66/96 PSoC devices. For the latest electrical specifications, confirm that you have the most recent data sheet by visiting the web at http://www.cypress.com/psoc.

Figure 10. Voltage versus CPU Frequency

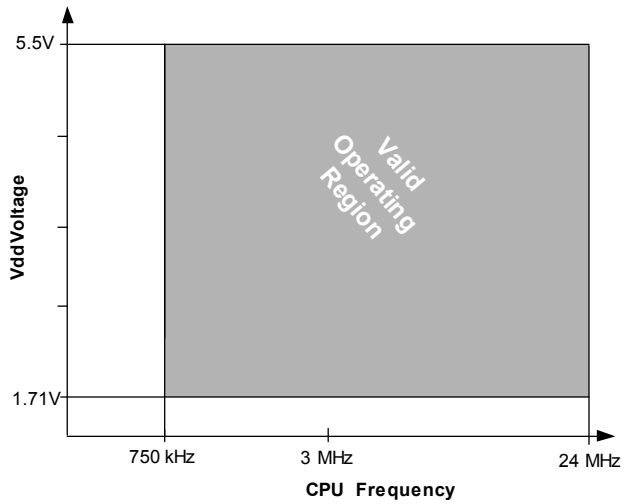
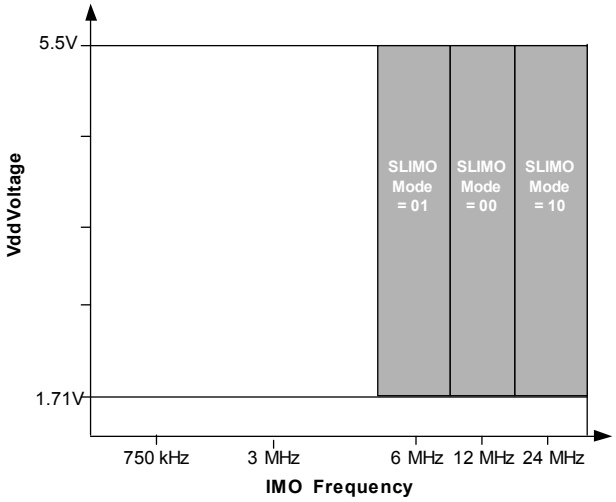


Figure 11. IMO Frequency Trim Options



The following table lists the units of measure that are used in this section.

Table 11. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	mA	milli-ampere
dB	decibels	ms	milli-second
fF	femto farad	mV	milli-volts
Hz	hertz	nA	nanoampere
KB	1024 bytes	ns	nanosecond
Kbit	1024 bits	nV	nanovolts
kHz	kilohertz	Ω	ohm
ksps	kilo samples per second	pA	picoampere
kΩ	kilohm	pF	picofarad
MHz	megahertz	pp	peak-to-peak
MΩ	megaohm	ppm	parts per million
µA	microampere	ps	picosecond
µF	microfarad	sps	samples per second
µH	microhenry	s	sigma: one standard deviation
µs	microsecond	V	volts
µW	microwatts		

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 12. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage Temperature	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
Vdd	Supply Voltage Relative to Vss		–0.5	–	+6.0	V
V_{IO}	DC Input Voltage		Vss – 0.5	–	Vdd + 0.5	V
V_{IOZ}	DC Voltage Applied to Tri-state		Vss –0.5	–	Vdd + 0.5	V
I_{MIO}	Maximum Current into any Port Pin		–25	–	+50	mA
ESD	Electro Static Discharge Voltage	Human Body Model ESD	2000	–	–	V
LU	Latch up Current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 13. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient Temperature		–40	–	+85	°C
T_J	Operational Die Temperature	The temperature rise from ambient to junction is package specific. Refer the table Thermal Impedances per Package on page 34. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
	Vdd Value for PPOR Trip	Vdd must be greater than or equal to 1.71V during startup, reset from the XRES pin, or reset from watchdog.				
V_{PPOR0}	PORLEV[1:0] = 00b, HPOR = 0		1.61	1.66	1.71	V
V_{PPOR1}	PORLEV[1:0] = 00b, HPOR = 1			2.36	2.41	V
V_{PPOR2}	PORLEV[1:0] = 01b, HPOR = 1		–	2.60	2.66	V
V_{PPOR3}	PORLEV[1:0] = 10b, HPOR = 1			2.82	2.95	V
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b		2.40[6]	2.45	2.51	V
V_{LVD1}	VM[2:0] = 001b		2.64[7]	2.71	2.78	V
V_{LVD2}	VM[2:0] = 010b		2.85[8]	2.92	2.99	V
V_{LVD3}	VM[2:0] = 011b		2.95	3.02	3.09	V
V_{LVD4}	VM[2:0] = 100b		3.06	3.13	3.20	V
V_{LVD5}	VM[2:0] = 101b		1.84	1.90	2.32	V
V_{LVD6}	VM[2:0] = 110b		1.75[9]	1.80	1.84	V
V_{LVD7}	VM[2:0] = 111b		4.62	4.73	4.83	V

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 24. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations		1.71	–	5.25	V
I_{DDP}	Supply Current During Programming or Verify		–	5	25	mA
V_{ILP}	Input Low Voltage During Programming or Verify	See the appropriate DC General Purpose IO Specifications on page 19	–	–	V_{IL}	V
V_{IHP}	Input High Voltage During Programming or Verify	See appropriate DC General Purpose IO Specifications on page 19 table on pages 15 or 16	V_{IH}	–	–	V
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor	–	–	0.2	mA
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor	–	–	1.5	mA
V_{OLP}	Output Low Voltage During Programming or Verify		–	–	Vss + 0.75	V
V_{OHP}	Output High Voltage During Programming or Verify	See appropriate DC General Purpose IO Specifications on page 19 table on page 16. For Vdd > 3V use V_{OH4} in Table 13 on page 18.	V_{OH}	–	Vdd	V
$Flash_{ENPB}$	Flash Write Endurance	Erase/write cycles per block	50,000	–	–	-
$Flash_{DR}$	Flash Data Retention	Following maximum Flash write cycles; ambient temperature of 55°C	10	20	–	Years

Notes
6. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
7. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
8. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
9. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 25. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU Frequency		5.7	–	25.2	MHz
F_{32K1}	Internal Low Speed Oscillator Frequency		19	32	50	kHz
F_{IMO24}	Internal Main Oscillator Frequency at 24 MHz Setting		22.8	24	25.2	MHz
F_{IMO12}	Internal Main Oscillator Frequency at 12 MHz Setting		11.4	12	12.6	MHz
F_{IMO6}	Internal Main Oscillator Frequency at 6 MHz Setting		5.7	6.0	6.3	MHz
DC_{IMO}	Duty Cycle of IMO		40	50	60	%
T_{RAMP}	Supply Ramp Time		20	–	–	µs
T_{XRST}	External Reset Pulse Width at Power Up	After supply voltage is valid	1			ms
T_{XRST2}	External Reset Pulse Width after Power Up[10]	Applies after part has booted	10			µs

Note
10. The minimum required XRES pulse length is longer when programming the device (see Table 32 on page 28).

AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 26. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO Operating Frequency	Normal Strong Mode Port 0, 1	0 0	– –	6 MHz for 1.71V<Vdd<2.4V 12 MHz for 2.4V<Vdd<5.5V	MHz
TRise23	Rise Time, Strong Mode, Cload = 50 pF Ports 2 or 3	Vdd = 3.0 to 3.6V, 10% – 90%	15	–	80	ns
TRise23L	Rise Time, Strong Mode Low Supply, Cload = 50 pF, Ports 2 or 3	Vdd = 1.71 to 3.0V, 10% – 90%	15	–	80	ns
TRise01	Rise Time, Strong Mode, Cload = 50 pF Ports 0 or 1	Vdd = 3.0 to 3.6V, 10% – 90% LDO enabled or disabled	10	–	50	ns
TRise01L	Rise Time, Strong Mode Low Supply, Cload = 50 pF, Ports 0 or 1	Vdd = 1.71 to 3.0V, 10% – 90% LDO enabled or disabled	10	–	80	ns
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	Vdd = 3.0 to 3.6V, 10% – 90%	10	–	50	ns
TFallL	Fall Time, Strong Mode Low Supply, Cload = 50 pF, All Ports	Vdd = 1.71 to 3.0V, 10% – 90%	10	–	70	ns

Figure 12. GPIO Timing Diagram

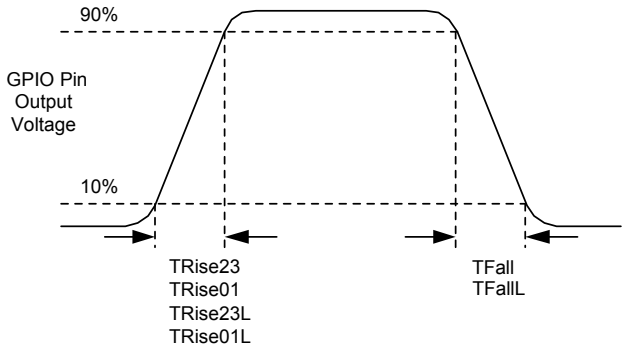


Table 27.AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full speed data rate	Average bit rate	12–0.25%	12	12 + 0.25%	MHz
Tdjr1	Receiver data jitter tolerance	To next transition	-18.5	–	18.5	ns
Tdjr2	Receiver data jitter tolerance	To pair transition	-9	–	9	ns
Tudj1	Driver differential jitter	To next transition	-3.5	–	3.5	ns
Tudj2	Driver differential jitter	To pair transition	-4.0	–	4.0	ns
Tfdeop	Source jitter for differential transition	To SE0 transition	-2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–		ns
Tfst	Width of SE0 interval during differential transition			–	14	ns

Table 28.AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	–	20	ns
Tf	Transition fall time	50 pF	4	–	20	ns
TR	Rise/fall time matching		90.00	–	111.1	%
Vcrs	Output signal crossover voltage		1.3	–	2.0	V

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{LPC}	Comparator Response Time, 50 mV Overdrive	50 mV overdrive does not include offset voltage.			100	ns

AC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 30. AC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SW}	Switch Rate	Maximum pin voltage when measuring switch rate is 1.8Vp-p	–	–	6.3	MHz

AC External Clock Specifications

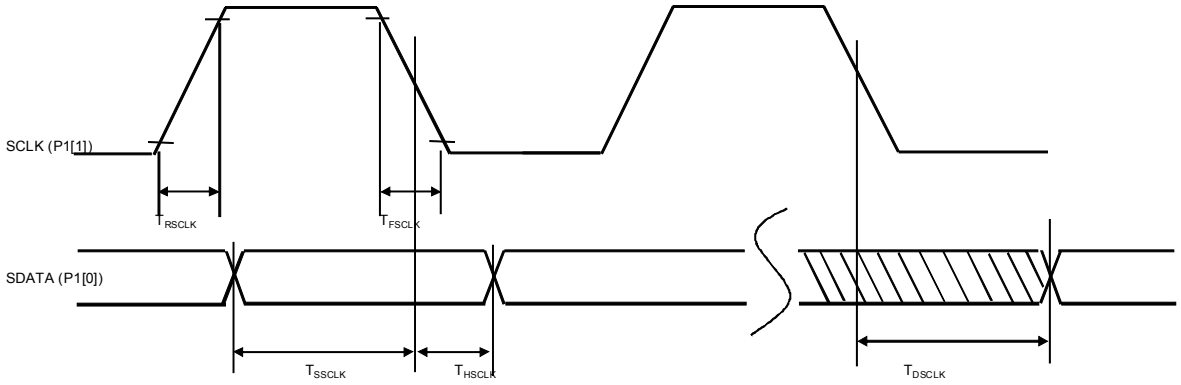
The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 31. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High Period		20.6	–	5300	ns
–	Low Period		20.6	–	–	ns
–	Power Up IMO to Switch		150	–	–	µs

AC Programming Specifications

Figure 13. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 32. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK		1	–	20	ns
T_{FSCLK}	Fall Time of SCLK		1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK		40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)		–	–	18	ms
T_{WRITE}	Flash Block Write Time		–	–	25	ms
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	3.6 < Vdd	–	–	60	ns
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	3.0 ≤ Vdd ≤ 3.6	–	–	85	ns
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	1.71 ≤ Vdd ≤ 3.0	–	–	130	ns
T_{XRST3}	External Reset Pulse Width after Power Up	Required to enter programming mode when coming out of sleep	263	–	–	µs

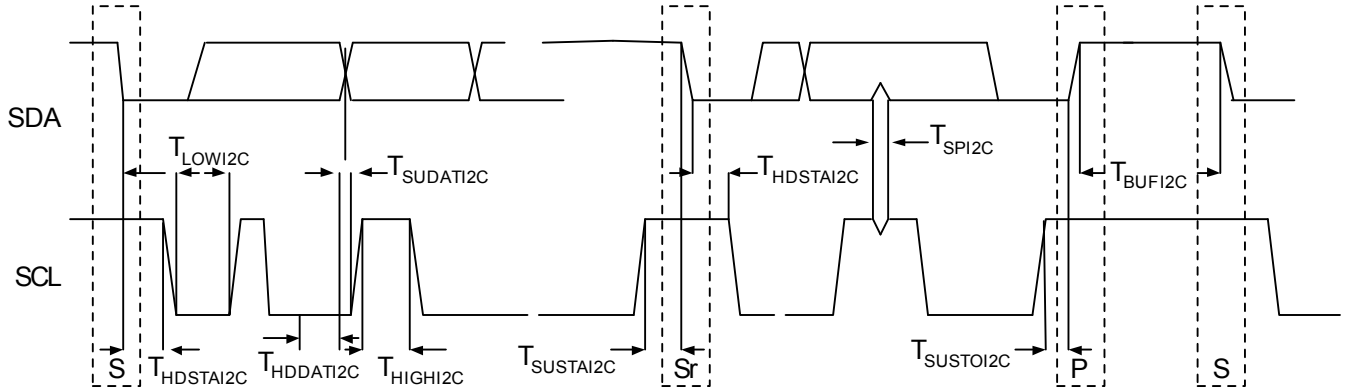
AC I2C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 33. AC Characteristics of the I2C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[11]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

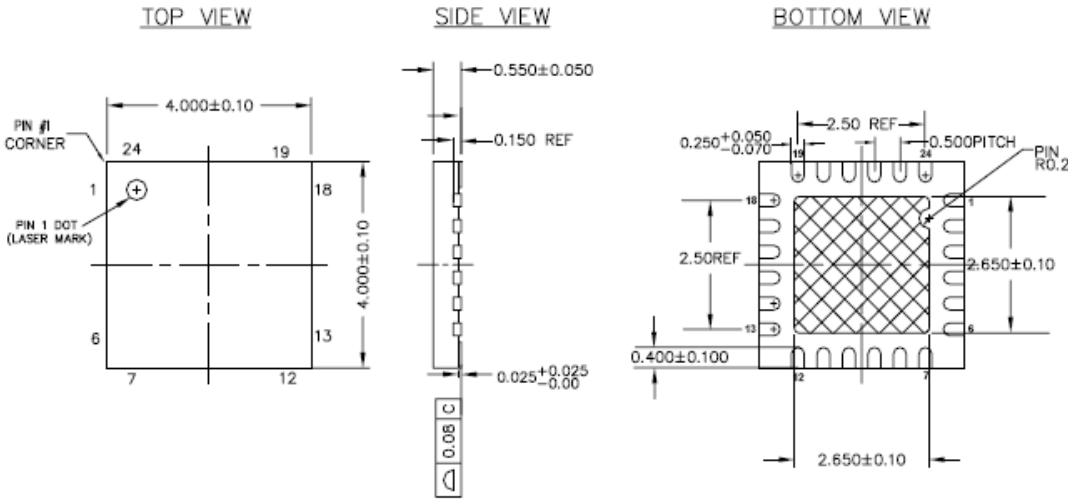
Figure 14. Definition for Timing for Fast/Standard Mode on the I^2C Bus



Note

11. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 16. 24-Pin (4x4 x 0.6 mm) QFN

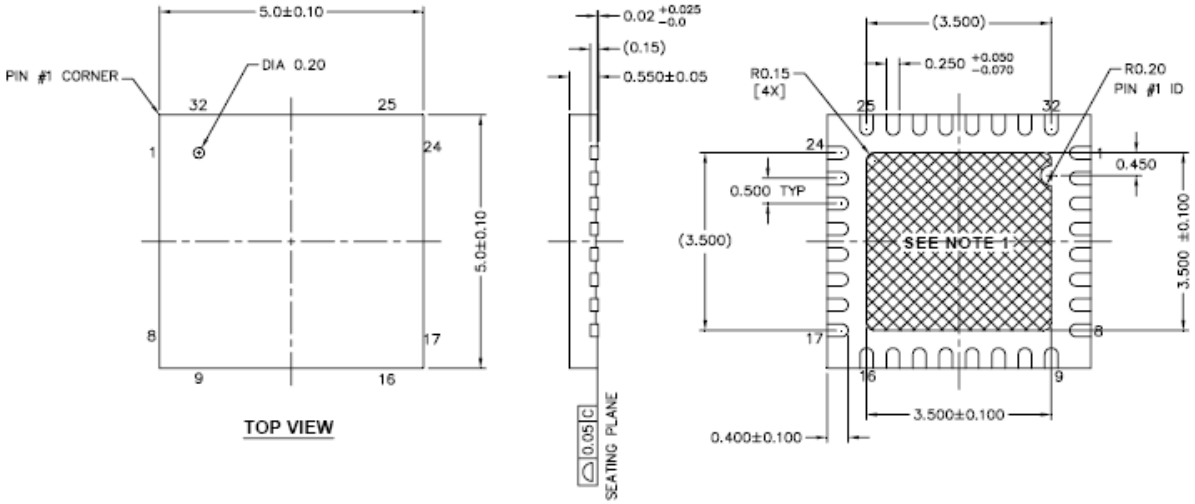


NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. UNIT PACKAGE WEIGHT : 0.024 grams
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *B

Figure 17. 32-Pin (5x5 x 0.6 mm) QFN



TOP VIEW

SIDE VIEW

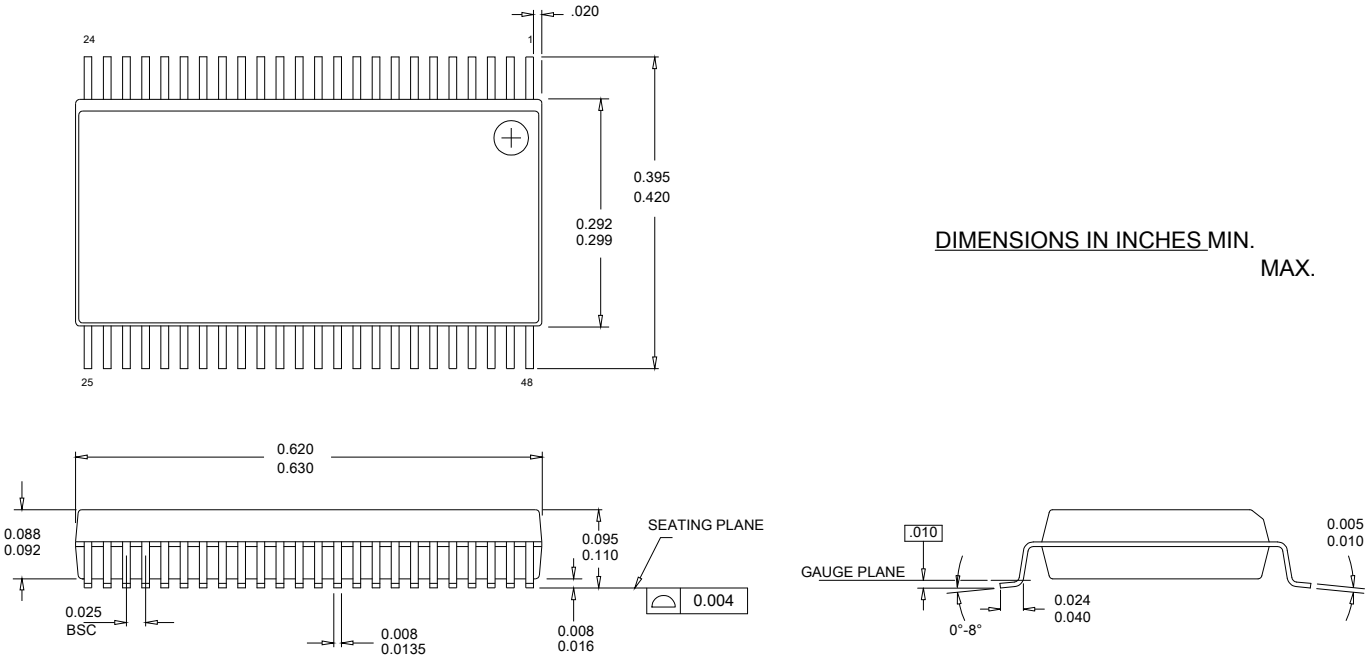
BOTTOM VIEW

NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

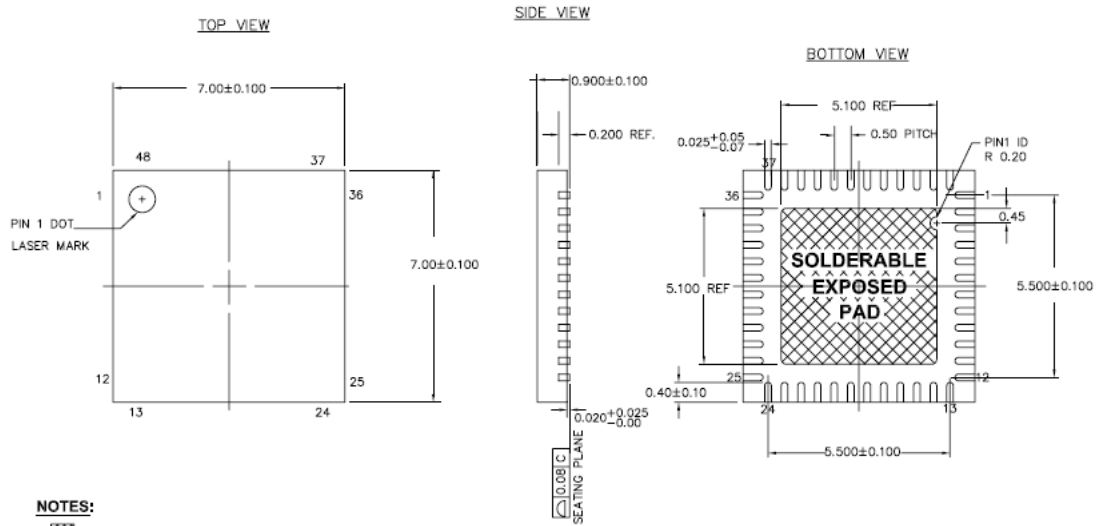
001-42168 *C

Figure 18. 48-Pin (300 MIL) SSOP



51-85061 *C

Figure 19. 48-Pin (7x7 mm) QFN



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *C

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of cost at http://www.cypress.com/psocprogrammer.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.
Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 38. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit[15]	Foot Kit[16]	Adapter[17]
CY8C20236-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-RK	See note 15
CY8C20246-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-FK	See note 17
CY8C20336-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 15
CY8C20346-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 17
CY8C20396-24LQXI	24 QFN	Not Available		
CY8C20436-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-RK	See note 15
CY8C20446-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 17
CY8C20466-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 17
CY8C20496-24LQXI	32 QFN	Not Available		
CY8C20536-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20546-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20566-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 17
CY8C20636-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17
CY8C20646-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17
CY8C20666-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 17

Third-Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com/?rID2748.

Notes
15. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
16. Foot kit includes surface mount feet that can be soldered to the target PCB.
17. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

The following table lists the CY8C20x36/46/66/96 PSoC devices' key package features and ordering codes.

Table 39. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs[18]	XRES Pin	USB
16-Pin (3x3x0.6mm) QFN	CY8C20236-24LKXI	8K	1K	1	13	13	Yes	No
16-Pin (3x3x0.6mm) QFN (Tape and Reel)	CY8C20236-24LKXIT	8K	1K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN	CY8C20246-24LKXI	16K	2K	1	13	13	Yes	No
16 Pin (3x3 x 0.6 mm) QFN (Tape and Reel)	CY8C20246-24LKXIT	16K	2K	1	13	13	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20336-24LQXI	8K	1K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20336-24LQXIT	8K	1K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN	CY8C20346-24LQXI	16K	2K	1	20	20	Yes	No
24 Pin (4x4 x 0.6 mm) QFN (Tape and Reel)	CY8C20346-24LQXIT	16K	2K	1	20	20	Yes	No
24-Pin (4x4x0.6mm) QFN	CY8C20396-24LQXI	16K	2K	1	19	19	Yes	Yes
24-Pin (4x4x0.6mm) QFN (Tape and Reel)	CY8C20396-24LQXIT	16K	2K	1	19	19	Yes	Yes
32-Pin (5x5x0.6mm) QFN	CY8C20436-24LQXI	8K	1K	1	28	28	Yes	No
32-Pin (5x5x0.6mm) QFN (Tape and Reel)	CY8C20436-24LQXIT	8K	1K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20446-24LQXI	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20446-24LQXIT	16K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20466-24LQXI	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20466-24LQXIT	32K	2K	1	28	28	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20496-24LQXI	16K	2K	1	25	25	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20496-24LQXIT	16K	2K	1	25	25	Yes	No
48-Pin SSOP	CY8C20536-24PVXI	8K	1K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20536-24PVXIT	8K	1K	1	36	36	Yes	No
48-Pin SSOP	CY8C20546-24PVXI	16K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20546-24PVXIT	16K	2K	1	36	36	Yes	No
48-Pin SSOP	CY8C20566-24PVXI	32K	2K	1	36	36	Yes	No
48-Pin SSOP (Tape and Reel)	CY8C20566-24PVXIT	32K	2K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20636-24LTXI	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20636-24LTXIT	8K	1K	1	36	36	Yes	No
48 Pin (7x7 mm) QFN	CY8C20646-24LTXI	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20646-24LTXIT	16K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN	CY8C20666-24LTXI	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20666-24LTXIT	32K	2K	1	36	36	Yes	Yes
48 Pin (7x7 mm) QFN (OCD)[4]	CY8C20066-24LTXI	32K	2K	1	36	36	Yes	Yes

Notes
18. Dual-function Digital I/O Pins also connect to the common analog mux.